Fabrication and Electrical Characterization of Floating Gate NAND Flash Transistor

A dissertation submitted in partial fulfillment of
the requirements for the degree of

Master of Technology

by

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Under the guidance of
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June, 2012

To my parents

Dissertation Approval

The dissertation entitled

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is approved for the degree of

Master of Technology

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Date: _____ Mayur Waikar

Abstract

Flash memory devices are increasingly expected to provide not only greater storage density, but also faster access to information. This has lead to scaling of flash memory to 30 nm node and now industry is targeting 22 nm node. To continue the scaling trend with better memory performance, all the attention is being given to the floating gate and blocking dielectric materials without modifying device structure. The low power PVD Al_2O_3 is optimized for blocking dielectric. The SiO_2 which is used as the tunnel oxide has been optimized. The process flow for floating gate flash transistor is established, mask is designed for third level as gate last process has been used. The graphene floating gate flash transistor has been fabricated successfully and has shown good program window. The problem with the erase of the cell needs to be resolved. The study of interaction between graphene and Al_2O_3 has been done as graphene has been embedded in the tunnel SiO_2 and blocking Al_2O_3 dielectrics it was important to investigate its interaction with dielectrics. The hybrid floating gate metal-graphene (Pt-Gr) flash transistor was fabricated and was characterized for memory performance. The platinum floating gate transistor has shown good program window but there is problem with the erase of the cell, for longer erase pulse duration some programming effect is observed. The most interesting results are with the Pt-Gr floating gate it shows erasing for positive stress and programming effect for negative stress thus cause for this needs to be investigated.

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Chapter 1

Introduction

1.1 Motivation

Flash memory devices are increasingly expected to provide not only greater storage density, but also faster access to information. This has lead to scaling of flash memory to 30 nm node and now industry is targeting 22 nm node. To continue the scaling trend with better memory performance, all the attention is being given to the floating gate and blocking dielectric materials without modifying device structure.

The motivation behind low power pulsed DC reactive sputtered Al_2O_3 experiments was to optimize the dielectric stack of the flash memory to meet the aforementioned requirements of flash memory for blocking dielectric.

The three figure of merits (FOM) of flash memory device are:

- Memory window
- Retention, Endurance
- Cell to cell interference

The graphene was explored as a floating gate due to its three exceptional intrinsic properties:

- High density of states
- High work function
- Atomic thinness

when compared to the conventional materials used for the two types of flash memory structures.

The motivation behind graphene floating gate flash transistor fabrication was to achieve the FOMs of flash memory by using the unique properties of graphene.

1.2 Thesis Outline

Chapter 1 was an introduction to Flash Memory. **Chapter 2** would be discussing the High power pulsed DC reactive sputtered Al_2O_3 study in detail. **Chapter 3** would be discussing the SiO_2/Al_2O_3 dielectric stack optimization with low power pulsed DC reactive sputtered Al_2O_3 for flash memory application. **Chapter 4** has a detailed study of fabrication and electrical characterization of graphene floating gate flash transistor. **Chapter 5** would be discussing the interaction of graphene with High-k Al_2O_3 dielectric and effect of this interaction on work function of graphene. **Chapter 6** would be discussing the fabrication and electrical characterization of hybrid platinum-graphene (PtGr) and metal (Pt) floating gate flash transistor and difference obtained in their electrical characteristics. **Chapter 7** would conclude the work and list out the possible improvements which can be worked upon in future with the list of publications and contribution to them from this thesis work. **Appendix A** would contain the detail process flow for graphene floating gate flash transistor.

Chapter 2

High Power Pulsed-DC Reactive Sputtered Al_2O_3 Study

High-k Al_2O_3 is being extensively investigated for blocking oxide in flash memories [1]. Reactive sputtering is an attractive option as the resultant film would be free of organic and other contaminants, which could be a problem in chemical vapour deposition (CVD) processes [2,3]. Also CVD technique requires expensive precursors which are generally hazardous and thus also needs expensive safety equipments. Whereas the pulse-DC supply used in reactive sputtering avoids these requirements of CVD and also does not require an impedance matching network unlike an RF sputtering process. These factors significantly reduce the cost of deposited films. However sputter deposited films have historically shown poor electrical characteristics as compared to CVD films due to sputter damage and low density [4].

Al_2O_3 thin film is deposited by reactive sputtering of high purity aluminium target (99.9995% pure) with O_2 as a reactive gas and Ar as sputtering gas which generates heavy Ar+ ions to remove atoms from the target surface. A schematic of the sputter system is shown in Fig 2.1. Al target is connected to the cathode where a pulsed- DC supplies continuous negative/positive pulses (V_P), while the substrate is connected to anode which is grounded. With pulsed supply continuous dielectric sputtering is possible with an arc free environment because, during pulse reversal (i.e. positive voltage) the attracted electrons neutralise the charges which builds-up on the surface of the target and chamber walls during the negative part of the pulse [5, 6]. Almost every reactive sputtering system has magnets connected to the chamber to confine the plasma near substrate surface and to increase the number of electrons for higher deposition rate due to secondary ionizations [7]. To obtain high quality Al_2O_3 dielectric film

using reactive sputter technique we optimized process parameters like gas flow ratio and applied process power. The films were characterized using spectroscopic ellipsometry (SE) for thickness and refractive index measurements. Metal- Oxide- Semiconductor (MOS) capacitors were fabricated and characterized by capacitance versus gate voltage (C-V) and gate current versus gate voltage (I-V) measurements to study the electrical properties of the film. *For the data in this chapter I have refered to published paper the details of which are in list of publications at no.4 with contribution from this thesis*.

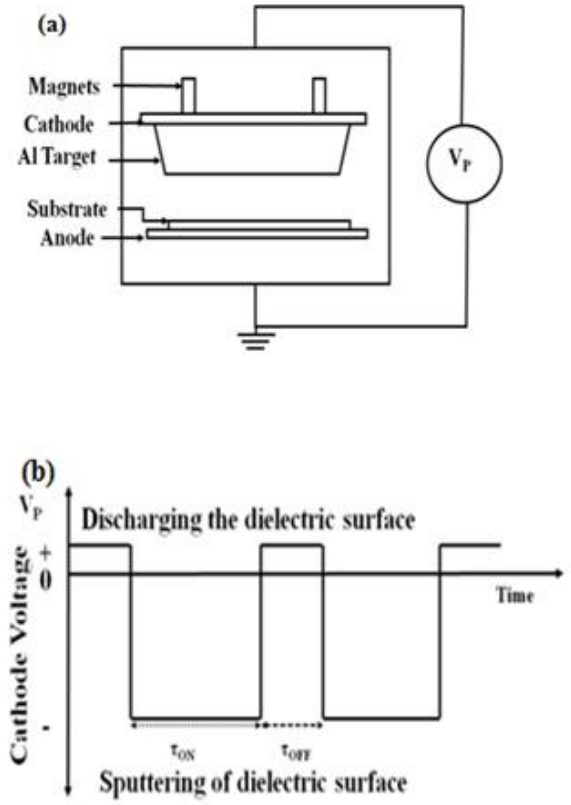

Figure 2.1: (a) Schematic of the reactive sputtering system with Aluminum as target connected to cathode and substrate is grounded through anode. (b)The waveform generated by pulsed- DC supply (V_P). Time τ_{ON} is target surface sputtering time and τ_{OFF} is the time when charges at the target surface get neutralized.

2.1 Experimental Details

The Al_xO_y dielectric film was deposited on $4''$ p-type Si (100) wafers in PVD chamber of Applied Materials ENDURA cluster tool. Prior to dielectric deposition the wafers were cleaned

by standard RCA cleaning process. After each standard clean (SC) process, native oxide is etched by 2% HF dip for 30 sec followed by a thorough de-ionized (DI) water rins. Wafers were subsequently dried in N_2 gas. The process chamber was pumped down to a base pressure of 7×10^{-8} torr before dielectric deposition. The deposition process was characterized by measuring hysteresis in the cathode voltage versus O_2 flow while Ar flow was kept constant at 15 sccm (standard cubic centimetre). Hysteresis measurement was carried out for different process power.Thickness and refractive index (RI) of the film was measured by Spectrocopic Ellipsometer. Stoichiometry of the film was characterized by XPS measurement for different O_2 flow with Ar flow at 10sccm and process power at 500 W. MOS capacitors were fabricated with aluminum as top gate and also for backside contact. MOS capacitors were subjected to forming gas annealing (FGA) at $420°C$ for 20 min. For all Al_xO_y depositions certain parameters including power supply variables were chosen as follows: pulse frequency at 100 kHz, reverse time (T_{rev}) at 3 μsec, duty cycle at 70% and deposition time at 300 seconds.

2.2 Results and Discussion

2.2.1 Hysteresis Behaviour

The hysteresis behaviour is observed in cathode voltage of the sputter system as the O_2 flow is varied from the minimum to a certain high value and subsequently retracing the flow to low values. This effect is observed because for low O_2 flow the target surface remains metallic as the reactive species concentration is low. However as the O_2 flow is increased the target surface starts reacting with O_2 and an oxide layer is formed on the surface. This oxide layer is charged by electrons from the plasma which causes a sudden drop in cathode voltage. During the retrace of the O_2 flow we have observed that the cathode voltage remains low until no oxide remains on the target surface at which point the target voltage rises to its initial value [8–11]. The critical flow for the retrace is lower than that in the forward direction, resulting in a hysteresis as shown in Fig 2.2 for different process power. It is observed that the value of O_2 flow at which a sudden drop in cathode voltage appears (i.e. knee point) is different for different process power. It is important to do the process in low cathode voltage of the hysteresis curve to obtain dielectric deposition on the wafer.

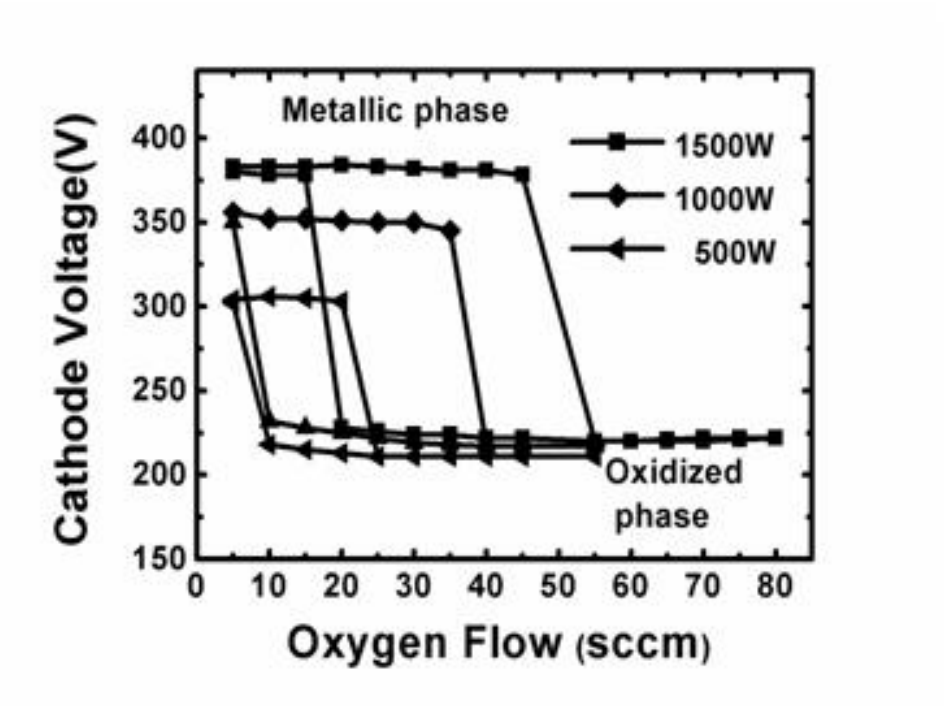

Figure 2.2: Hysteresis behaviour observed in cathode voltage of sputter system as a function of O_2 flow for different process power

2.2.2 Stoichiometry of the Deposited Film

A thermo VG scientific make multilab 2000 x-ray photoelectron spectrometer used for the stoichiometry measurement of the deposited Al_xO_y with Mg Kα radiation source (photon energy E = 1253.6 eV) as an excitation source. The stoichiometry of the Al_xO_y film is observed for different gas flow ratio i.e. Ar:O_2 of 1:2.5 and 1.3. Using surface analysis the Al 2p spectra and O 1s spectra is generated, as shown in Fig 2.3 (a) and (b) respectively. A stoichiometric Al_2O_3 film was obtained at O_2 flow slightly above knee point in forward direction of the hysteresis curve i.e. at O_2 flow of 25 sccm for 500W, while the film become O rich for higher O_2 flow. Ar flow was maintained constant at 10 sccm for these depositions.

2.2.3 Deposition Rate and Optical Property

The thickness and refractive index (RI) of the film is measured with Sentech spectroscopic ellipsometry (SE-800) followed by curve fitting using SpectraRay. Fig 2.4 shows the deposition rate and RI obtained for different O_2 flow with Ar flow held constant at 15 sccm while the process power was 500W. The deposition rate is decreasing with increasing O_2 flow, due an increase in process pressure which causes a decrease in mean free path and hence the sputtering

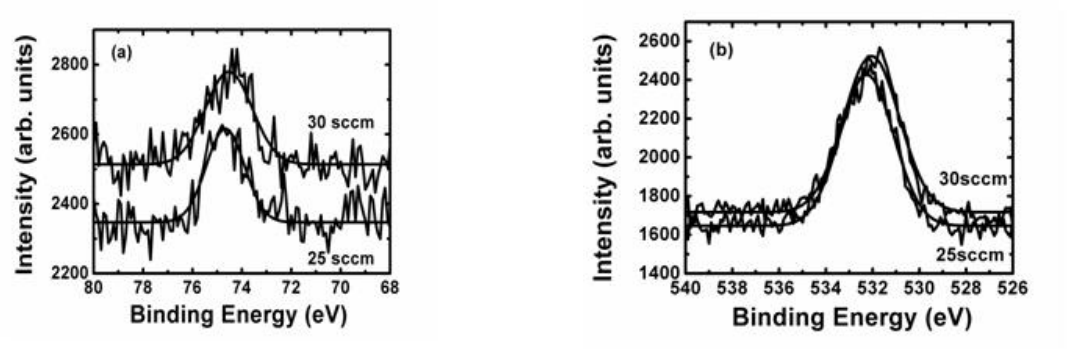

Figure 2.3: XPS specta of Al_xO_y films deposited on Si wafer for two different O_2 flow while Ar flow was kept constant at 10 sccm (a) Al 2p spectra (b) O 1s spectra. Films were deposited at a process power of 500 W

rate. Also for the oxidized target a secondary electron emission coefficient is higher which leads to less sputtering of metal [10] and lower reaction at the target surface [9]. The RI $\sim$ 1.478 is observed for gas flow ratio of Ar:O_2 1:2.5 which is the stoichiometric Al_2O_3 film, whereas the value of RI goes down a little for higher O_2 flow i.e. for O rich films.

2.2.4 Electrical Characterization

High frequency C-V and I-V measurements of MOS capacitors were carried out using Keithley 4200 semiconductor characterization system. MOS capacitors were fabricated with the optimized Ar: O_2 flow ratio of 1:2.5 i.e. a stoichiometric Al_2O_3 dielectric film with low roughness. Fig 2.5 shows the normalised C/C_{max} versus gate voltage curve measured at a frequency of 100kHz. A SiO_2 equivalent oxide thickness (EOT) of $\sim$ 8.59 nm with a dielectric constant (k) of 8.15 is extracted from this curve. Fig 2.6 shows the Weibull distribution of effective breakdown field, a mean effective breakdown field (EBD) of 18.07MV/cm is obtained for the optimized deposition recipe. The EBD obtained by our optimized process is comparable to values reported for films deposited by CVD-Al_2O_3 films [12] as shown in Table 2.1.

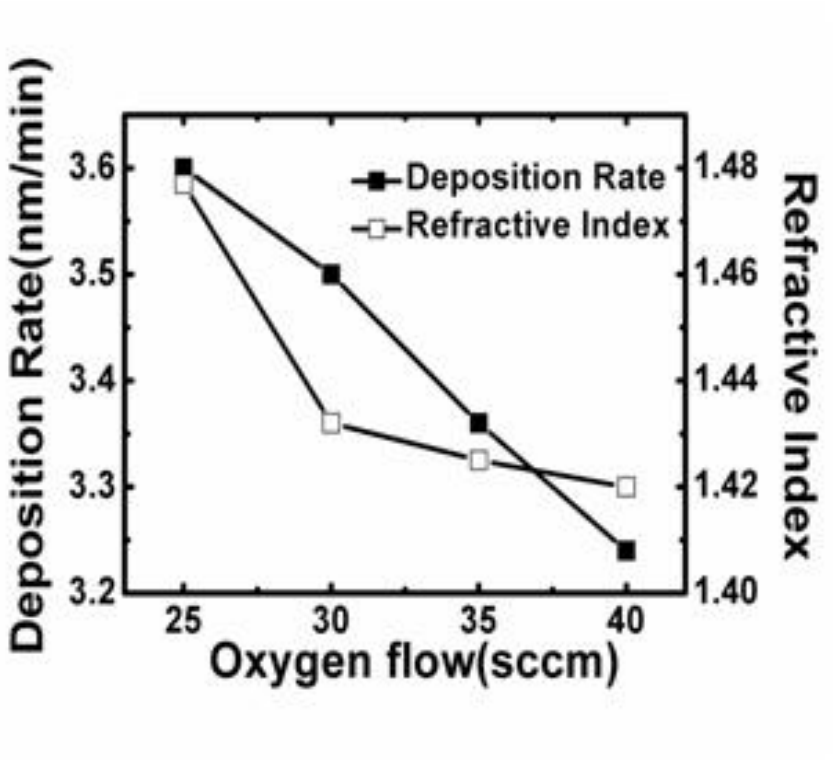

Figure 2.4: Deposition rate and refractive index of Al_xO_y film for different O_2flow, it is observed that a deposition rate as well as RI is going down with O_2 flow

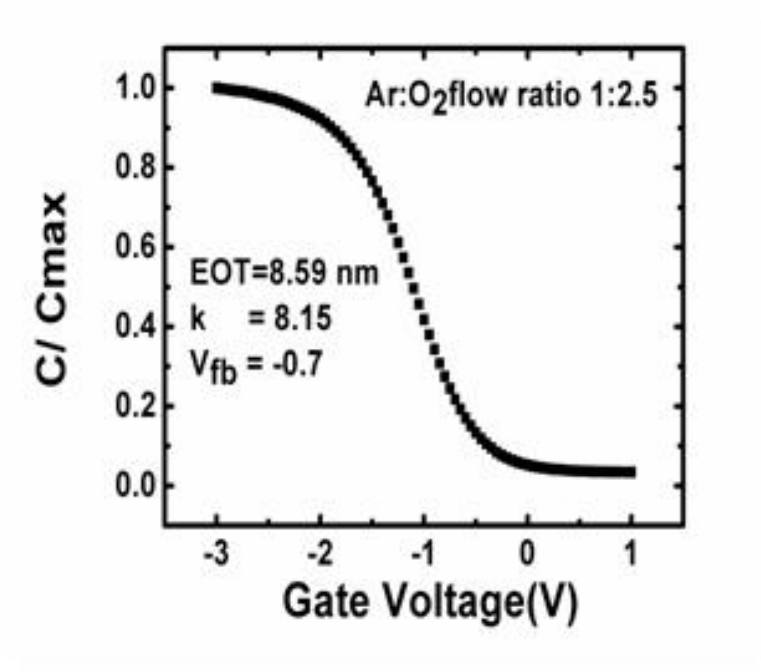

Figure 2.5: High frequency normalised C/C_{max} versus gate voltage plot of Al_2O_3 MOS capacitor with Al_2O_3 deposited with gas flow ratio of Ar:O_2 at 1:2.5 and oxide thickness of 17.97 nm

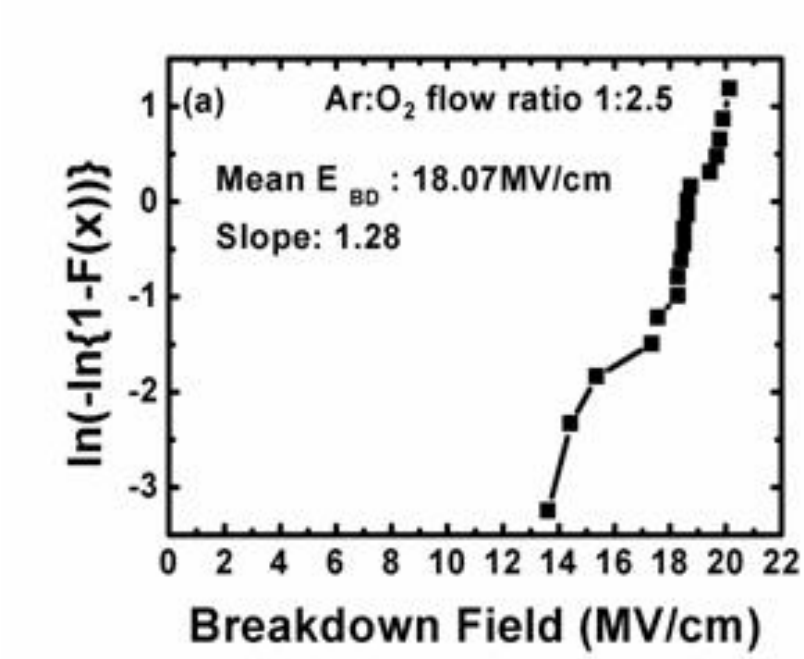

Figure 2.6: Weibull distribution plot of breakdown field for Al_2O_3 capacitor with Al_2O_3 deposited with gas flow ratio of Ar:O_2 at 1:2.5 and oxide thickness of 17.97 nm. E_{BD} refers to the effective breakdown field

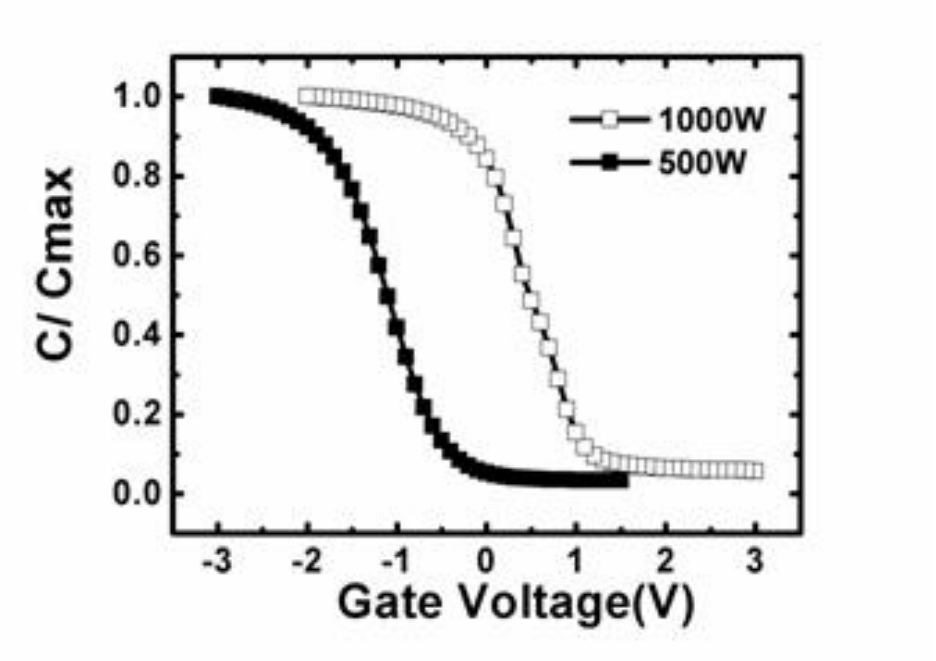

Figure 2.7: High frequency normalised C/C_{max} versus gate voltage plot of Al_xO_y MOS capacitor with Al_xO_y deposited at 500W and 1000W

High frequency C-V of capacitors with Al_xO_y films deposited at 1000W and comparison with the optimized recipe are shown in Fig 2.7. A positive shift in flat band voltage (V_{FB}) is observed for film deposited at higher power. The values of effective oxide thickness (EOT),

Power (W)	**EOT (nm)**	**k**	$\mathbf{V_{FB}}$ **(V)**	$\mathbf{N_{ox}}$ $(\mathbf{cm^{-2}})$
500	8.59	8.15	-0.7	-3.5×10^{11}
1000	12.44	8.93	0.8	-2.88×10^{12}

Table 2.1: Effective oxide thickness (EOT), dielectric constant (k), flatband voltage (V_{FB}) and fixed oxide charge density (N_{ox}) extracted data from HFCV measurement for Al_xO_y deposited for two different process powers

Deposition Method	**EOT (nm)**	$\mathbf{E_{BD}}$ **(MV/cm)**
MOCVD	5.5	19.3
RF Reactive Sputtering	6.3	14.1
Reactive Sputtering using Pulsed DC-supply	8.59	18.07

Table 2.2: Comparison of the effective breakdown field (E_{BD}) and EOT of pulsed DC reactive sputtered Al_2O_3 with different deposition methods.

dielectric constant (k), flatband voltage (V_{FB}) and oxide charge density extracted results from HFCV are shown in Table 2.2. It shows the film deposited at higher power has more negative oxide charges (Q_{ox}) of $2.88 \times 10^{12} cm^{-2}$ as compared to low power deposited film which has Q_{ox} of $3.5 \times 10^{11} cm^{-2}$.

Chapter 3

SiO_2/Al_2O_3 Dielectric Stack Optimization

For SiO_2/Al_2O_3 stack optimization, Al_2O_3 is deposited by physical vapor deposition technique using pulse DC power supply and Ar as a sputtering gas and O_2 as a reactive gas. In this Al_2O_3 optimization process, the first aim was to find the optimum deposition power and Ar:O_2 flow. For all the experiments reported in this work, Al_2O_3 deposition is done on a thermally grown SiO_2 layer of thickness varying from 3.2-3.5nm. In any sputtering process, plasma induced damage in the underneath dielectric in inevitable, hence the criteria for choosing the power is to study the interface states of Si/SiO_2 interface after Al_2O_3 deposition at different powers. The other two important parameters considered in selecting the optimum deposition power are dielectric constant of the Al_2O_3 film and effective breakdown field of the SiO_2/Al_2O_3 stack. Once power is selected, post dielectric anneal study is carried out to densify the Al_2O_3 film in O_2 ambient. Details of the experiments and results are given in the following sections. *For the data in this chapter I have refered to published paper the details of which are in list of publications at no.2 with contribution from this thesis.*

3.1 Deposition Power Optimization for Al_2O_3 Film

3.1.1 Experimental Details

A good quality (less D_{it}, high breakdown field of 15-16MV/cm) SiO_2 of thickness 3.2 ($\pm$0.3nm) is thermally grown on $4''$ Si wafers after RCA cleaning. Thickness of the as grown SiO_2 is mea-

sured by ellipsometer. Al_2O_3 deposition is done at four different powers ranging from 150W, 200W, 300W and 400W. The gas flow ratio Ar:O_2 was 10:(knee point+5) where knee point as well as target voltage to be maintained to achieve target conditioning as obtained from hysteresis curve [13] shown in Fig 3.1. Thickness and refractive index of as deposited Al_2O_3 is measured by ellipsometer. For top gate electrode, aluminum was evaporated on top of the Al_2O_3 and patterned using optical lithography and reactive ion etching to obtain capacitors with circularly shaped gates having diameter of 80μm. Back side metallization is done to form the back contact.

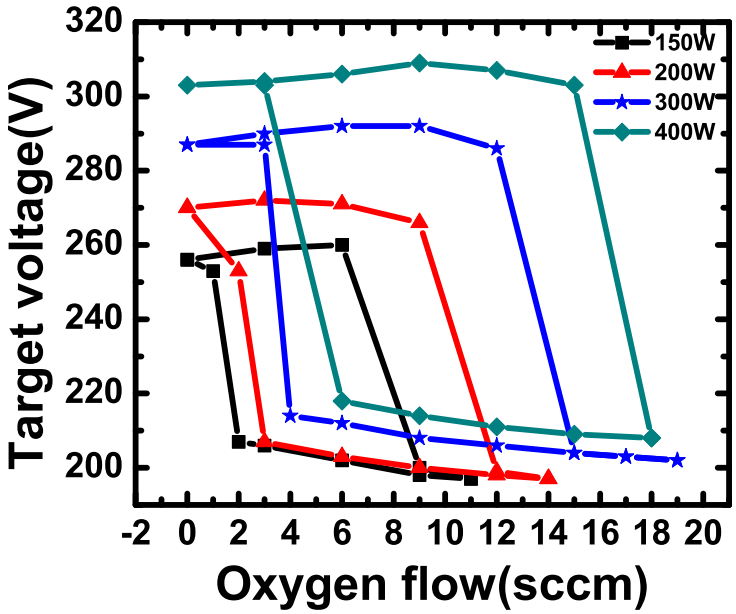

Figure 3.1: Hysteresis behavior of target voltage with oxygen flow for different target powers

3.1.2 Result and Discussion

Variation in deposition rate and refractive index of as deposited Al_2O_3 at different powers is shown in Fig 3.2. As the deposition power increases deposition rate and refractive index increases. With higher deposition rate refractive index reaches towards its ideal value i.e. 1.62, which indicate that at higher powers, with more deposition rate, film reaches to its bulk properties quickly while for low power, since the deposition rate is low, film properties may not be of that bulk Al_2O_3. Hence, to get the bulk like Al_2O_3 properties, longer time deposition should be done at low powers.

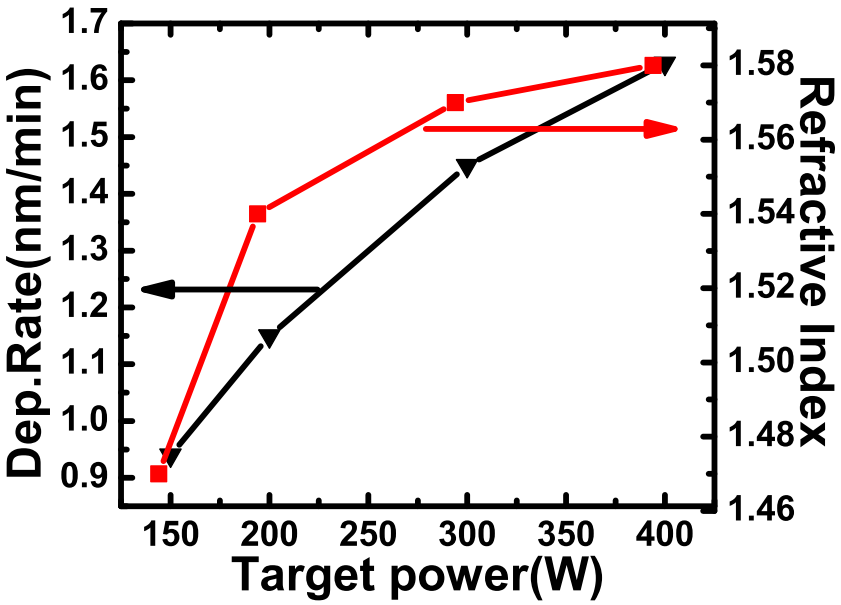

Figure 3.2: Deposition rate and refractive index (RI) vs. deposition power

Normalized capacitance vs. Voltage (C-V) and current density vs. breakdown filed (J-E) curves for the Al_2O_3 deposited at different powers is shown in Fig. 3.3(a) and Fig. 3.3(b) respectively. From the C-V, it is clear that as the deposition power increases, flatband voltage increase from a value of -1V at 150W to 0.43V at 400W, indicating higher oxide charge density incorporated in the film at higher deposition powers. Bulk oxide charges and interface trap density with different deposition powers is shown in Fig. 3.4. High deposition power also causes the increased interface state density. This is directly attributed to the plasma damage caused by higher power during deposition. Different values of flatband voltage, fixed oxide charge and interface state density is tabulated in Table 3.1 of this chapter. Dielectric breakdown of the SiO_2/Al_2O_3 stack is studied by performing the J-E analysis as shown in Fig. 3.3(b). Al_2O_3 deposited at 200W results in the highest breakdown field. This can be explained on the basis of low oxide charges, and low interface damage caused to the SiO_2/Al_2O_3 interface at 200W deposition. From Fig. 3.4, it can be misunderstood that, 150W deposited SiO_2/Al_2O_3 stack has the lowest fixed oxide charges and minimum interface states, however, lowest breakdown field of this stack reveals that Al_2O_3 deposition at 150W is not proper. We have done the Al_2O_3 deposition at 100W (data not shown here) however, we could not get any reasonable value of the Al_2O_3 thickness. This suggests that 100W is too low power to get any good quality Al_2O_3 film. 150W gives some deposition but poor breakdown field indicate that deposition is still not

of good quality. Hence, from C-V, and J-E analysis, we conclude that 200W is the optimum power for depositing good quality Al_2O_3.

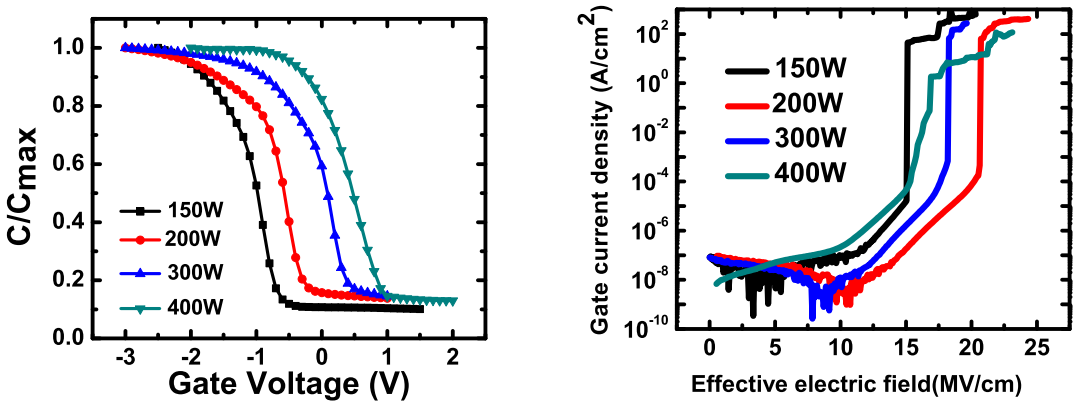

Figure 3.3: (a) Normalized CV curves for different target powers (b)JE plot for different powers. Electric field shown is the effective electric field given by $(V_G - V_{FB})/EOT$

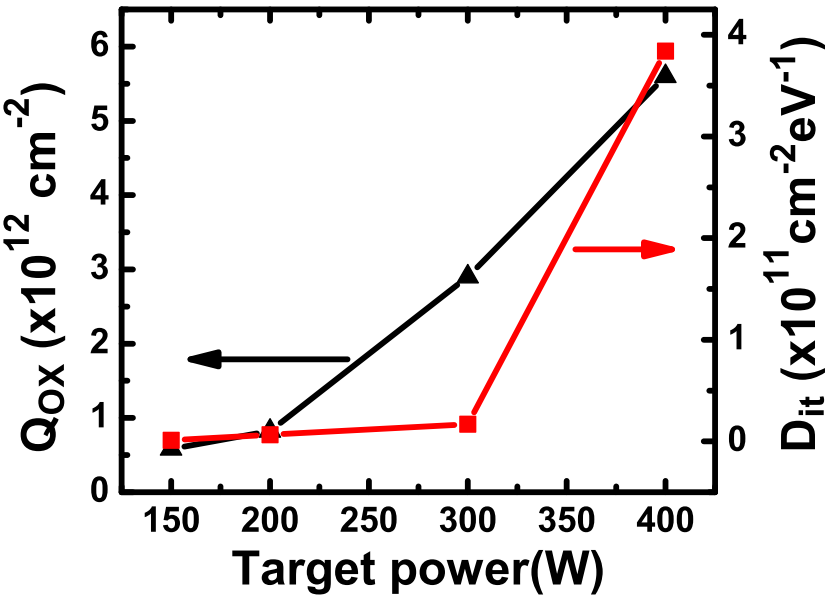

Figure 3.4: Bulk oxide charges and interface trap density as a function of target power

Deposition Power (W)	$\mathbf{V_{FB}}$ **(V)**	$\mathbf{Q_{ox}}$ $(\#/\mathbf{cm^{-2}})$	$\mathbf{D_{it}}$ $(\#/\mathbf{cm^{-2}eV^{-1}})$	$\mathbf{E_{BD}}$ **(MV/cm)**
150	-1	5.81×10^{11}	1.12×10^{11}	14.98
200	-0.64	8.25×10^{11}	6.59×10^{11}	20.55
300	0.07	2.90×10^{12}	1.69×10^{12}	18.11
400	0.43	5.60×10^{12}	3.84×10^{12}	15.31

Table 3.1: Different Electrical parameters of SiO_2/Al_2O_3 stack obtained from C-V and J-E plot: Effect of Power

3.2 Effect of post deposition anneal at different temperatures on the electrical performance of $\mathrm{SiO_2/Al_2O_3}$ stack

3.2.1 Experimental Details

Post dielectric deposition anneal (PDA) is one of the important way to increase the density of as deposited films. Previous experiment suggests that 200W is the optimum power for Al_2O_3 deposition. Hence for studying the effect of different anneal temperatures on the electric performance of SiO_2/Al_2O_3 stack, Al_2O_3 deposition is done at 200W. Like previous experiment, in this experiment also, Al_2O_3 is deposited at 3.2nm SiO_2. Rapid thermal annealing is done at $700°C$, $800°C$ and $900°C$for 15 sec in O_2 ambient in Applied Materials Gate Stack tool.

3.2.2 Result and Discussion

C-V curves of these samples are shown in Fig. 3.5.Change in the dielectric constant and D_{it} with PDA temperature is shown in Fig. 3.6. As the anneal temperature increases D_{it} decreases from a value of $2.57 \times 10^{12} cm^{-2} eV^{-1}$ to a value $2.03 \times 10^{12} cm^{-2} eV^{-1}$ suggesting the improved quality of dielectric interface. With the increasing PDA temperature, stoichiometry of the Al_2O_3 film is also improved as suggested by the increase in the value of K from 6.39 for un-annealed sample to a value of 7.53 for 9000C annealed sample. Improved stoichiometry is also supported by X-ray photon spectroscopy analysis as shown in Fig. 3.7a and 3.7b. For un-annealed sample, ratio of O1s to Al2p peak is 2.1 and decreases to a value of 1.75 for sample annealed at $900°C$. Value 1.75 is close to stoichiometric value of 1.5. However, the maximum value of K i.e. 7.53 is less than the maximum K value of Al_2O_3 reported in the literature [14]. The improvement

in the K value with high temperature anneal signifies the increased densification of the film. The J-E plot and Weibull distribution for these samples are shown in Fig. 3.8 and Fig. 3.9 respectively. Breakdown field of the devices decreases from an average value of 17-18MV/cm for un-annealed sample to an average value of 15-16MV/cm for annealed devices. Maximum breakdown field 16MV/cm is obtained for the devices annealed at $900°C$. This breakdown field is comparable to the breakdown field reported in the literature for the ALD deposited Al_2O_3 on SiO_2 [15]. However, the reduction in the breakdown field, in the present study, with high temperature anneal is contrary to what is reported in literature [15]. Change in different electrical parameters with anneal temperature is tabulated in Table 3.2 of this chapter. High temperature anneal may also induce the change in bandgap of Al_2O_3. There are contradictory reports on this [15] reported the same value of bandgap after exposing the Al_2O_3 to temperatures $900°C$, $1000°C$ and $1100°C$. On the contrary in [16] and [17], improved memory performance of flash memory is attributed to the increased conduction band offset of the crystallized Al_2O_3. In the present study, increased value of dielectric constant, less D_{it} and higher breakdown field for the samples annealed at $900°C$ suggests that $900°C$ is the optimum temperature for the PDA. A systematic study of the effect of higher temperature anneals on the bandgap and crystallization of Al_2O_3 should be further explored.

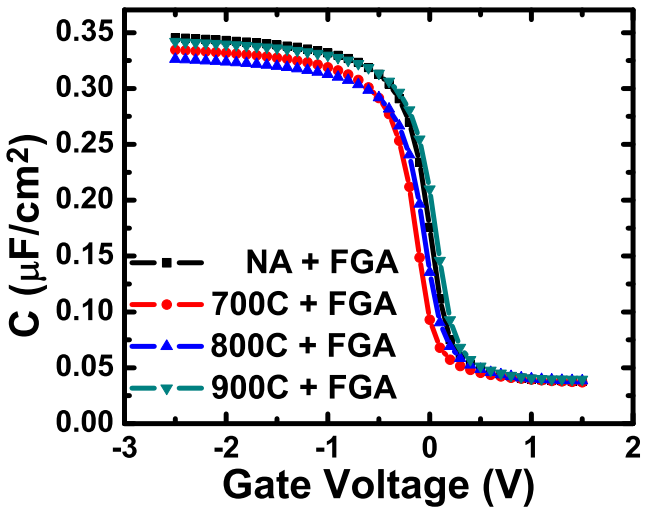

Figure 3.5: C-V curves for the devices annealed at different temperatures

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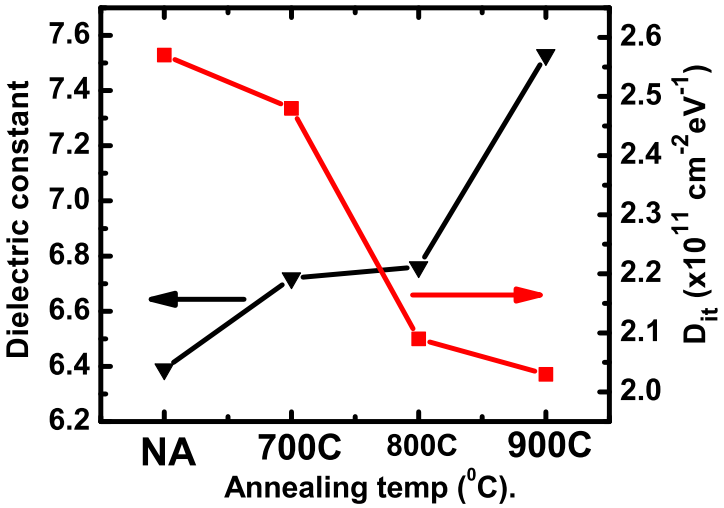

Figure 3.6: Dielectric constant (K) and interface trap density (D_{it}) as a function of annealing temperatures for 200W deposition

Temperature (°C)	V_{FB} (V)	D_{it} ($\#/cm^{-2}eV^{-1}$)	**Dielectric constant**	E_{BD} **(MV/cm)**
Unannealed	0.035	2.57×10^{12}	6.39	17.5
700	-0.09	2.48×10^{12}	6.72	15.5
800	-0.04	2.09×10^{12}	6.76	15
900	0.09	2.03×10^{12}	7.53	16.2

Table 3.2: Different Electrical parameters of SiO_2/Al_2O_3 stack obtained from C-V and J-E plots: Effect of PDA

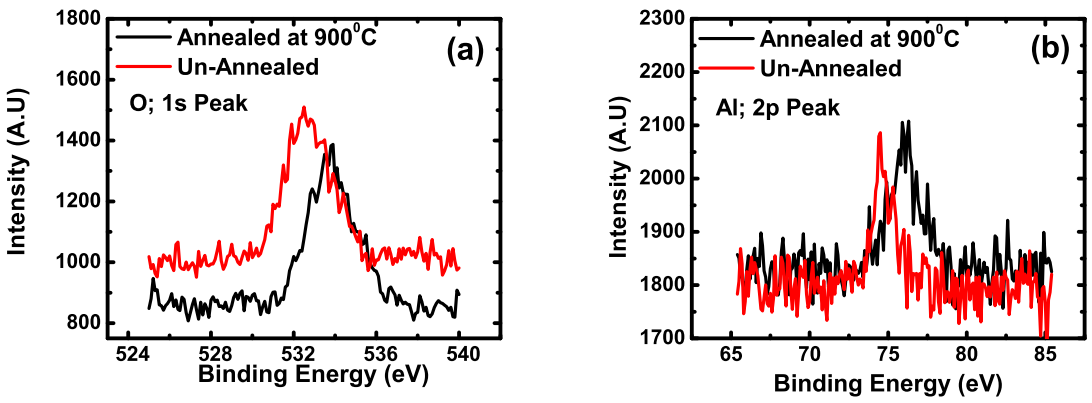

Figure 3.7: Comparison of XPS spectra of Al_2O_3 un-annealed and annealed at $900°C$, (a) O;1s peak (b) Al;2p peak

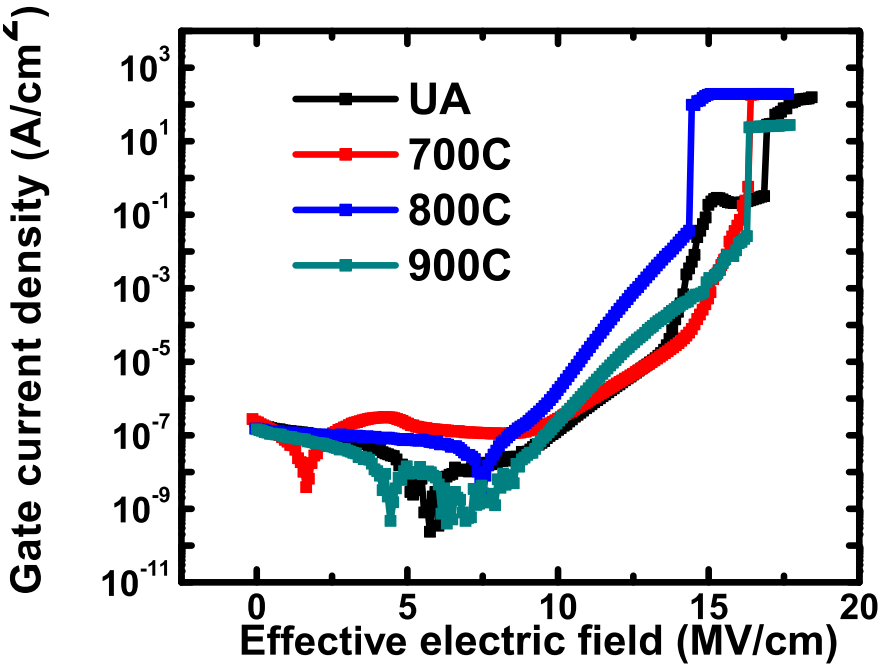

Figure 3.8: J-E plot for different annealed temperatures for 200W deposition

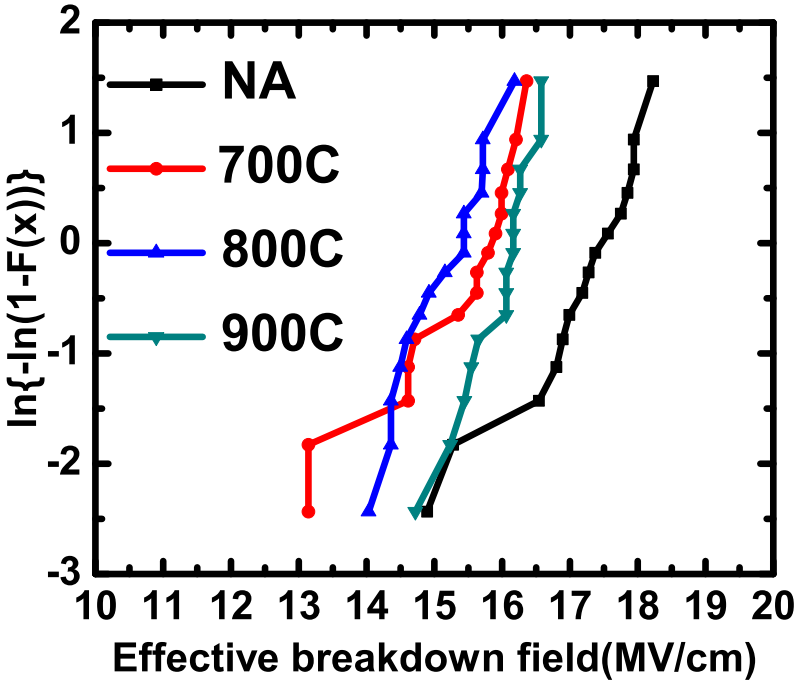

Figure 3.9: Weibull distribution for different annealed temperatures for 200W deposition

Chapter 4

Graphene Floating Gate (FG) Flash Transistor Fabrication and Electrical Characterization

In flash MOS capacitor structure it is observed that erasing is faster as compared to programming, reason being the electrons which are used for programming the flash memory are the minority carriers in the p-type substrate whereas the holes which are used for erasing are the majority carriers. This is the bottleneck in flash MOS capacitor which stops us from getting the large memory window and faster programming. The motivation for fabrication of flash transistor was to get the enhanced memory window at the same programming voltage as MOS capacitor. This will help to increase the fidelity of the information stored in memory device and to achieve faster programming. The work involved establishment of process flow, design of gate mask, electrical characterization and analysis of results for floating gate flash transistor.

4.1 Establishment of Process Flow and Design of Third Level Gate Mask

For detail process flow please refer Appendix A. In the transistor fabrication, source and drain implant is one of the important step involved in process flow. But ion implantation causes damage to the crystal structure of the substrate which is often unwanted. Thus ion implantation step is often followed by a thermal annealing for damage recovery and for dopant activation.

The matter of concern was the thermal annealing step required after implantation if we wanted to use gate self alignment process for implantation. In this step whole memory stack will be undergoing annealing at around $1000^{\circ}C$ as it will affect the blocking dielectric and will degrade the dielectric properties. The top gate as well floating gate might diffuse in the dielectric at such a high temperature. Thus to avoid effect of annealing on the flash memory stack and retaining the flexibility of trying out new materials for blocking dielectric, floating gate and top gate even if they have low thermal budget the gate last process was chosen.

Fabrication of floating gate flash transistor involved three level mask process:

1. First Level-Active area definition
2. Second Level-Dummy gate for source and drain implant
3. Third Level-Actual memory stack patterning

The already available active area mask and the bright field gate area mask were used for defining active area and dummy gate respectively. The design of bright field gate area mask was modified to get the third level mask. The two important considerations while designing the third level mask were

1. The misalignment error while doing the optical lithography for third level for which $1\mu m$ and $0.5\mu m$ extension were kept on both sides of gate finger. Thus $10\mu m$ channel length were modified to $12\mu m$ and $11\mu m$
2. The laser writer was used for writing the mask, the etch process and stripping process used after writing to develop the mask reduces the channel length by $2\mu m$. Thus 1μm extension was introduced on both sides of gate finger.

The gate length of $10\mu m$ was modified to $14\mu m$ and $13\mu m$ in design of bright field gate mask using CADENCE tool. After writing the mask, the optical lithography was done to check whether we get the proper patterns as well the length of the fingers which we were targeting i.e $12\mu m$ and $11\mu m$ for $10\mu m$ fingers.

4.2 Fabrication of Flash Transistor

The p-type $4''$ Si (100) wafers were cleaned by standard RCA cleaning process. High quality SiO_2 is grown on the wafers by thermal oxidation in a horizontal hot wall furnace to obtain

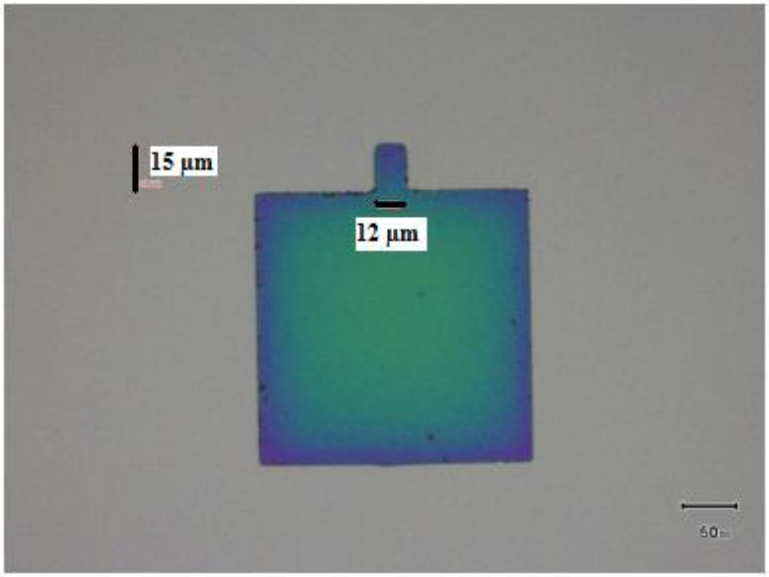

Figure 4.1: The pattern for $10\mu m$ gate finger giving $12\mu m$m due to extensions of $1\mu m$ on both sides.

12nm SiO_2. The silicon nitride is deposited in LPCVD furnace to obtain 60nm thickness. Then optical lithography is performed to define the active area as shown in Fig 4.2 below.

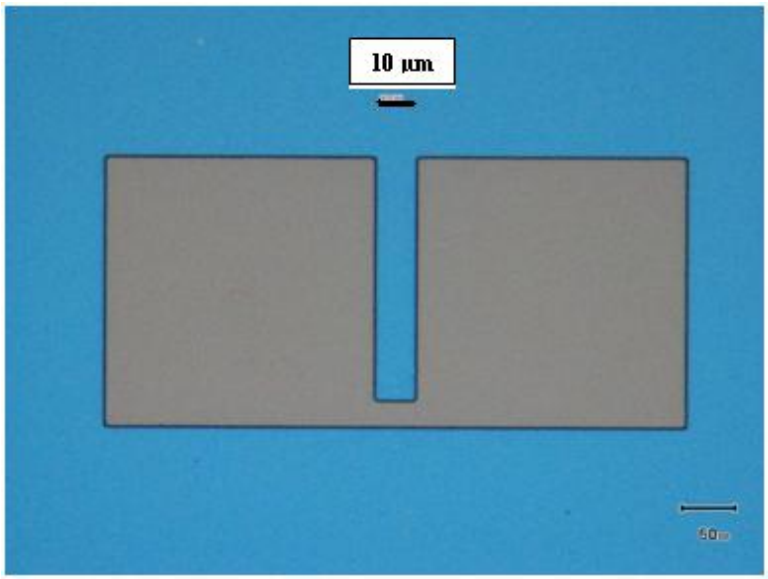

Figure 4.2: Microscopic image of active area after first level optical lithography

The dry etching of nitride is performed in RIE etch system to remove the nitride from the areas other than the active area. The field oxide is grown in pyrogenic oxide furnace to obtain thickness of 315nm. The resist is removed from the active area by ashing and wet etching is performed to remove the nitride from the active area. RCA cleaning is performed on the wafers and then the thermal oxidation is done in a horizontal hot wall furnace to obtain 7.2nm SiO_2.

The dummy gate is defined using optical lithography as shown below in Fig 4.3.

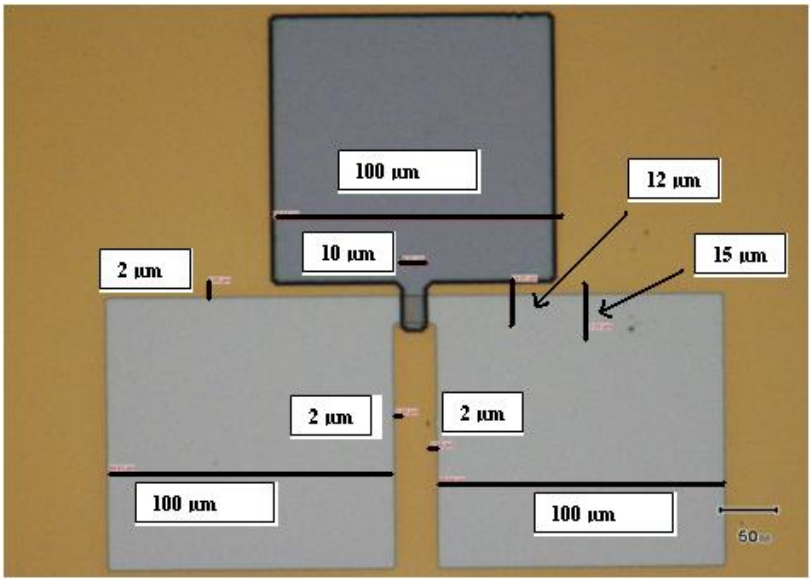

Figure 4.3: Microscopic image of dummy gate defined by second level optical lithography for $10\mu m$ channel length

The source and drain implantation is done using PIII implanter for n-type phosphorous implant. For damage recovery and implant activation, wafers are annealed at $900°C$ for 20 sec in AnnealSys RTP system. Ashing is done to remove the resist after which acetone and IPA dip is given for 5min each to remove the residues of resist, still there were some residues of resist which were removed by piranna cleaning. Before growing the gate oxide 2% HF dip is given to wafers and RCA cleaning is performed. The high quality gate oxide is grown by thermal oxidation in a horizontal hot wall furnace to obtain 5.8nm SiO_2.

The reduced graphene oxide is used as a floating gate for charge storage purpose. The drop casting method is used to make sure graphene is exactly introduced on the active area. The dummy wafer was used which had gate patterns on it and first graphene was introduced on these fingers and then microscopic inspections and SEM was done to make sure graphene is present on the gate fingers. The Fig 4.4 shows the SEM image of the gate finger which shows graphene is present on it. Then after making sure graphene can be drop casted exactly on the gate fingers, the actual wafer was used and graphene was drop casted on it by keeping the wafer on the hot plate at $100°C$.

The AMAT ENDURA tool is used to get PVD deposited Al_2O_3 of 20 nm thickness which is used as the blocking dielectric. The TiN which is used as the top gate is deposited by using AMAT ENDURA tool to obtain thickness of 120 nm. SEM was done to find the thickness of

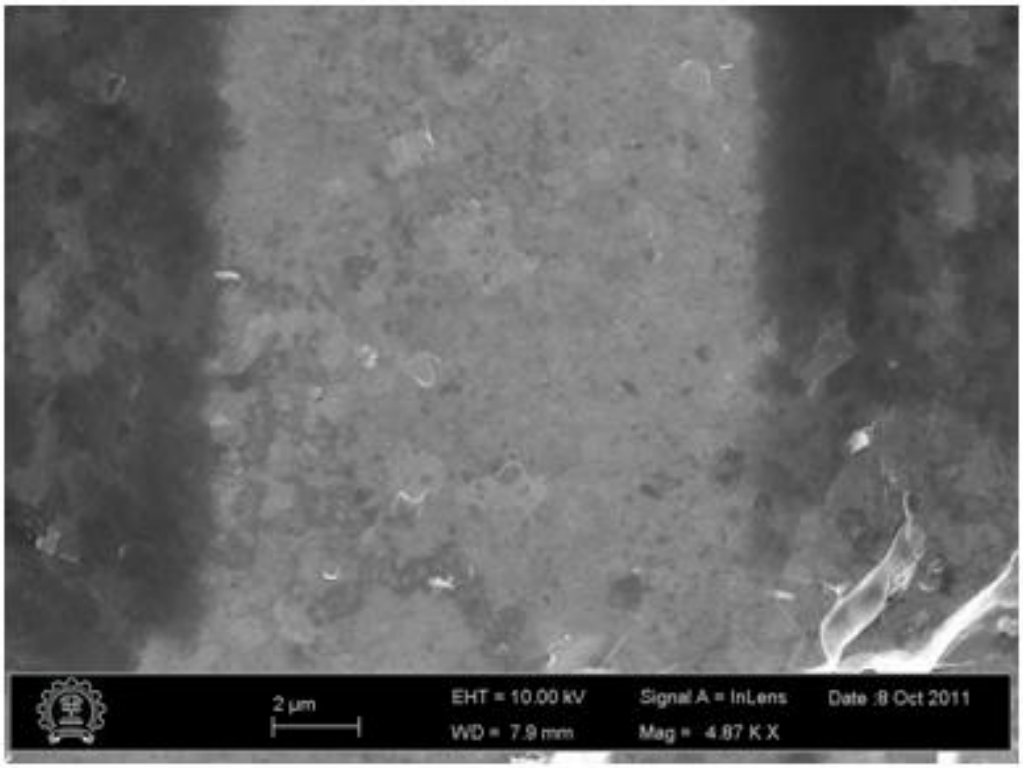

Figure 4.4: SEM image of gate finger showing the presence of graphene on it

TiN. Finally the third level optical lithography is performed to pattern the final gate stack for which the laser writer bright field mask was used. In first run of DSA, there was misalignment so was not able to get the device due to gate finger shorting with the source and drain as shown in Fig 4.5 below. The resist was stripped off using acetone and IPA to perform second run of DSA in order to pattern the top gate using third level optical lithography. After this microscopic inspections were done on each die and mapped the position of all devices which were aligned properly and it was found that yield of around 5% was achieved for the channel lengths of $10\mu m$, $5\mu m$, $3\mu m$, $2\mu m$ and $1\mu m$. The Fig 4.6 shows the $10\mu m$ device after third level of lithography.

After the third level lithography, etching was done of the flash memory stack in the sequence TiN, Al_2O_3 and then finally ashing was performed to remove the resist as well as graphene, all the processing was done in AMAT ETCH CENTURA tool. Acetone and IPA dip was given and then finally backside etching was done.

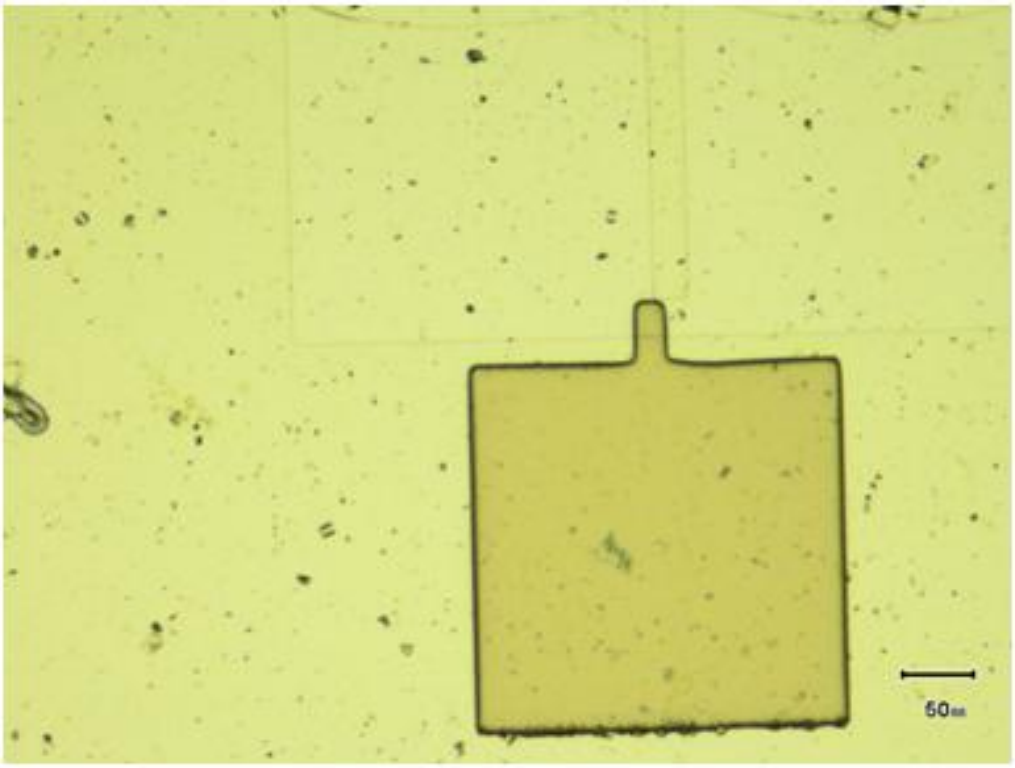

Figure 4.5: Microscopic image after third level optical lithography showing short of gate fingers with the source and drain

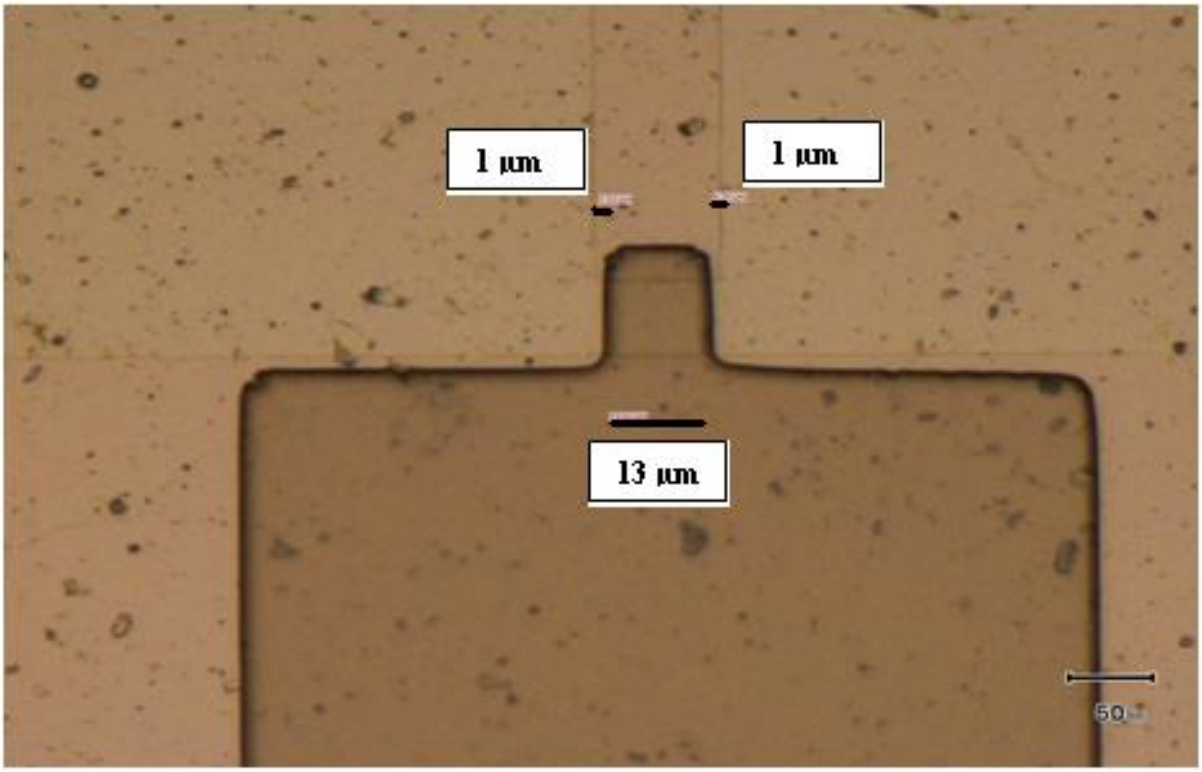

Figure 4.6: Microscopic image of $10\mu m$ device after third level optical lithography

4.3 Electrical Characterization of Flash Transistor

4.3.1 Source and Drain Diode Characteristics

To check whether source and drain implant has been activated, both source and drain n-p junctions where tested for diode I-V characteristics as shown in Fig 4.7 and Fig 4.8, thus confirming that source and drain implant has been activated.

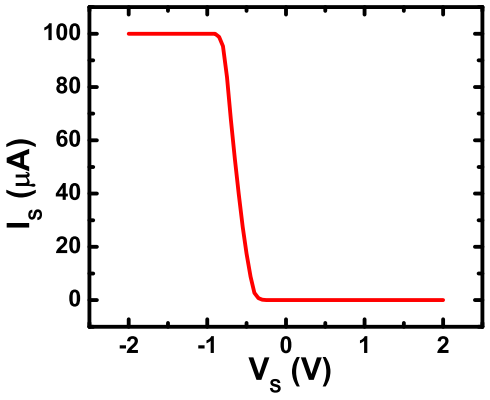

Figure 4.7: Diode characteristics for source n-p junction

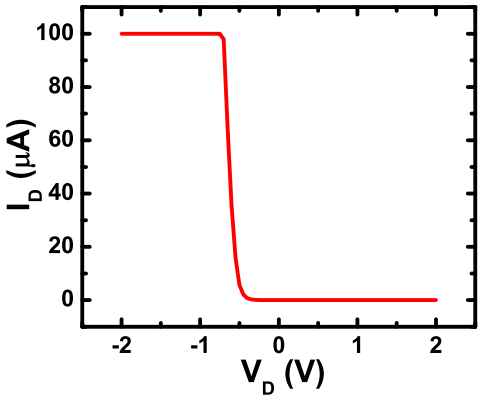

Figure 4.8: Diode characteristics for drain n-p junction

4.3.2 $I_D - V_{GS}$ Characteristics

The Fig 4.9 and Fig 4.10 below shows the $I_D - V_{GS}$ characteristics for the $10\mu m$ channel length transistor. The threshold voltage for the $10\mu m$ floating gate transistor is V_T = 7.1V from Fig 4.10. The trend of $I_D - V_{GS}$ for floating gate transistor is same as the conventional transistor also the maximum I_D increases with increasing the drain bias as shown in Fig 4.9. The Fig 4.11 and Fig 4.12 below shows the $I_D - V_{GS}$ characteristics for the $5\mu m$ channel length transistor. The threshold voltage for the $5\mu m$ floating gate transistor is V_T = 3.52V from Fig 4.12. The Fig 4.13 and Fig 4.14 below shows the $I_D - V_{GS}$ characteristics for the $3\mu m$ channel length transistor. The threshold voltage for the $3\mu m$ floating gate transistor is V_T = 3.10V from Fig 4.14. The Fig 4.15 and Fig 4.16 below shows the $I_D - V_{GS}$ characteristics for the $2\mu m$ channel length transistor. The threshold voltage for the $2\mu m$ floating gate transistor is V_T = 2.04V from Fig 4.16. Thus there is decrease in threshold voltage of floating gate flash transistor with channel length on the other hand I_D increases for the same drain bias and same V_{GS} as channel length increases

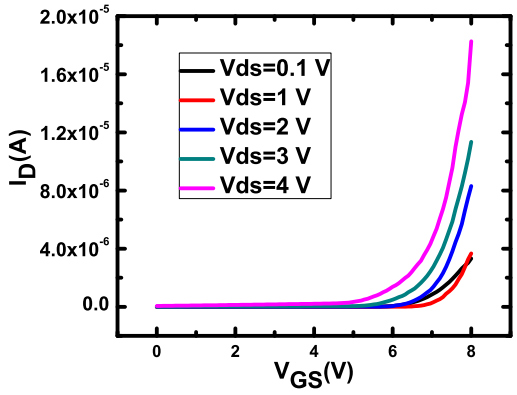

Figure 4.9: $I_D - V_{GS}$ curve for $10\mu m$ channel length (Linear scale)

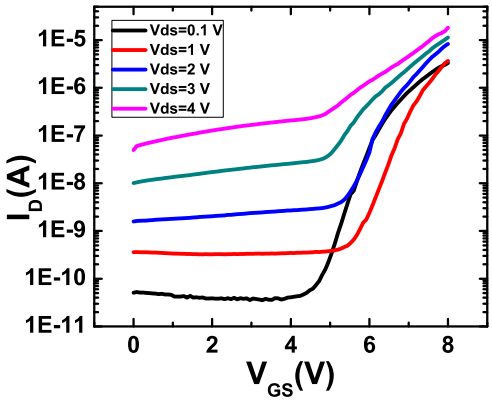

Figure 4.10: $I_D - V_{GS}$ curve for $10\mu m$ channel length (Log scale)

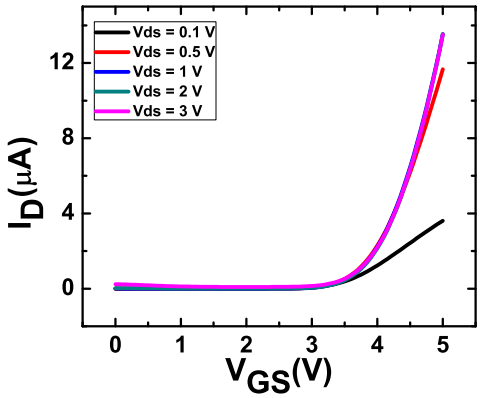

Figure 4.11: $I_D - V_{GS}$ curve for $5\mu m$ channel length (Linear scale)

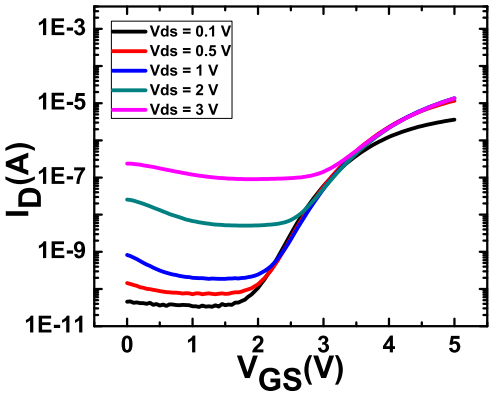

Figure 4.12: $I_D - V_{GS}$ curve for $5\mu m$ channel length (Log scale)

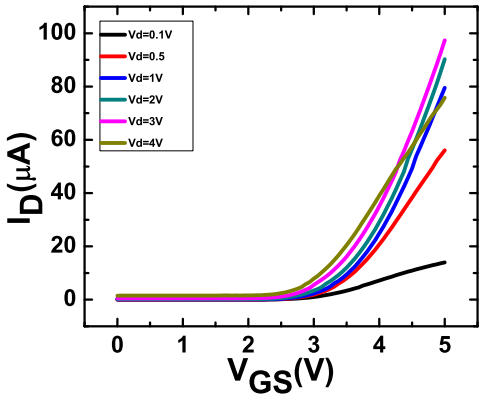

Figure 4.13: $I_D - V_{GS}$ curve for $3\mu m$ channel length (Linear scale)

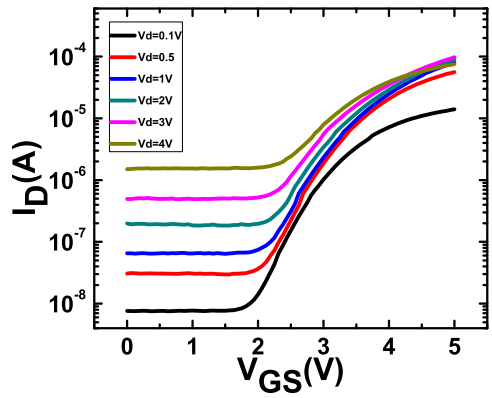

Figure 4.14: $I_D - V_{GS}$ curve for $3\mu m$ channel length (Log scale)

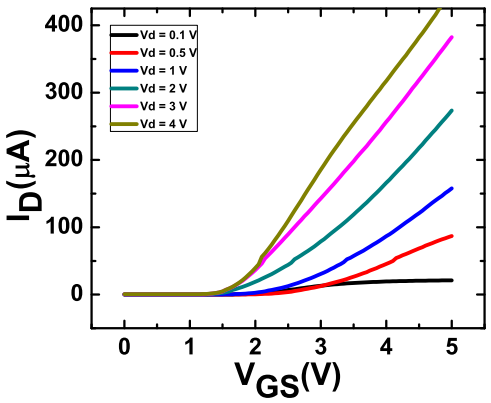

Figure 4.15: $I_D - V_{GS}$ curve for $2\mu m$ channel length (Linear scale)

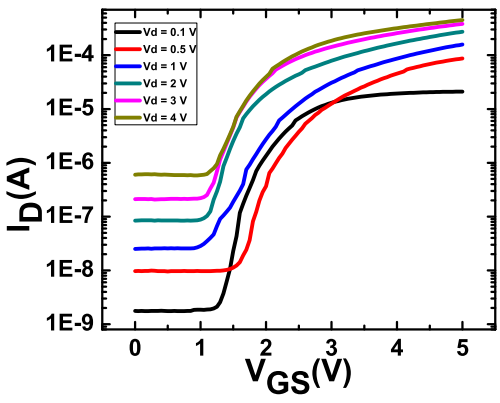

Figure 4.16: $I_D - V_{GS}$ curve for $2\mu m$ channel length (Log scale)

4.3.3 $I_D - V_{DS}$ Characteristics

The $I_D - V_{DS}$ characteristics were measured for different channel lengths of $10\mu m$, $5\mu m$, $3\mu m$, $2\mu m$ as shown below in Fig 4.17,4.19,4.21,4.23 (linear scale) and Fig 4.18,4.20,4.22,4.24 (log scale) respectively by sweeping the V_{DS} from 0 to 4V for constant V_{GS} value ranging from 1 to 8V. It is observed in all the $I_D - V_{DS}$ curves for all the channel lengths that there is significant increase in drain current at V_{GS}=8V more than 100 times compared to V_{GS}=3V the reason being at V_{GS}=8V the gate overdrive (V_{GS}-V_T) is larger. The Fig 4.21 for $3\mu m$ channel length floating gate transistor shows that the capacitive coupling between the drain and the FG modifies the $I_D - V_{DS}$ characteristics of FG MOS transistors with respect to conventional MOS transistors [18, 19]:

1. The FG transistor can go into depletion mode operation and can conduct current even when $V_{GS} < V_T$. This is because the channel can be turned on by the drain voltage this effect is usually referred to as "drain turn-on". As can be seen from Fig 4.21 below for $3\mu m$ channel length with V_T=3.10V even when $V_{GS} < V_T$ there is some drain current flowing due to drain turn on effect.

2. The saturation region for the conventional MOS transistor is where I_D is essentially independent of the drain voltage. This is no longer true for the floating gate transistor in which the drain current will continue to rise as the drain voltage increases and saturation will never occur as seen in Fig 4.21 below for $3\mu m$ channel length.

3. At higher values of drain bias there is sudden dip in the I_D, the reason for which is

the hot electron (HE) injection effect for higher values of Vd. The Fig 4.21 below for $3\mu m$ channel length shows the sudden dip in $I_D$at V_{DS}=3.5V due to HE injection. This is confirmed by looking at Fig 4.25 which shows the increase in gate current (I_G) for $3\mu m$ channel length due to addition of electrons in I_G which are generated due to Impact Ionization (II) in drain depletion region. The secondary holes generated due to II are collected at bulk thus increasing I_B at V_{DS}=3.5V for $3\mu m$ channel length as shown in Fig.4.26.

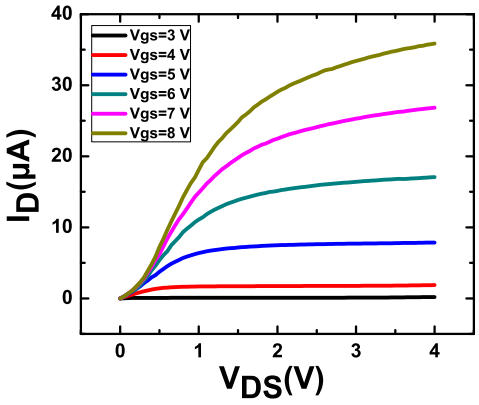

Figure 4.17: $I_D - V_{DS}$ curve for $10\mu m$ channel length (Linear scale)

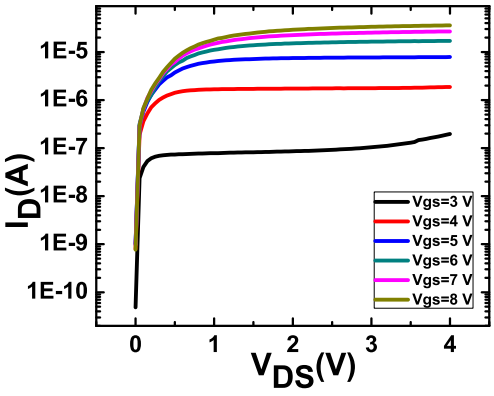

Figure 4.18: $I_D - V_{DS}$ curve for $10\mu m$ channel length (Log scale)

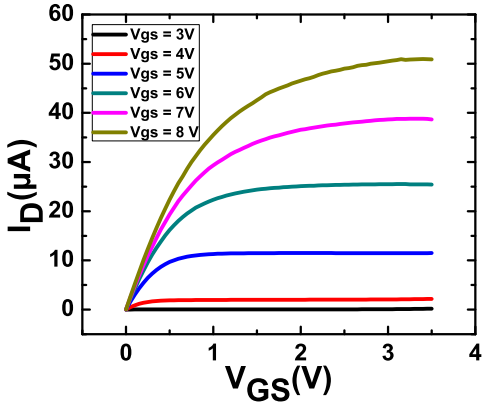

Figure 4.19: $I_D - V_{DS}$ curve for $5\mu m$ channel length (Linear scale)

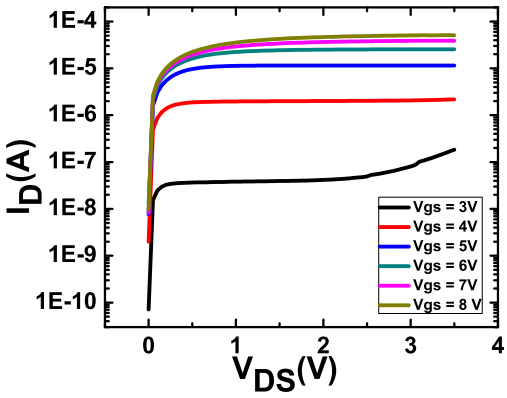

Figure 4.20: $I_D - V_{DS}$ curve for $5\mu m$ channel length (Log scale)

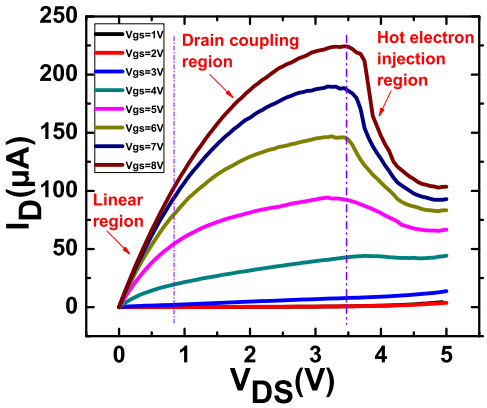

Figure 4.21: $I_D - V_{DS}$ curve for $3\mu m$ channel length (Linear scale)

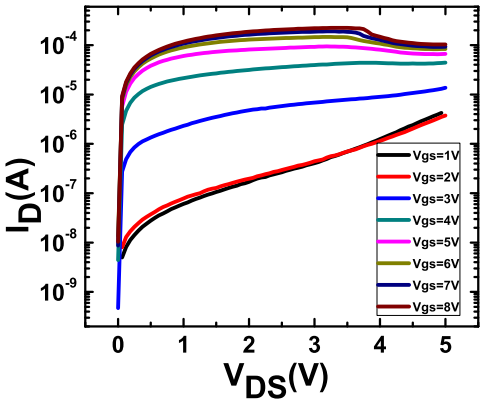

Figure 4.22: $I_D - V_{DS}$ curve for $3\mu m$ channel length (Log scale)

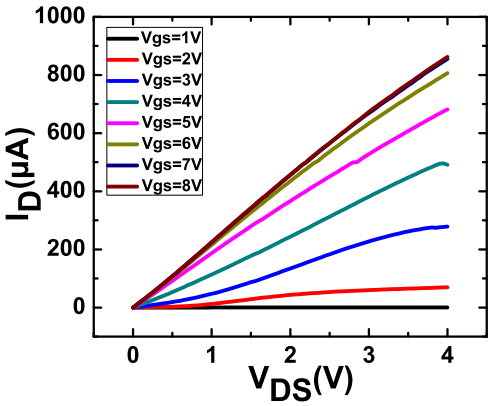

Figure 4.23: $I_D - V_{DS}$ curve for $2\mu m$ channel length (Linear scale)

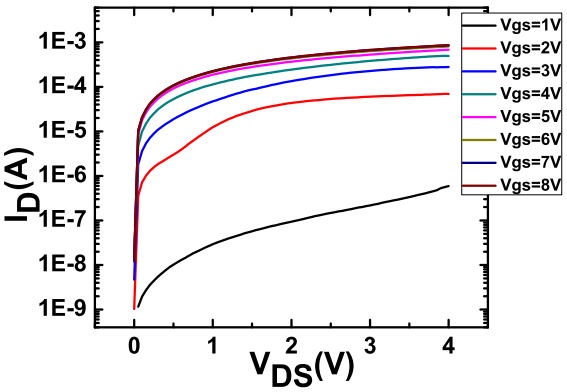

Figure 4.24: $I_D - V_{DS}$ curve for $2\mu m$ channel length (Log scale)

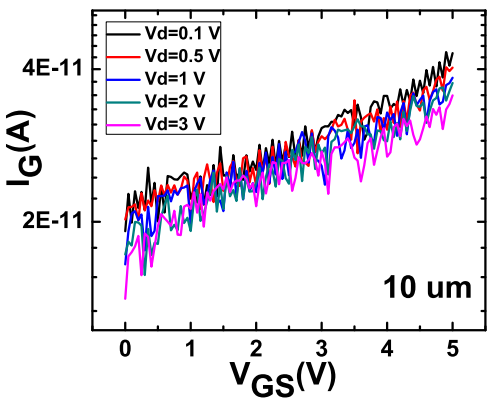

Figure 4.25: $I_G - V_{GS}$ curve for $3\mu m$ channel length (Linear scale)

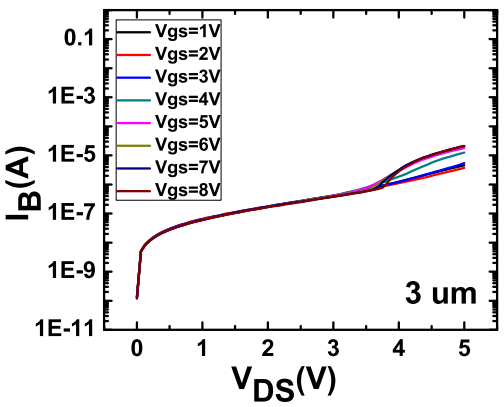

Figure 4.26: $I_B - V_{GS}$ curve for $3\mu m$ channel length (Log scale)

4.3.4 Comparison of Source and Drain Currents

The Fig 4.27, 4.28, 4.29 and 4.30 below shows the comparison between I_S and I_D for $10\mu m$, $5\mu m$, $3\mu m$, $2\mu m$ respectively. The I_S is less by 1 or 2 orders than I_D for $V_{GS} < V_T$ for all the channel lengths which shows that I_S is less influenced by the leakage current as compared to drain. For $V_{GS} > V_T$ both I_S and I_D are same as expected due to formation of inversion layer. For $3\mu m$ channel length I_S is least influenced by the leakage as it is less by almost 3 orders than the drain current as shown in the Fig 4.29 for $V_{GS} < V_T$. Whereas for other channel lengths the difference is less between I_S and I_D. The $5\mu m$ channel length has almost same effect of leakage on I_S and I_D as can be seen from the Fig 4.28 below. These curves also help us to calculate the V_T for all the channel lengths, where V_T is the value of V_{GS} from where both I_S and I_D are same.

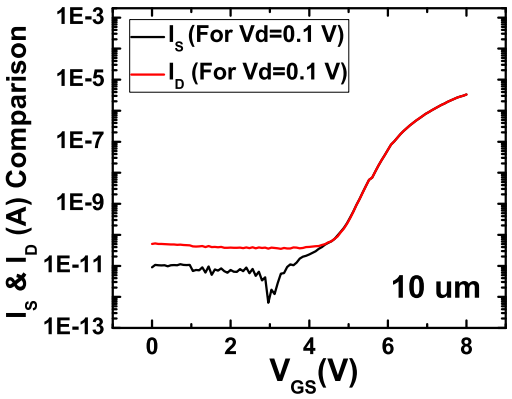

Figure 4.27: Comparison of I_S & I_D for $10\mu m$

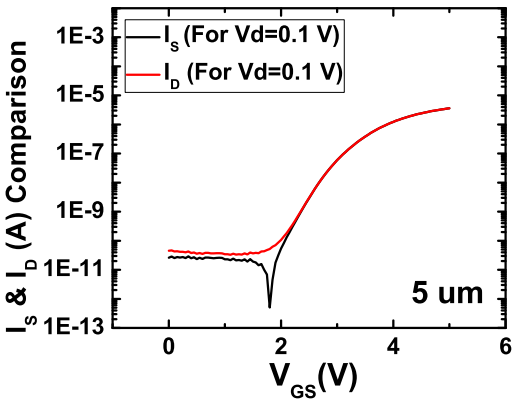

Figure 4.28: Comparison of I_S & I_D for $5\mu m$

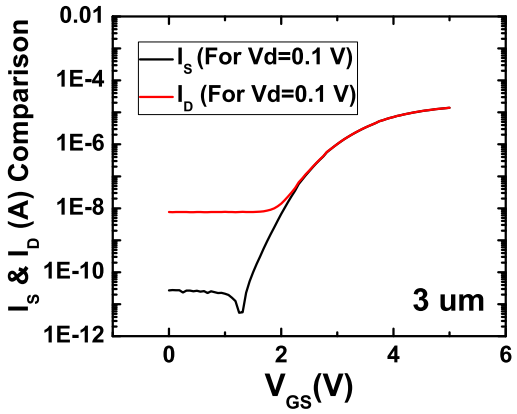

Figure 4.29: Comparison of I_S & I_D for $3\mu m$

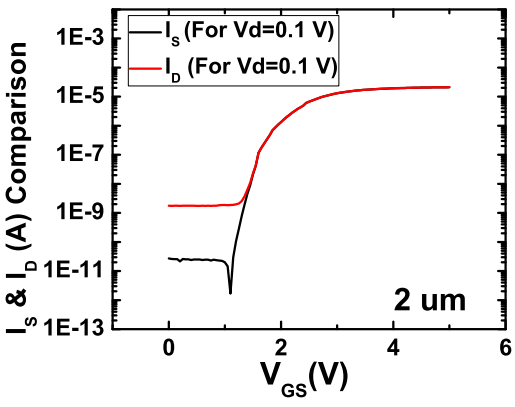

Figure 4.30: Comparison of I_S & I_D for $2\mu m$

4.3.5 Calculation of I_{ON}/I_{OFF} Ratio

The Table 4.1 below shows the comparison between the I_{ON}/I_{OFF} ratio for different channel lengths. The I_{ON} current is calculated from $I_D - V_{DS}$ curve for each channel length at V_{DS}=4V and gate over drive voltage of 1V satisfying the condition for saturation $V_{DS} > VGS - V_T$ for all the channel lengths. The I_{OFF} current is calculated for all the channel lengths such that $V_{GS} < V_T$ i.e transistor is in off state.

Channel Length (μm)	**Threshold Voltage (V)**	**I_{ON} (μA)**	**I_{OFF} (nA)**	**I_{ON}/I_{OFF} ($\times 10^5$)**
10	7.1	36	0.0352	102
5	3.52	11.36	0.0336	33.8
3	3.10	40	7.6	5.26
2	2.04	22	1.76	129

Table 4.1: Comparison between the I_{ON}/I_{OFF} ratio for different channel lengths

Thus I_{ON}/I_{OFF} ratio is around 4 orders which is expected for all the channel lengths.

4.4 Program/Erase (P/E) Characteristics of Graphene Floating Gate Flash Transistor

4.4.1 P/E Characteristics of 5μm Channel Length Device at $\pm$10V

The 5μm channel length device was programmed at 10V for 1μsec, 10μsec, 100μsec, 1msec, 10msec, 100msec time array and some programming was observed but while erasing the device programming effect was observed as shown in Fig 4.31. The program window of around 2.06V was observed for the above mentioned time array as shown in Fig 4.32.

4.4.2 P/E Characteristics of 3μm Channel Length Device at $\pm$14V

The $3\mu m$ channel length device showed good programming as well as some erase though complete erase was not seen but no programing effect was observed during erasing. The Fig 4.33 below shows the program and erase curves for the same time array mentioned for $5\mu m$ device.

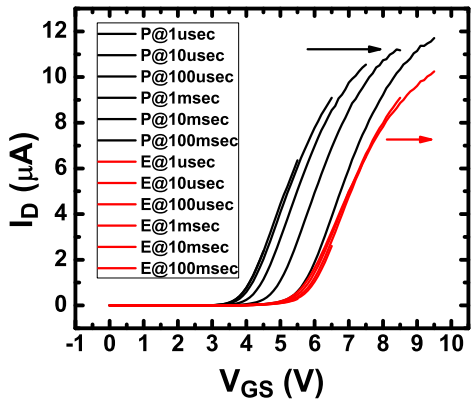

Figure 4.31: Program and Erase curves

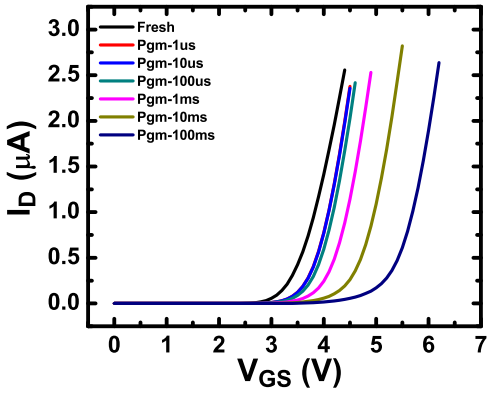

Figure 4.32: $I_D - V_G$ curves after programming the device for different times

The program window of 3.42V was observed at 14V programming voltage for $3\mu m$ device as shown in Fig 4.34. The Fig 4.35 shows both the program and erase $I_D - V_G$ curves which clearly shows there is no programming effect while erasing the $3\mu m$ device at -14V.

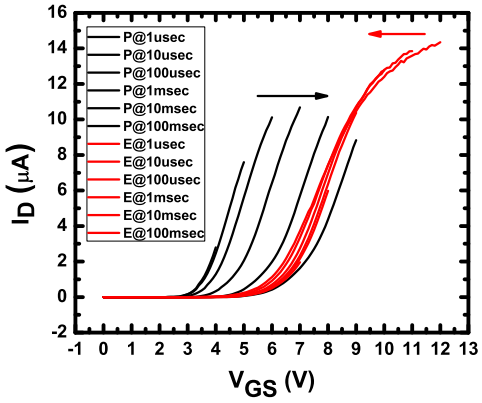

Figure 4.33: Program and Erase curves for $3\mu m$ at $\pm$14V

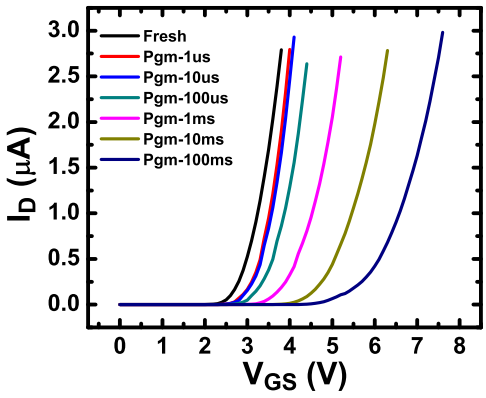

Figure 4.34: $I_D - V_G$ curves after programming the device at $\pm$14V

4.4.3 Problems and Possible Solutions for Graphene FG Flash Transistor

- The programming effect is observed while trying to erase the devices while only slight erase is observed in some devices
- In most of the devices measured the good program window is observed, while erase happens only for $10\mu s$ or $100\mu s$ erase pulse. For longer erase pulse programming effect is observed

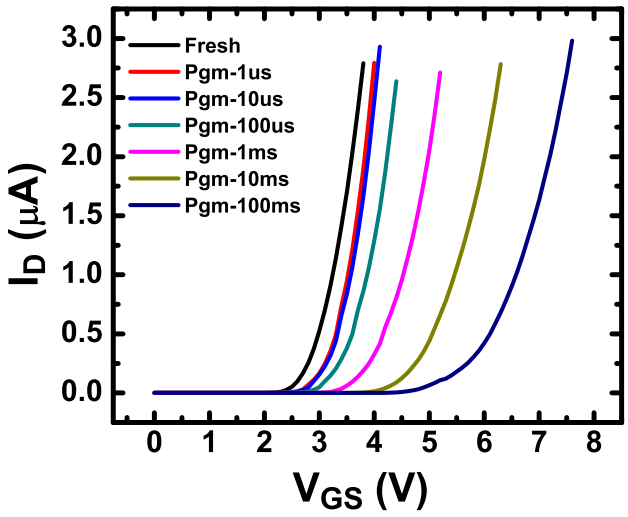

Figure 4.35: $I_D - V_G$ curves for P/E for $3\mu m$ at $\pm$14V

- Injection of carriers from gate electrode due to its low WF (TiN 4.3-4.5eV) may be one of the reason for undesirable erase curves
- The Pt (20nm)-TiN (80nm) as a gate electrode can be tried as it will increase the control gate work function thus reducing the probability of injection of carriers from gate electrode
- The physical thickness of Al_2O_3 used was about 20nm so it can be increased by 3-4nm more to block the injection from top gate.

Chapter 5

Study of Interaction of Graphene with High-k (Al_2O_3) Dielectric

5.1 Motivation

- Graphene was used as FG in transistor study due to its good memory performance in flash MOS capacitors. Also as Gr is very thin material it can be seen as potential candidate to address the issues faced by scaling for lower technology nodes
- Graphene is embedded between SiO_2 which is used as tunnel oxide and Al_2O_3 which is used as blocking dielectric in flash transistor. Thus understanding of interaction between graphene and dielectrics is very important
- The distance between first layer of graphene and SiO_2 is 0.9nm whereas 0.6nm in case of Al_2O_3 thus interlayer van der waals interaction is 2.25 times stronger on Al_2O_3 than on SiO_2 [20]
- High-k will have higher polarization thus dipole formation will be there at the interface of High-k and Gr which could be one of the possible cause for stronger interaction between Al_2O_3 and Gr as compared to SiO_2 and Gr

5.2 Experimental details

1. $4''$ wafer was RCA cleaned and 20nm Al_2O_3 was deposited at 200W power in AMAT Endura tool.The details of 200W recipe are mentioned in chapter 3

2. Gr was drop casted by keeping wafer on hot plate at $1300°C$ then it was reduced by keeping it in Polygen chamber of AMAT Centura for 1hr at $500°C$ in Ar ambient

3. SEM was done to note down the coordinates to identify the regions with and without graphene on the wafer

4. TiN was deposited on top in AMAT Endura tool and PMMA was spin coated on the sample and circular patterns of TiN dots of $80\mu m$ diameter are patterned at the already noted coordinates by electron beam lithography system (RAITH 150Two)

5.3 Results and Discussion

The areas with and without Gr were identified in microscope and both the MOS capacitors with and without Gr were characterized using Keithley 4200 having inbuilt CV card. The Capacitance-Voltage (C-V) plots of these two devices are shown in Fig 5.1 which shows that C-V of TiN/Gr electrode shifts right as compared to TiN electrode for Al_2O_3 MOS capacitors.

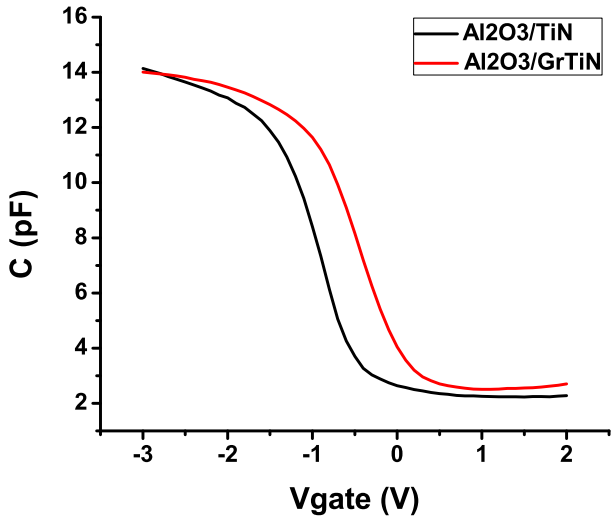

Figure 5.1: Comparison of C-V plots for TiN and TiNGr electrode Al_2O_3 MOS capacitors

The V_{FB} for TiN electrode is -0.98V whereas for TiNGr electrode is -0.51V thus V_{FB} has increased by 0.47V in case of TiNGr electrode there are two possible explanations for increase in V_{FB}.

1. This can be due to increase in work function (WF) of Gr due to increase in number of layers of graphene [21] as here thick Gr has been taken so WF will be higher compared to single or bilayer graphene sheets

2. The Gr gets hole doped when it is deposited on dielectric and there is significant increase in WF of Gr compared to its value in suspended state [21]. The hole doping is strong when the underlying dielectric is high-k [20] in our case we have High-k Al_2O_3 as our dielectric. This could be another reason for increase in V_{FB} in case of TiNGr electrode compared to TiN electrode

Thus in conclusion thick Gr and High-k Al_2O_3 dielectric under the graphene layer could be reason for this shift in V_{FB} in TiNGr electrode.

Chapter 6

Fabrication and Electrical Characterization of Hybrid FG (PtGr) Flash Transistor

6.1 Motivation

- The diffusion of metal used FG into tunnel oxide will be ceased if we take thick Gr under metal . The formation of metal oxide will be avoided due to presence of Gr between SiO_2 which is used as tunnel oxide and metal
- The metal over graphene will result in scattering and thus reduction in mobility of charge carriers,which will reduce the vertical mobility and carriers will be constrained in floating gate
- The PtGr combination will result in higher density of states (DOS) as compared to just Gr as FG and thus will result in higher memory window
- It will be interesting to see how Gr will be doped when we place higher work function metal like platinum on it,and its effect on memory performance
- The control samples in this case will be flash transistor with thin platinum metal as FG.This will help in comparison with PtGr transistor and thin metalFG transistor

6.2 Experimental Details

The CMOS flow was used for transistor fabrication with LOCOS isolation. The gate last process was used because it will protect the gate stack from exposure to high temperature annealing when activating the implant. It will also provide the study of transistor characteristics with and without gate stack annealing. The tunnel oxide thickness was around $8 \sim 9$nm and blocking dielectric around 20nm. The two important fabrication steps which are different from Gr flash transistor as mentioned in Appendix A have been mentioned in Table 6.1 below.

Step	Recipe Used	Tool Used
Implantation	RF power: 900W, Sample bias: (-2kV) Pressure: 0.12 mbar, Bias Frequency: 5kHz Duty cycle: 10%, Phosphine: 20sccm	PIII
Annealing to activate the implant	Temperature: $1000^{\circ}C$, Time: 5 sec Ambient: N_2 flow, 800sccm (90 sec) O_2 flow: 50 sccm (90 sec)	RTP Annealsys
Platinum Deposition	20W, 3 min for 15nm thick film	Nordiko

Table 6.1: Important fabrication steps involved in hybrid PtGr FG flash transistor fabrication which differed from Gr flash transistor fabrication

For the Gr FG flash transistor fabrication 1000W recipe was used for implantation,but it was found that 800W and 900W also were optimized for implantation so we can choose the lower power for implantation to reduce the implant induced damage so 900W recipe was choosen for implantation.

6.3 Result and Discussion

6.3.1 P/E Characteristics for Control Transistor

The control transistor means the one without any floating gate just the SiO_2/Al_2O_3 dielectric stack was characterized for P/E at $\pm$10V to see whether dielectric stack is intact and it does not shows any memory characteristics. There was no shift in I-V when control transistor was programmed at +10V neither there was any shift when it was erased at -10V. Fig. 6.1 shows the P/E characteristics for control sample of $10\mu m$ channel length.

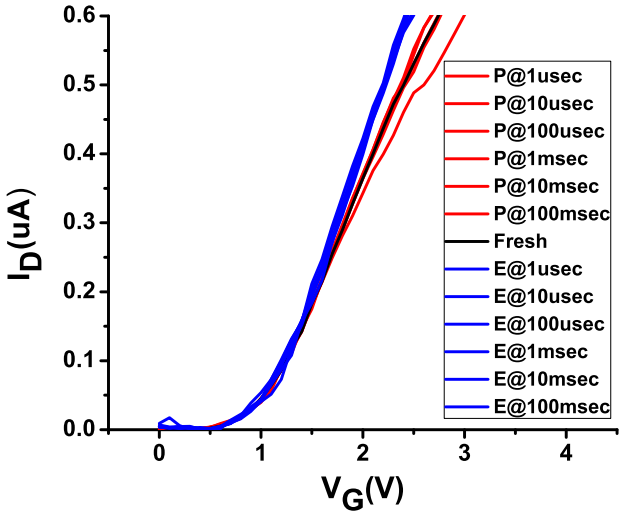

Figure 6.1: P/E characteristics for control sample of $10\mu m$ channel length showing no program or erase window

6.3.2 P/E Characteristics for Pt FG Flash Transistor

The Pt FG transistor has shown some program window but still there was problem with the erase of the transistor for longer pulse duration of 10msec and 100msec. The programming effect was observed for longer erase duration the cause of which might be injection from top gate. The Fig. 6.2 shows P/E characteristics of Pt FG flash transistor for $5\mu m$ channel length.

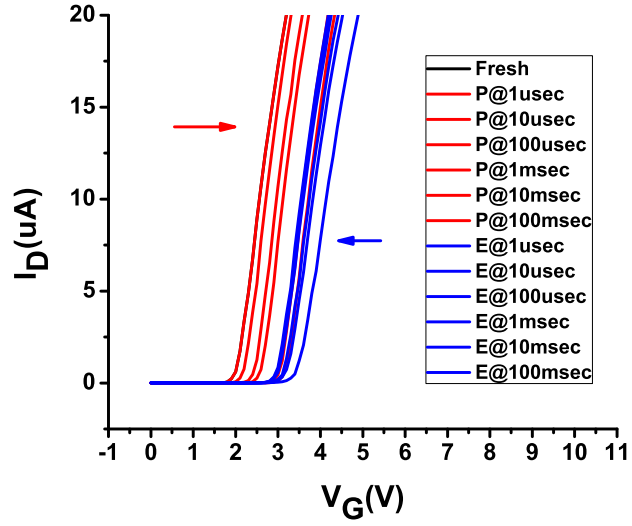

Figure 6.2: P/E characteristics of Pt FG flash transistor at $\pm$10V for $5\mu m$ channel length for V_D=0.1V

6.3.3 P/E Characteristics for PtGr FG Flash Transistor

The PtGr FG transistor were characterized for P/E performance and a very surprising effect was observed. The transistor was showing erase behavior for +10V voltage for all the channel lengths and programming effect for -10V voltage. The simple reason for this behavior could be injection from top gate while trying to program the transistor. As control transistor has not shown any memory characteristics that means dielectric were intact. The Fig 6.3 below shows the P/E characteristics of $5\mu m$ channel length for PtGr FG flash transistor.

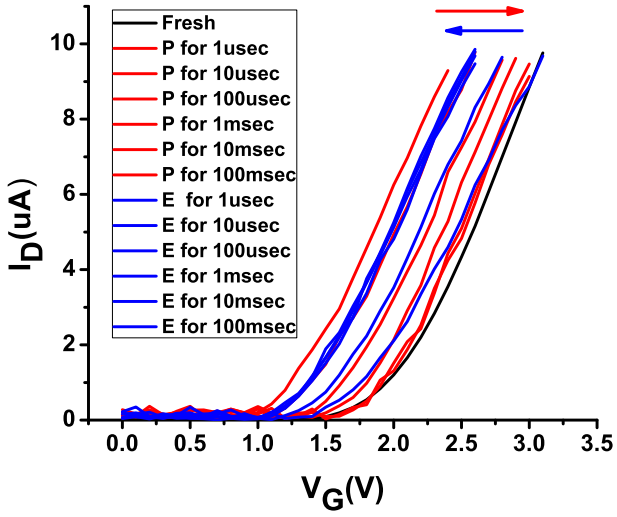

Figure 6.3: P/E characteristics of $5\mu m$ channel length for PtGr FG flash transistor at $\pm$10V for V_D=0.1V

6.3.4 Experiment to Measure Different Currents while Constant Volatge Bias at Gate

The gate current levels where low in range of pA when gate was swept to measure $I_D - V_{GS}$ characteristics after each program and erase pulse. The I_G, I_S and I_D were measured when constant voltage bias was applied to gate during program and erase to check whether I_G is low during P/E pulse application and there is no injection from top gate. The Fig. 6.4(a) and (b),Fig 6.5 (a) and (b) shows the I_G and I_S, I_D currents of $5\mu m$ channel length for Pt FG flash transistor for +10V stress and -10V stress respectively.

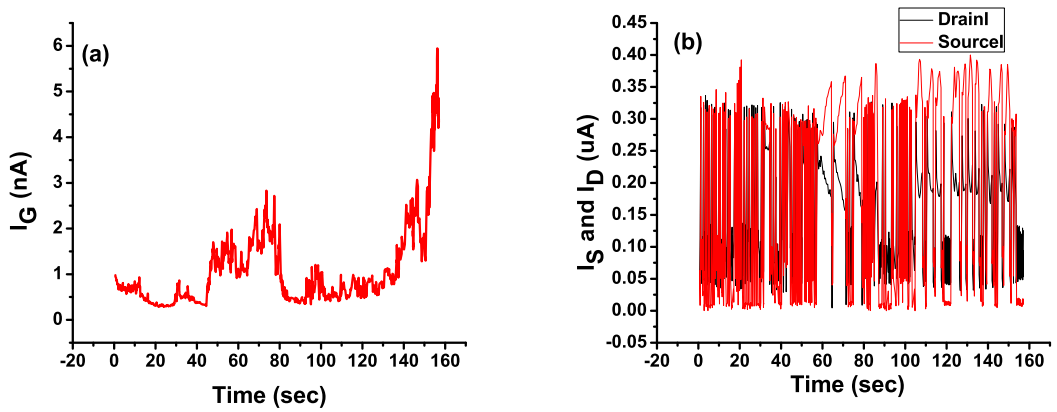

Figure 6.4: (a) I_G current of $5\mu m$ channel length for Pt FG flash transistor when +10V stress is applied on gate (b) I_S and I_D currents of $5\mu m$ channel length for Pt FG flash transistor when +10V stress is applied on gate

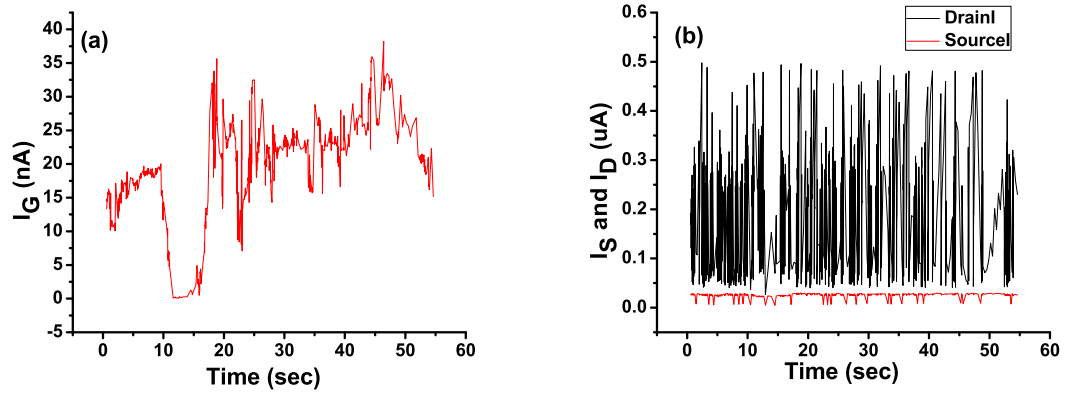

Figure 6.5: (a) I_G current of $5\mu m$ channel length for Pt FG flash transistor when -10V stress is applied on gate (b) I_S and I_D currents of $5\mu m$ channel length for Pt FG flash transistor when -10V stress is applied on gate

The fresh $5\mu m$ channel length device of Pt FG flash transistor was chosen for this experiment and $I_D - V_G$ measurement was done. Then after +10V stress was applied again $I_D - V_G$ measurement was done to see the effect on Vt of the device and it was seen that I-V shifts to right. After -10V stress again $I_D - V_G$ measurement was done and it was seen that I-V shifts to left showing that cell has been erased. Fig. 6.6 below shows the $I_D - V_G$ curves for fresh and after $\pm$10V stress.

The Fig. 6.7(a) and (b),Fig 6.8 (a) and (b) shows the I_G and I_S, I_D currents of $5\mu m$ channel length for PtGr FG flash transistor for +10V stress and -10V stress respectively. The gate currents for Pt and PtGr FG transistors are comparable for both +10V and -10V stress. Even though gate currents are comparable PtGr FG shows the erase behaviour after constant

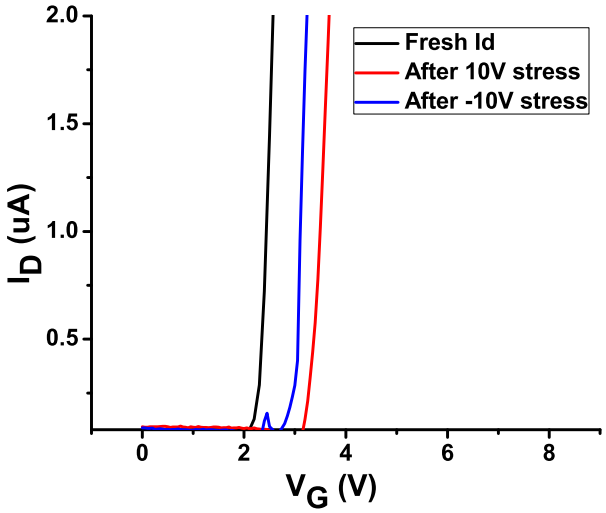

Figure 6.6: The $I_D - V_G$ characteristics of $5\mu m$ channel length device of Pt FG flash transistor for fresh device and after $\pm$10V stress on gate at V_D ==0.1V

+10V stress was applied and program behavior after constant -10V stress was applied on gate. This can be seen from Fig. 6.9 below, if there is injection from top gate then both Pt and PtGr FGs should behave in same way. The cause for this opposite behavior has to be investigated and the problem needs to be resolved. The next chapter dealts with how to identify and resolve the problem.

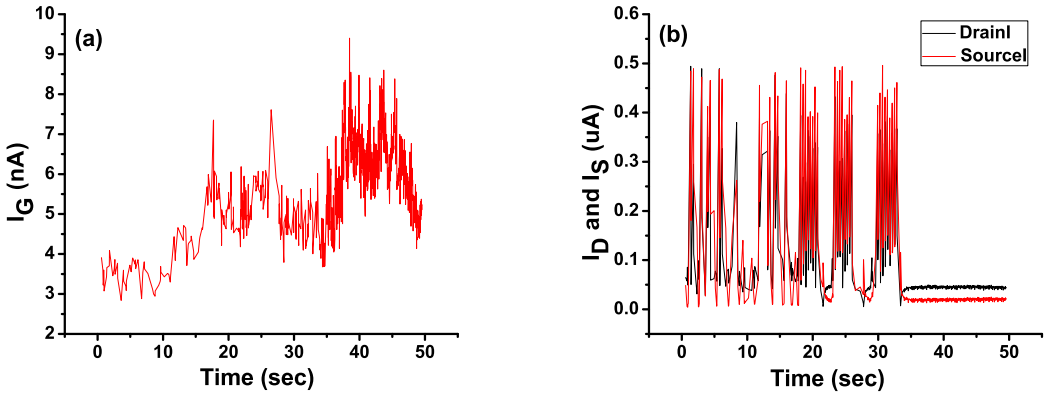

Figure 6.7: (a) I_G current of $5\mu m$ channel length for PtGr FG flash transistor when +10V stress is applied on gate (b) I_S and I_D currents of $5\mu m$ channel length for Pt FG flash transistor when +10V stress is applied on gate

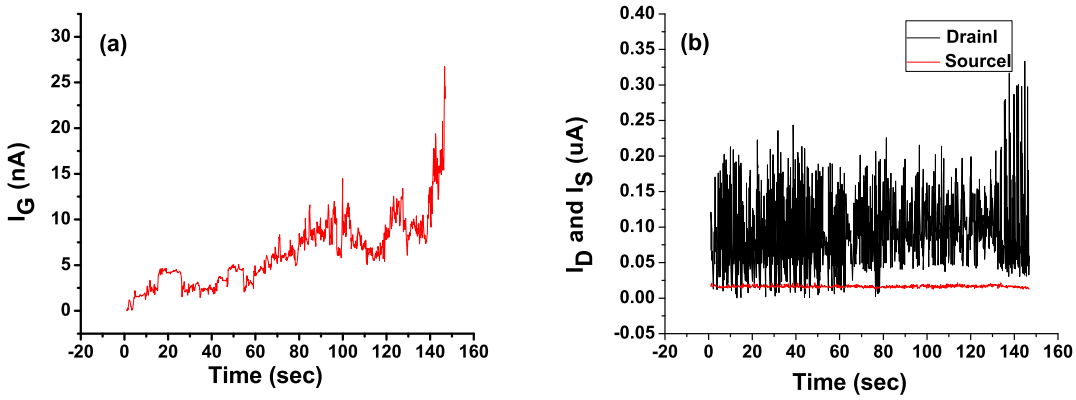

Figure 6.8: (a) I_G current of $5\mu m$ channel length for PtGr FG flash transistor when -10V stress is applied on gate (b) I_S and I_D currents of $5\mu m$ channel length for Pt FG flash transistor when -10V stress is applied on gate

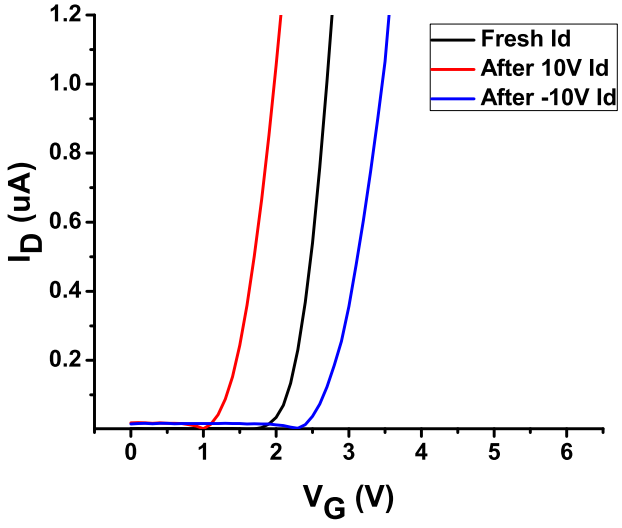

Figure 6.9: The $I_D - V_G$ characteristics of $5\mu m$ channel length device of PtGr FG flash transistor for fresh device and after $\pm$10V stress on gate at V_D=0.1V

Chapter 7

Conclusions and Future Work

7.1 Conclusions

1. The study of high power pulsed-DC reactive sputtered Al_2O_3 film reveals that high power deposition results in films with negative charges also there is sputtered induced damage at high powers. These things make high power deposited Al_2O_3 an undesirable choice for blocking oxide in NAND flash memory application. This was the motivation for studying the low power deposition of Al_2O_3.

2. SiO_2/Al_2O_3 dielectric stack was optimized with low power pulsed-DC reactive sputtered High-k Al_2O_3 as blocking dielectric for NAND flash application. The low power (200W), $900^{\circ}C$ annealed pulsed-DC reactive sputtered Al_2O_3 seems to be good option for blocking dielectric in flash application as it has good breakdown field, RI, dielectric constant, less D_{it} and negative oxide charges and good stoichiometry.

3. After optimization of flash memory stack the emphasis was given on studying the memory performance using MOS capacitor structure for flash memory. But it was observed that programming was slower compared to erasing due to lack of electrons in p-type substrate used in MOS capacitor fabrication.

4. To get the enhanced memory window which will help to improve the fidelity of information stored in memory it was decided to fabricate the FG flash transistor. The working process flow for fabrication has been established. The graphene based FG transistors of length $10\mu m$, $5\mu m$, $3\mu m$, $2\mu m$ has been successfully fabricated indigenously and tested for IV characteristics which are benchmarked with literature. Thus fabrication of gate

last FG transistor was successfully done. The transistor structure will allow us to study memory performance, endurance and retention characteristics of FG flash memory.

5. The interaction of graphene with High-k Al_2O_3 dielectric was studied and it was found that there is increase in workfunction of graphene when it is placed on dielectric the reason being graphene is hole doped when it is placed on dielectric.

6. The platinum metal floating gate has shown some program window but there is problem in erase for longer erase pulse duration some programming effect is observed. The hybrid (Metal + Gr) FG is showing surprising results, erase is observed for positive stress and programming is observed for negative stress. The cause of this behavior in hybrid floating gate might be injection of carriers from top gate, if this is the cause then why Pt FG transistors which are on same wafer shows programming effect for positive gate stress. Further measurements and experiments needs to be done to identify and resolve the issue.

7.2 Future work

1. The programming effect is seen for longer erase pulse duration in both Pt and Gr transistor. The use of high work function metal like Pt as top gate electrode and increasing the Al_2O_3 thickness by 2$\sim$3nm might help in resolving this issue of erase

2. The tunnel dielectric thickness can be reduced from 8nm to 6nm to enable fast programming

3. The bulk and gate currents are to be measured by connecting source and drain to ground and applying constant stress to gate to ensure there is no charge injection from gate for programming and erase. These measurements need to be performed

4. There is one wafer ready till source and drain implant just gate stack needs to taken on it. The tunnel oxide can be kept 6nm and blocking dielectric thickness can be increased to 22$\sim$23nm and high work function metal can be used as top gate. This might help to resolve the aforementioned issue of erase

7.3 List of Publications

The list of publications with the contribution from this thesis work has been mentioned below

1. Abhishek Misra, Mayur Waikar, Amit Gour, Hemen Kalita, Manali Khare, Mohammed Aslam, and Anil Kottantharayil *Work function tuning and improved gate dielectric reliability with multilayer graphene as a gate electrode for metal oxide semiconductor field effect device applications*, published in Appl. Phys. Lett. 100, 233506 (2012).
   Contribution : Tunnel dielectric optimization.

2. Abhishek Misra, Mayur Waikar , Amit Gour, Meenakshi Bhaisare, Sandeep Mane, Pradeep Nyaupane, Anil Kottantharayil SiO_2/Al_2O_3 *dielectric stack with low power pulsed-DC reactive sputtered High-K* Al_2O_3 *as blocking dielectric for NAND flash application*, presented at IWPSD-2011 at IIT Kanpur.
   Contribution : Worked on SiO_2/Al_2O_3 dielectric stack optimization with low power pulsed-DC reactive sputtered High-K Al_2O_3.

3. Abhishek Misra, Hemen Kalita, Mayur Waikar, Meenakshi Bhaisare, Amit Gour, Mohammed Aslam and Anil Kottantharayil *Multilayer Graphene as Charge Storage layer in Floating Gate Flash Memory*, published in Memory Workshop (IMW), 2012 4th IEEE International.
   Contribution : Worked on SiO_2/Al_2O_3 dielectric stack optimization with low power pulsed-DC reactive sputtered High-K Al_2O_3.

4. Meenakshi Bhaisare, Abhishek Misra, Mayur Waikar and Anil Kottantharayil *High quality* Al_2O_3 *dielectric films deposited by pulsed- DC reactive sputtering technique for high-k applications*, published in Nanoscience and Nanotechnology Letters,Vol.4,1-6,2012.
   Contribution : Worked on Fabrication and Electrical characterization of high power Al_2O_3 dielectric MOS capacitors.

5. Abhishek Misra, Sunny Sadana, Satya Suresh, Meenakshi Bhaisare, Senthil Srinivasan, Mayur Waikar, Amit Gaur and Anil Kottantharayil *Effect of Different High-K Dielectrics on the Pt Nanocrystal Formation Statistics (size, density and area coverage) for Flash Memory Application*, published in MRS fall 2010.
   Contribution : Worked on optimization of Al_2O_3 dielectric.

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Appendix A

S. No	Module	Process	Specification	Recipe	System
1	Wafer Select		1-5 ohm-cm, P-Type, <100>, 4" wafer		
2	Wafer labeling	Wafer Back side	Depends on the number of wafers		Micro-2 lab
LOCOS ISOLATION					
3		RCA Clean		2%HF dip = 1152ml DI water+ 48ml (49%HF) 30sec, RCA1=NH_4OH:H_2O_2:DIwater::125ml:250ml:875 ml , 75C on hot plate, 2%HF dip 30sec RCA2 = HCl:H_2O_2:DI water::125ml:250ml:875ml, 2%HF dip 30sec	Wet bench Micro -1 lab
4		Wafer drying			MOT - Nanolab
5		Pad oxide growth	10nm	Pre-growth step: Temperature 800°C; O_2 gas flow 50sccm; N_2 gas flow ON; Duration 120sec Growth step: Temperature 800°C; O_2 gas flow 5000sccm; N_2 gas flow OFF; Duration 40min Ellipsometer measuremet: Thickness obtained 10-11nm mean; Refractive Index 1.468	Ultech Furnance (dry-ox)
6		Ellipsometry to determine thickness of the oxide		Model Used : Air-Cau Thermal SiO_2-100 Si jellison Cau Thermal SiO2 : R.I is 1.468	Ellipso-meter
7		Nitride deposition	60nm, stoichio-metric	Ramp-up step 5min Temp. Stabilization step 2min	Ultech Furnance (Nitride)

				Pressure stabilization step: 5min Deposition step: SiH_4 gas flow 80sccm; NH_3 gas flow 100sccm; N_2 gas flow 1000sccm; Temp 780°C; Pressure 0.3torr; Duration 3900sec Ellipsometer measurement: Thickness obtained 61 nm mean; Refractive Index 1.985	
8		Ellipsometry to determine thickness of the nitride		Model : Air-Cau Si_3N_4-Thermal SiO_2-100 Si jellison Cau Thermal SiO_2 : R.I. 1.468 , Cau Si_3N_4 : R.I. 1.985	Ellipso-meter
9		Active area photo-litho and development		Cleaning of Spinner, Tweezers, Laminar flow bench, hot plate, etc. Wafer cleaning by DI water rinse and N_2 drying. Mask set: CMOS Mask level: Active Dehydration: 130°C, >5min on hot-plate HMDS spin: 7000 rpm,45sec Bake: 120 C, 6 min Photo-Resist: Shipley-1813 Spinning: 6000rpm , 45 sec(Program E) 1.47um Spin the resist on a dummy wafer with nitride and check the thickness using ellipso Prebake: 90°C,2min Exposure: 64mJ/cm2 (V+H)contact - 1um separation Development: MF-319(vertical)	DSA System/ Ellipso-meter

				25sec Post Development Bake 90^{o}C,1min MASK Plate cleaning with Acetone & IPA immediately after lithography	
10		Microscopic Inspection	Inspect the dies in the centre for 10µm, 5 µm, 2 µm channel lengths	Active area pads , Dimension of the region where gate falls in active area, Corner rounding in Active area, Global and Local alignment marks, any other strange feature.	Olympus Micro-scope
11		Etch nitride	Dry Etch	CF_4 gas flow 40sccm O_2 gas flow 4sccm RF Power for Selective Etch (SE) 50W Chamber pressure (SE) 110mtorr Etch rate of Si_3N_4 (SE) (nm/min) 31 Etch rate of SiO_2 (SE) (nm/min) 9 Selectivity obtained 3.5	STS RIE
12		Strip Resist	Acetone Strip	5 min in Acetone followed by IPA	Sonicator
13		Resist Ashing		N_2 gas flow 200sccm O_2 gas flow 3500sccm H_2O Flow 300sccm Pressure 2mtorr Source Power 1400W Time 2min	AMAT Tool + Wet bench
14		Piranha Clean		H_2SO_4:H_2O_2::910ml:390ml, 1hr dip	Wet bench – Micro-1

15		Microscope inspections	Check for resist residues if any	Images have to be saved			Olympus Micro-scope/ Raith 150
16		HF dip		2% HF, 30sec			Wet bench - Micro-1
17		Field oxide growth	280nm, pyrogenic oxide (Use a dummy wafer also)	Growth step	H_2 gas flow O_2 gas flow Temp Torch temp Duration	8000sccm 6000sccm 1000^oC 835^oC 35min	Ultech Furnance (pyro-oxide)
				Ellipsometer measurement	Thickness obtained Refractive Index	290nm mean 1.468	
18		Ellipsometry to determine thickness of the oxide		Model : Air-Cau Thermal SiO_2-100 Si jellison Cau Thermal SiO_2 : R.I. 1.468			Ellipso-meter
19		Nitride etch	Wet Etch (Use a dummy Nitride wafer also)	BHF (5:1)dip H_3PO_4 Concentration Etch temperature Si_3N_4 Etch rate SiO_2 Etch rate Total etch time	10 sec 87% 160^oC ~2nm/min 0.2nm/min 50min		TMAH Setup
20		Microscope inspections		Images have to be saved.			Olympus Microscop e/ Raith 150

21		RCA Clean		2%HF dip = 1152ml DI water+ 48ml(49%HF) 30sec , RCA1=NH_4OH:H_2O_2:DIwater::125ml:250ml:875 ml , 75C on hot plate , 2%HF dip 30sec RCA 2= HCl:H_2O_2:DI water::125ml:250ml:875ml, 2%HF dip 30sec			Wet bench Micro1
SOURCE / DRAIN IMPLANTATION USING DUMMY GATE							
22		Screening oxide for implantation	~6nm (Use a dummy wafer)	Pre-growth step	Temperature	850^{o}C	Ultech Furnance (dry-ox)
					O_2 gas flow	50sccm	
					N_2 gas flow	ON	
					Duration	30sec	
				Growth step	Temperature	850^{o}C	
					O_2 gas flow	500sccm	
					N_2 gas flow	OFF	
					Duration	120sec	
				Annealing step	Temp	850^{o}C	
					N_2 gas flow	ON	
					Duration	5min	
				Ellipsometer measurement on dummy	Model : Air-Cau Thermal SiO_2-100 Si jellison Cau Thermal SiO_2 : R.I. 1.468	Thickness 4nm mean	

23		Dummy gate litho using DSA for sorce drain implant		Cleaning of Spinner, Tweezers, Laminar flow bench, hot plate, etc. Wafer cleaning by Acetone, IPA rinse followed by DI water rinse and N_2 drying Mask set: CMOS Mask level: Gate Dehydration: 130^{o}C, >5min on hot-plate HMDS spin: 7000 rpm,45sec Bake: 120 C, 6 min Photo-Resist: Shipley-1813 Spinning: 6000rpm , 45 sec(Program E) Prebake: 90^{o}C,2min Exposure: 50mJ/cm2 (V+H)contact -1um separation Development: MF-319(vertical) 30sec Post deve-lopment bake: 90^{o}C,1min MASK Plate cleaning with Acetone & IPA immediately after lithography	DSA System
24		Microscopic Inspection (To check the gate fingers)	Inspect the dies in the centre for 10µm, 5 µm, 2 µm channel lengths fingers	Active area pads , Dimension of the region where gate falls in active area, Corner rounding in Active area, Global and Local alignment marks, any other strange feature. Make sure that gate fingers don't touch active area	Olympus Micro-scope
25		Phosphorous Implant		RF power-1000W,Sample bias-(-2KV), Press-1.2E-1 mbar, Bias freq-5KHz,Duty Cycle-10%, Phosphine-20sccm.	PIII
26		Resist Ashing		N_2 gas flow: 200sccm O_2 gas flow: 3500sccm H_2O Flow: 300sccm Pressure: 2mtorr	AMAT Tool + Wet bench

				Source Power 1400W Time 2min	
27		Piranha Clean		H_2SO_4:H_2O_2::910ml:390ml, 1hr dip	Wet bench Micro-1
28		Microscope inspections	Check for resist residues if any	Images have to be saved	Olympus Micro-scope/ Raith 150
29		HF dip to remove the screening oxide		2% HF, 30sec	Wet bench Micro-1
30		Annealing to activate the implant		Temp-1000 C,Time-5 sec, Ambient-N_2 flow-800sccm(90sec), O_2 flow-50 sccm(90 sec)	RTP Anneal Sys
FLASH MEMORY GATE STACK					
31		RCA Clean		2%HF dip = 1152ml DI water+ 48ml (49%HF) 30sec, RCA1=NH_4OH:H_2O_2:DIwater::125ml:250ml:875ml , 75C on hot plate, 2%HF dip 30sec RCA_2 = HCl:H_2O_2:DI water::125ml:250ml:875ml, 2%HF dip 30sec	Wet bench Micro -1 lab
32		Tunnel oxide SiO_2 growth	6nm (Use the dummy wafer)	Pre-growth step: Temperature 850^oC; O_2 gas flow 50sccm; N_2 gas flow ON; Duration 120sec Growth step: Temperature 800^oC; O_2 gas flow 5000sccm; N_2 gas flow OFF; Duration 30min Annealing at 900 ^oC for 15min in N_2 Ellipsometer measuremet: Thickness obtained 6.5nm mean; Refractive Index 1.468	Ultech Furnance (dry-ox)

33		Ellipsometry Measurement		Model : Air-Cau Thermal SiO_2-100 Si jellison Cau Thermal SiO_2 : R.I. 1.468	Ellipsometer
34		Graphene Floating gate	5 to 6nm	Keep the wafer at 130 ^oC on hot plate and drop cast the graphene	Hot plate Nano lab
35		Blocking Dielectric Al_2O_3	20nm (Use dummy wafer)	Power : 200W, Deposition Time : 840sec, Gas flow ratios : Ar:O_2 (10:14), Target voltage : 200V, Chamber press : 1.35mTorr, Thickness : 15nm, RI=1.587.	AMAT Endura
36		Ellipsometry Measurement		Model : Air-Cau sputter Al_2O_3-100 Si jellison Cau sputter Al_2O_3 : R.I. 1.58	Ellipsometer
37		TiN top gate deposition		Power : 350W, Gas flow ratios : Ar: N_2 (20:20)sccm, Time : 15min, Chamber pressure : 1.65mTorr, Thickness around : 80nm	AMAT Endura
38		Third level gate litho using DSA for flash gate stack		Cleaning of Spinner, Tweezers, Laminar flow bench, hot plate, etc. Wafer cleaning by Acetone, IPA rinse followed by DI water rinse and N_2 drying Mask set: Flash Transistor Mask level: Gate Dehydration: 130^oC, >5min on hot-plate HMDS spin: 7000 rpm,45sec Bake: 120 C, 6 min Photo-Resist: Shipley-1813 Spinning: 6000rpm , 45 sec(Program E) Prebake: 90^oC,2min Exposure: 64mJ/cm2 (V+H)contact -1um separation Development: MF-319(vertical) 30sec	DSA System

				Post deve- lopment bake 90^{o}C,1min MASK Plate cleaning with Acetone & IPA immediately after lithography	
39		Microscopic Inspection after third level litho	Inspect the dies in the centre for 10µm, 5 µm, 2 µm channel lengths	Active area pads , Dimension of the region where gate falls in active area, Corner rounding in Active area, Global and Local alignment marks, any other strange feature.Make sure gate fingers don't touch the active area	Olympus Micro-scope
40		TiN Etch		Cl_2: 100sccm, BCl_3: 30sccm, RF power: 1000 sccm, Bias power: 130W	AMAT Etch Centura
41		Al_2O_3 Etch		Cl_2: 20sccm, BCl_3: 60sccm, Ar: 5sccm, RF power: 600W, Bias power: 30W, Chamber press: 9 mTorr, Time: 45 sec.	AMAT Etch Centura
42		Resist ashing and graphene removal at the same time		Step 1: RF Power: ---- N_2: --- O_2 ----- H_2O 300 sccm Time 10 sec Pressure 2 Torr Step 2: RF Power: 1400 W N_2: 200 sccm O_2: 3000 sccm H_2O: 300 sccm Time: 120 sec Pressure: 2 Torr	AMAT Etch Centura
43		Piranha Clean		H_2SO_4:H_2O_2::910ml:390ml, 1hr dip	Wet bench Micro-1
44		Microscopic Inspection after piranha cleaning	Inspect all the dies and active areas of all the transistors	Check whether all the resist has been removed and there are no residues	Olympus Micro-scope
45		Back side Al Metallization		Current 55 A, Pressure - 2 X 10 -6 mbar	Thermal Evaporator (Micro 1 lab)