# Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives

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*Abstract*—This paper presents a technology review of voltage-source-converter topologies for industrial medium-voltage drives. In this highly active area, different converter topologies and circuits have found their application in the market. This paper covers the high-power voltage-source inverter and the most used multilevel-inverter topologies, including the neutral-point-clamped, cascaded H-bridge, and flying-capacitor converters. This paper presents the operating principle of each topology and a review of the most relevant modulation methods, focused mainly on those used by industry. In addition, the latest advances and future trends of the technology are discussed. It is concluded that the topology and modulation-method selection are closely related to each particular application, leaving a space on the market for all the different solutions, depending on their unique features and limitations like power or voltage level, dynamic performance, reliability, costs, and other technical specifications.

*Index Terms*—High-power applications, multilevel converters, voltage-source inverters (VSIs).

## I. INTRODUCTION

**T**HE FIELD of high-power drives has been one of the most active areas in research and development of power electronics in the last decades. Several industrial processes have increased their power-level needs, driven mainly by economy of scale (production levels and efficiency), triggering the development of new power semiconductors, converter topologies, and control methods. The development of high-power converters and medium-voltage (MV) drives started in the mid-1980s when 4500-V gate-turn-off (GTO) thyristors became commercially available [1]. The GTO was the standard for the MV drive until the advent of high-power insulated-gate bipolar transistors (IGBTs) and gate-commutated thyristors (GCTs) in the late 1990s [2], [3]. These switching devices are now extensively used in high-power drives due to their superior switching characteristics, reduced power losses, ease of gate control, and snubberless operation.

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High-power converters have found widespread applications in industry. They can be used for pipeline pumps in the petrochemical industry [4], fans in the cement industry [5], pumps in water pumping stations [6], traction applications in the transportation industry [7], steel rolling mills in the metals industry [8], grid integration of renewable-energy sources [9]–[11], reactive-power compensation [12]–[14], and other applications [15], [16]. A summary of the MV-drive applications is given in [17, Appendix].

One of the major markets for MV drives is retrofit applications. It is reported that 97% of the currently installed MV motors operate at a fixed speed, and only 3% of them are controlled by variable-speed drives [18]. When fans or pumps are driven by a fixed-speed motor, the control of air or liquid flow is normally achieved by conventional mechanical methods, such as throttling control, inlet dampers, and flow-control valves, resulting in a substantial amount of energy loss. The installation of the MV drive can lead to a significant savings on energy cost. It was reported that the use of the variable-speed MV drive resulted in a payback time of the investment from one to two and a half years [6].

Fig. 1 presents a simplified classification of converter families used in high-power drive applications, which have a basic division into direct and indirect topologies. The former usually connects the load directly to the source through power semiconductors and a suitable control logic, while the latter transfers the power in two stages, rectification and inversion, and is usually linked by an energy-storage component.

For direct conversion, the cycloconverter (CCV) is the most used topology in high-power applications, which uses an array of power-semiconductor switches to connect directly the power supply to the machine, converting a three-phase ac voltage with a fixed magnitude and frequency to a three-phase ac voltage with variable magnitude and variable frequency. It allows power flow in both directions in an efficient way, although limited in dynamic performance. Matrix converters also belong to this category but are not included in the classification, since the technology is still not available for high-power ranges, reaching only up to 150 kVA [19].

On the other hand, indirect converters are classified into current-source and voltage-source topologies, depending on the dc-link energy-storage component. Fig. 2 shows a general block diagram of an indirect MV drive. Depending on the system requirements and the type of the converters employed, the line- and motor-side filters are optional. A phase-shifting transformer with multiple secondary windings is often used mainly for the reduction of line-current distortion. The rectifier
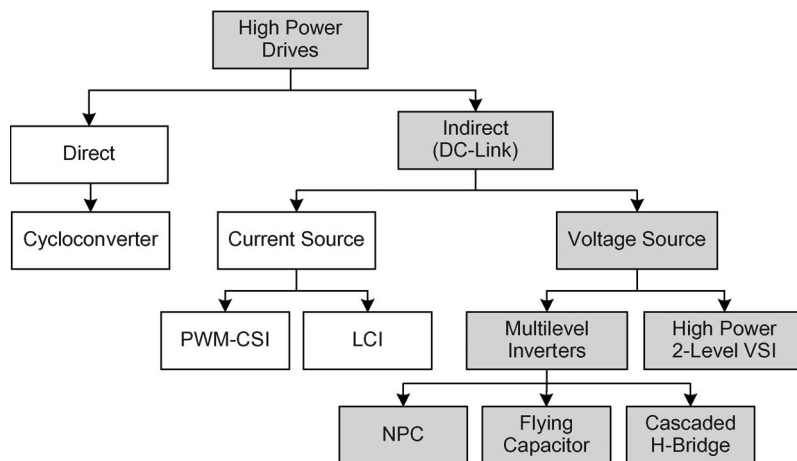
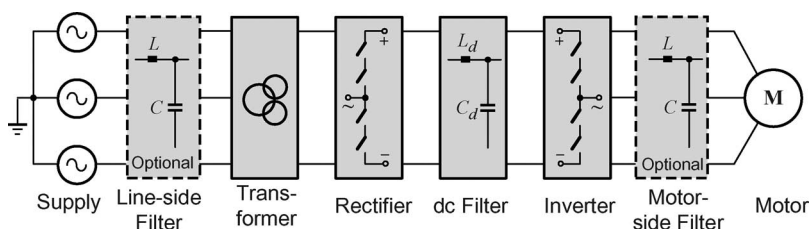Fig. 1. Classification of converters for high-power drives (>1 MW).



Fig. 2. General block diagram of the MV drive.

converts the utility supply voltage to a dc voltage with a fixed or adjustable magnitude. The commonly used rectifier topologies include multipulse diode or thyristor rectifiers and pulsewidth-modulated (PWM) rectifiers. The dc filter can simply be a capacitor that provides a stiff dc voltage in voltage-source drives or an inductor that smoothes the dc current in current-source drives.

For high-power applications, two current-source-inverter (CSI) topologies have found industrial presence: the load-commutated inverter (LCI) and the PWM-CSI. The LCI has been used for several decades featuring simple converter topology, low manufacturing cost, and reliable operation. Its main drawbacks include low-input power factor and distorted input-current waveforms [20]. These problems are overcomed by the newer PWM-CSI solution.

On the other hand, high-power voltage-source-inverter (VSI)-fed drives, which correspond to the darkened boxes in the classification diagram shown in Fig. 1, have experienced a higher market penetration and a more noticeable development over the last decade, in comparison to CSI topologies. The classical two-level VSIs (2L-VSIs) were limited to low- or medium-power applications due to the power-semiconductor voltage limits. The series connection of switching devices enabled the high-power 2L-VSI. However, the addition of few components, like diodes or capacitors, permitted a more interesting use of these additional switches (and control degrees) to enhance the quality of input and output variables, originating the multilevel-VSI (ML-VSI) technology.

Although ML-VSIs were originally developed to reach higher voltage operation, before being restricted by semiconductor limits, the extra switches and sources (provided by multiple dc-link capacitors) could be used to generate different output-voltage levels, enabling the generation of a stepped waveform with less harmonic distortion, reducing $dv/dt$'s and common-mode voltages, and enabling operation under fault conditions and converter modularity [21]. These characteristics have made them popular for high-power MV applications. Many topologies have been developed, among them, the neutral-point clamped (NPC) [22], flying capacitor (FC) [23], and the cascaded H-bridge (CHB) [24], are the most studied and commercialized by major manufacturers. Currently, these topologies cover a voltage and power range from $v_{ll} = 2.3$ to 13.8 kV and $S_C = 0.3$ kVA to 32 MVA, respectively [25]. The following pages present in more detail the operating principles of these converters, the most relevant characteristics, established modulation methods, latest advances, and future trends.

## II. TWO-LEVEL VSI

The well-known 2L-VSI is also applied for medium- and high-power traction and industrial high-power drives. IGBT modules of 3.3, 4.5, and 6.5 kV are the mostly used high-power semiconductors today. To increase the converter voltage, a series connection of these switches is applied. Thus, an inverter leg is composed by two groups of active switches, each consisting of two or more switches in series, depending on the dc-link voltage. In addition, additional capacitors in series could be necessary to reach the desired voltage. In practical MV drives, MV film capacitors are normally used as a dc-link filter instead of electrolytic capacitors. Therefore, there is no need to connect the film capacitors in series. The power circuit of
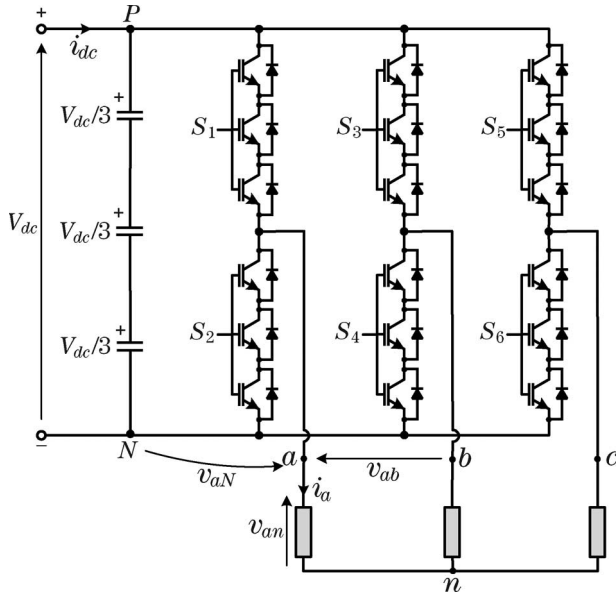
Fig. 3.  Two-level high-power VSI power circuit.

the high-power 2L-VSI is shown in Fig. 3, considering three switches in series connection controlled with the same gating signal and, hence, working as a single switch.

The increase of the voltage level, and the requirement of additional dc-link capacitors, makes the use of multipulse rectifiers attractive. These types of rectifiers enable the desired voltage operation while reducing the input-current harmonics. This is particularly important in high-power applications, where the amount of power involved in these harmonics can be harmful for the utility grid and is restricted by standards. Fig. 4 shows 12, 18, and 24 pulse circuit configurations and qualitative input-current waveforms when considering a dc choke as a filter.

The most used modulation schemes for the high-power VSI are the well-known bipolar PWM, including third-harmonic injection, space-vector modulation (SVM), and offline optimized pulse patterns [e.g., selective harmonic elimination (SHE)] [26].

## III. MULTILEVEL CONVERTERS

Multilevel-converter technology has experienced a fast growing attention in the last decade, and several topologies have been reported [21]. This section is focused mainly on the most established and commercialized multilevel inverters, i.e., the three-level NPC, the four-level FC, and the CHB converter, that will be analyzed for seven levels, although it is also commercially available in 9, 11, and 13 levels.

### A. Neutral-Point Clamped

*1) Topology Description:* In the early 1980s, a new pioneering converter topology was proposed [22], [27]: the three-level NPC voltage-source converter (3L NPC-VSC), also known as diode-clamped converter. Since all semiconductors are operated at a commutation voltage of half the dc-link voltage, the

topology offered a simple solution to extend voltage and power ranges of the existing 2L-VSC technology, which were severely limited by the blocking voltages of power semiconductors with active turn-on and turn-off capabilities. Hence, the converter was of particular interest for MV applications (2.3–4.16 kV). The 3L NPC-VSC was soon introduced to the market by leading manufacturers and gained more and more importance [28]–[30]. The three-level power circuit is shown in Fig. 5. NPC converters can be extended to generate more output-voltage levels [21], [31], [32]. However, these topologies have not found industrial acceptance to date and, therefore, will not be further discussed in this paper.

In a 2L VSC, a series connection of two switches per switch position is required to enable an operation at the same dc and converter voltage like a 3L NPC-VSC. The 3L NPC-VSC features two additional diodes per phase leg as compared to a 2L VSC with a direct series connection of two devices per switch position. These so-called NPC diodes link the midpoint of the "indirect series connection" of the main switches to the neutral point of the converter. This allows the connection of the phase output to the converter neutral point $N$ and enables the three-level characteristic of the topology. Table I shows the switch states of one phase leg.

Note that two pairs of switches of one leg receive inverted gate signals $S_{ak}$ and $\bar{S}_{ak}(k = 1, 2)$ to enable a proper modulation and to avoid forbidden switch states. The overall converter switching state can be defined by $S = (S_a, S_b, S_c)$, where, according to Table I, each phase switching state $S_x$ $(x = a, b, c)$ can be represented by a $(+1)$ when generating $V_{dc}/2$, a $(-1)$ when generating $-V_{dc}/2$, or a $(0)$ when connected to the neutral point, hence generating zero-voltage level. Combining the states of all three phases, the 3L NPC-VSC features $n_{ss} = L^3 = 3^3 = 27$ switch states, where $L$ is the number of voltage levels of $v_{xN}$ $(x = a, b, c)$. The different switch states can be represented in the complex $\alpha-\beta$ frame, simply by calculating the space vector $(\mathbf{v}_s)$ associated to each switching state

$$
\begin{aligned}
\mathbf{v}_s &= \frac{2}{3}\left[ v_{aN} + a v_{bN} + a^2 v_{cN} \right] \\
&= \frac{2}{3}\left[ S_a \frac{V_{dc}}{2} + a S_b \frac{V_{dc}}{2} + a^2 S_c \frac{V_{dc}}{2} \right]
\end{aligned} \tag{1}
$$

where $a = e^{j2\pi/3}$. The 27 different switching states and their corresponding voltage vectors are plotted in Fig. 6. Note that some switching states have redundant space-vector representations. This redundancies can be used for neutral-point balance purposes.

*2) Modulation Methods:* There are different modulation schemes to generate the desired converter voltage. Commonly applied modulation methods in industry are the carrier-based sine-triangle modulation [33]–[35] based on multiple-carrier arrangements in vertical shifts. In addition, the space-vector modulation has been extended for the multilevel case [36], [37] and has been generalized via 3-D algorithms [38] even for multiphase systems [39]. Other methods, like SHE, have also been adapted for multilevel waveforms [40]–[42].
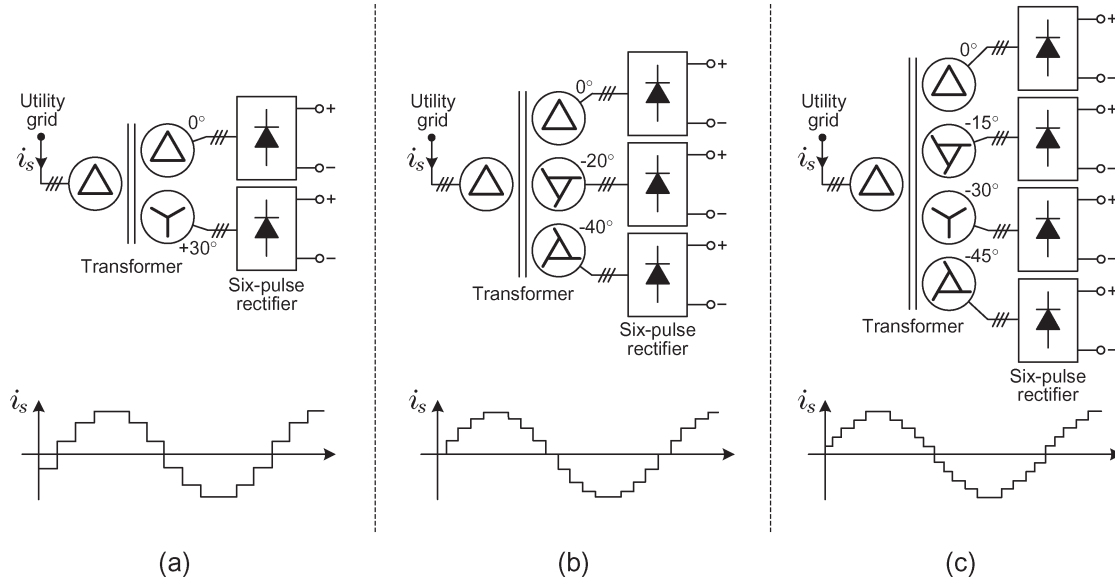
Fig. 4. Multipulse diode rectifiers power circuit and input current: (a) 12 pulse, (b) 18 pulse, and (c) 24 pulse.
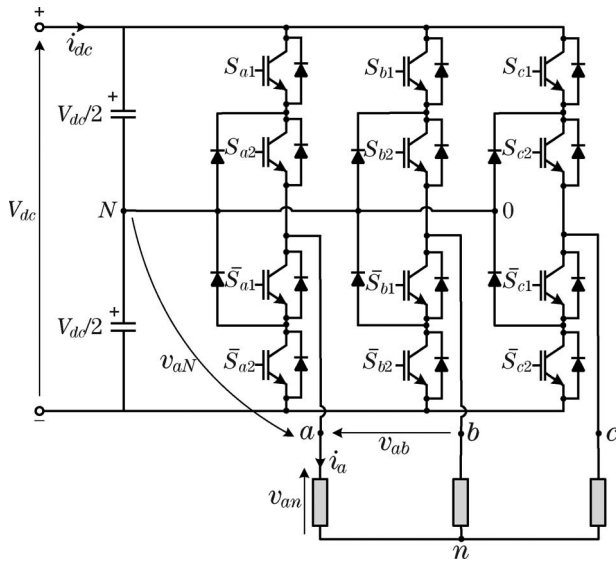


Fig. 5. Circuit configuration of 3L NPC-VSC.



Fig. 6. Voltage space vectors generated by a 3L NPC-VSC.

TABLE I
THREE-LEVEL NPC SWITCH STATES (PHASE $a$)

| Output Voltage | Gate signals | | Switching state |
|---|---|---|---|
| $v_{aN}$ | $S_{a1}$ | $S_{a2}$ | $S_a$ |
| $V_{dc}/2$ | 1 | 1 | $(+)$ |
| 0 | 0 | 1 | $(0)$ |
| $-V_{dc}/2$ | 0 | 0 | $(-)$ |

As an example, Fig. 7 shows the waveforms for a phase-disposition (PD) sine-triangle modulation, which is also known as level-shifted PWM. To enable a maximum modulation index

$$M = \frac{\hat{V}_{aN}^1}{\frac{V_{dc}}{2}} \quad (2)$$

of $M = 1.15$, the reference voltage contains one-sixth third harmonics.

The spectrum of midpoint and line-to-line voltage can be appreciated in Fig. 8(a) and (b), respectively. Due to the increased number of voltage levels, the harmonic voltages and the total harmonic distortion (THD) are distinctly lower than that of a comparable 2L VSC. The harmonics appear in carrier bands with a frequency of $f_{cb} = n \cdot f_c$, where $n$ is an integer $(n = 1, 2, 3, \ldots)$ and $f_c$ is the frequency of the carrier signal.

One of the drawbacks of this topology is the need to control the neutral-point potential, or the difference between both capacitors' voltages, to maintain a balanced and proper operation. This subject has been extensively studied and reported in several works over more than a decade [43]–[47] and is considered a solved problem in industry.

The control of the 3L NPC-VSC is determined by the requirements of the application. While the field-oriented control [48], [49] and the direct-torque control [50], [51] are widely spread control schemes of machine-side converters, the

Fig. 7.   Waveforms of 3L NPC-VSC applying PD-PWM one-sixth-added third harmonics ($f_c/f_1 = 15$; $M = 0.8$).
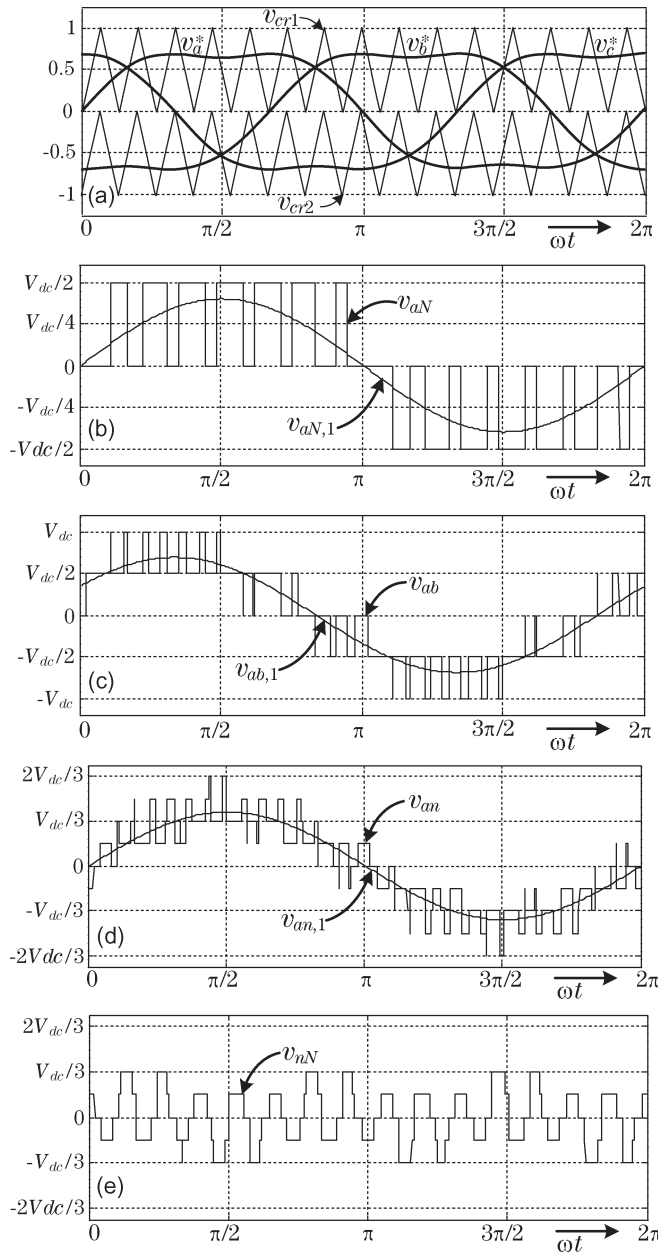


Fig. 8.   Voltage spectrum of 3L NPC-VSC applying a PD-PWM with one-sixth-added third harmonics ($f_c/f_1 = 15$; $M = 0.8$). (a) Phase-neutral voltage. (b) Line–line voltage.

voltage-oriented control [52] or the direct-power control [52] are often applied in active front-end (AFE) grid converters.

*3) Modularity and Common DC-Bus Configurations:* The 3L NPC-VSC topology can be used as active rectifier inverter, respectively. Usually, the layout and design of the 3L NPC-VSC as rectifier and inverter are identical. As grid-side converter (active rectifier), the 3L NPC-VSC allows four-quadrant operation for regenerative braking, an adjustable power factor in the entire drive-operating range, and sinusoidal grid currents by the use of optimized pulse patterns. Alternatively, conventional 6-, 12-, 18-, 24-, or 36-pulse full-bridge diode rectifiers can be used as grid-side converter in applications with two-quadrant operation. If short-term braking capability is required in this case, an additional brake chopper can be installed. In an industrial converter or drive configuration, a high degree of modularity is
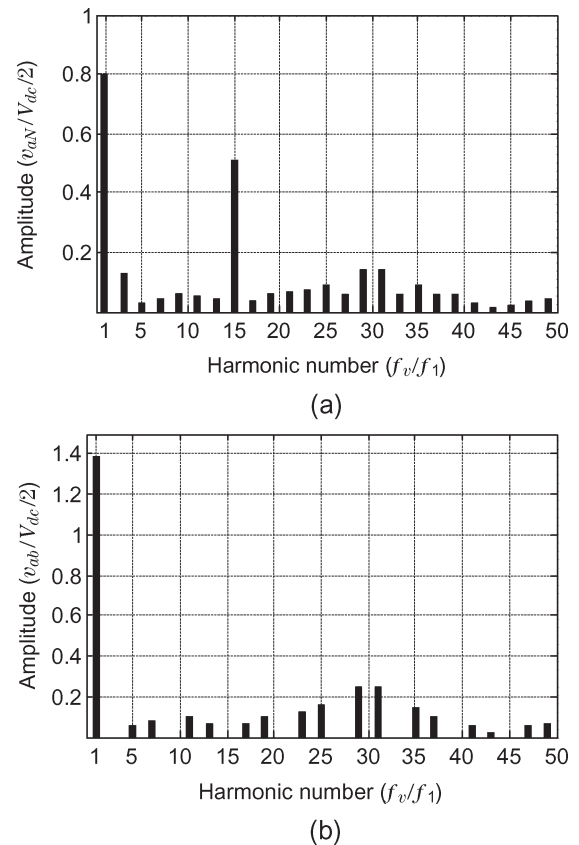
achieved by the realization of rectifier and inverter units which can be connected in various configurations to one dc-voltage link, which is usually called common dc bus.

Fig. 9 shows the typical converter arrangement for a single motor drive. The grid-side converter can be realized by a 12-pulse diode rectifier [Fig. 9(a)] or a 3L NPC-VSC [Fig. 9(b)]. A common dc-bus converter configuration to supply one motor with three winding systems can be taken from Fig. 10. Usually, windings in Y-connection are chosen. An increase of the power and the realization of redundancy schemes enabling a higher availability are possible. If a 12-pulse diode rectifier is applied in each of the three subconverters, then a 36-pulse behavior of the three rectifiers can be realized. Alternatively, 3L NPC-VSCs can also be used as rectifiers. Fig. 11 shows a multimotor-drive configuration for multiple synchronous or induction machines. This, or similar configurations, are mainly applied in rolling mills or gear-test benches. If the machines operate as motor and generator, respectively, there is an energy flow from the generator to the motor via the common dc bus. Thus, the rated power of the transformer and the line-side converter can substantially be lower than the sum of the converter powers of the machine-side converters.

*4) Latest Technological Developments:* Semiconductors: Currently, 3.3-, 4.5-, and 6.5-kV IGBTs (modules or press packs) and 4.5- and 5.5-kV IGCTs (press packs only) are applied in newly developed industrial 3L NPC-VSCs. Both IGBTs and IGCTs have replaced GTOs almost completely
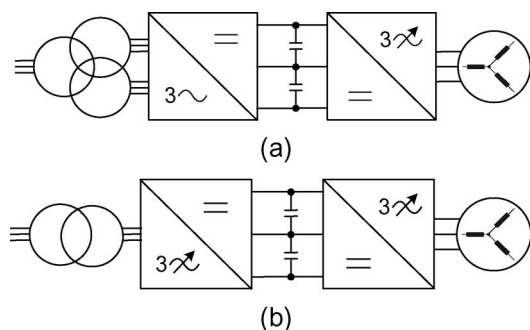
Fig. 9. Block diagram of single-motor-drive configuration (grid-side converter: (a) 12-pulse diode rectifier, (b) 3L NPC-VSC; machine-side converter: 3L NPC-VSC).
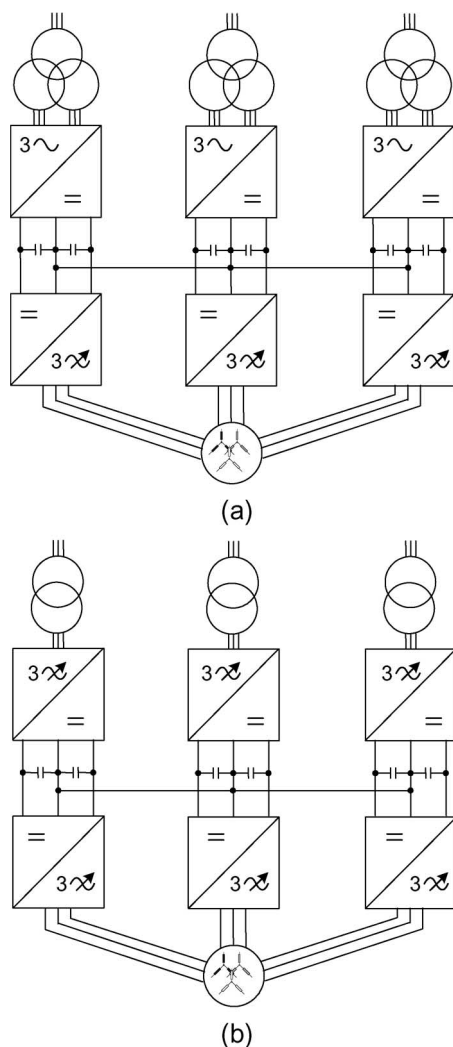


Fig. 10. Block diagram of motor-drive configuration with three winding systems (grid-side converters: (a) three 12-pulse diode rectifiers, (b) three 3L NPC-VSC; machine-side converters: three 3L NPC-VSCs).



Fig. 11. Block diagram of common dc-bus multimotor-drive configuration supplying three electric machines (grid-side converter: 3L NPC-VSC; machine-side converters: three 3L NPC-VSCs).



Fig. 12. IGCT 68 mm (10 kV, 1 kA).

in newly developed commercially available converters for MV drives for about ten years [25]. While state-of-the-art IGBT converters are operated snubberless in the hard-switching mode, IGCT converters require a small clamp inductor which limits short-circuit peak currents and the $di/dt$ during IGCT turn-on transients to enable diode turn-off transients within the safe operating area, as well as homogeneous IGCT turn-on
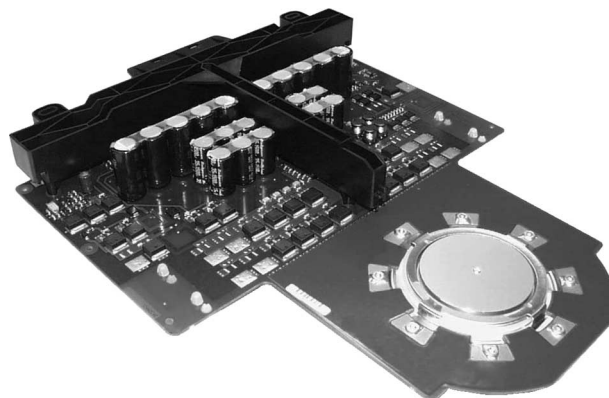
transients [25], [28], [30], [53]. To achieve output voltages of $V_{ll} = 6-7.2$ kV, a series connection of two or three devices per switch position or devices with higher blocking voltages are required [54]. To enable an extension of the converter-voltage range, efficiency concepts for a series connection of IGBTs [28] or IGCTs [55] were recently developed. Alternatively to a series connection of IGCTs, 10-kV IGCTs have also been developed and successfully tested, which enable converter voltages of $4.16$ kV $< V_{ll} \leq 7.2$ kV without a series connection of devices (Fig. 12) [54].

The main structural drawbacks of the 3L NPC-VSC are the unequal loss distribution and the resulting unsymmetrical semiconductor-junction temperature distribution [56]. The unequal loss distribution can be substantially improved, if active switches are placed in both NPC branches, as shown in Fig. 13 [56]. The corresponding circuit configuration is called 3L active-NPC-VSC (3L ANPC-VSC). The more equal semiconductor-junction temperature distribution enables a substantial increase of the converter output current and power at nominal operation and at zero speed or alternatively an

Fig. 13.   Circuit configuration of 3L ANPC-VSC.

TABLE II
SEMICONDUCTORS, CONVERTER VOLTAGE, AND POWER RANGE OF
MEDIUM VOLTAGE DRIVES (MVDs) USING THE 3L NPC-VSC
(POWER RANGE INCLUDING COMMON DC-LINK CONFIGURATIONS)

| Semiconductor | Semiconductor blocking voltage [kV] | Converter voltage [kV] | Converter power [MVA] |
|---|---|---|---|
| IGBT Module | 3.3[kV], 6.5[kV] | 2.3, 3.3, 4.16, 6, 6.6 | 0.8 -10 |
| IGBT Press Pack | 4.5[kV] | 3.3, 3.4 | 6 - 32 |
| IGCT Press Pack | 4.5[kV], 5.5[kV] | 2.3, 3.3, 4.16 | 0.3 - 30 |

increase of the carrier frequency. Steimer *et al.* [57] describes the application of the 3L ANPC-VSC in a 3.3-kV 16-MVA VSC on the basis of IGCTs.

*5) Applications:* Currently, the 3L NPC-VSC is the most widely spread topology in MV drives. Table II summarizes the voltage and power range of commercially available MV drives on the basis of the 3L NPC-VSC.

It becomes clear that IGCTs compete against IGBT modules and IGBT press packs in the low- to medium- and medium- to high-power ranges, respectively. MV-drive applications, using the 3L NPC-VSC, span a wide range of areas, among them are oil and gas, metals, power, mining, water, marine, and chemical processes [25], [53].

### B. Cascaded H-Bridge

The CHB multilevel inverter appeared first in 1988 [24]. It matured during the 1990s and gained more attention after 1997 [58], [59]. Currently, this topology has been used in MV high-power drives (maximum rates of 13.8 kV, 1400 A, and 31 000 kVA) due to its modular structure and power-quality operational characteristics.

*1) Topology Description:* The CHB is composed by the series connection of H-bridge power cells. For this reason, the CHB is also known as a multicell inverter. Each cell includes a single-phase 3L H-bridge inverter, a capacitive dc-link, a rectifier, and an independent or isolated voltage source provided



Fig. 14.   CHB power cells. (a) Nonregenerative. (b) Regenerative.



Fig. 15.   CHB power circuit, here, shown for a $2k + 1$-level configuration.

by transformer secondaries or batteries. Usually, the rectifier consists of a three-phase-diode full-bridge rectifier, while an AFE is preferred for regenerative applications, as shown in Fig. 14(a) and (b), respectively [60], [61].

A generalized three-phase CHB multilevel inverter with $k$ power cells is shown in Fig. 15, here shown with diode rectifiers and the corresponding multipulse transformer, with appropriate secondary winding displacements for input-current harmonics reduction. The relation between the number of power cells, the number of output levels, the number of voltage vectors, the displacements between secondaries of the transformer, the input-current pulses, and the output voltage is summarized in Table III. Note that an increase in the voltage ratings (which is imposed by the application) has a direct impact in the CHB power quality, due to the increase in the number of the output-voltage levels and the increase of the number of input-current

TABLE III
CHB RELATIONS PER CELL

| n° of cells | n° of levels | n° of vectors | Shifts in secondaries | Current pulses | Output Voltage |
|---|---|---|---|---|---|
| 3 | 7 | 127 | $20°$ | 18 | 2.30[kV] |
| 4 | 9 | 217 | $15°$ | 24 | 3.30[kV] |
| 5 | 11 | 331 | $12°$ | 30 | 4.16[kV] |
| $k$ | $2k+1$ | $12k^2+6k+1$ | $60°/k$ | $6k$ | — |

TABLE IV
FIVE-LEVEL CASCADED INVERTER SWITCHING STATES

| Output Voltage | Cell 1 | | | Cell 2 | | |
|---|---|---|---|---|---|---|
| $v_{aN}$ | $S_{11}$ | $S_{12}$ | $v_{a1}$ | $S_{22}$ | $S_{22}$ | $v_{a2}$ |
| $2V_{dc}$ | 1 | 0 | $V_{dc}$ | 1 | 0 | $V_{dc}$ |
| $V_{dc}$ | 1 | 0 | $V_{dc}$ | 0 | 0 | 0 |
| | 1 | 0 | $V_{dc}$ | 1 | 1 | 0 |
| | 0 | 0 | 0 | 1 | 0 | $V_{dc}$ |
| | 1 | 1 | 0 | 1 | 0 | $V_{dc}$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 1 | 1 | 0 |
| | 1 | 1 | 0 | 0 | 0 | 0 |
| | 1 | 1 | 0 | 1 | 1 | 0 |
| | 1 | 0 | $V_{dc}$ | 0 | 1 | $-V_{dc}$ |
| | 0 | 1 | $-V_{dc}$ | 1 | 0 | $V_{dc}$ |
| $-V_{dc}$ | 0 | 1 | $-V_{dc}$ | 1 | 1 | 0 |
| | 0 | 1 | $-V_{dc}$ | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 1 | $-V_{dc}$ |
| | 1 | 1 | 0 | 0 | 1 | $-V_{dc}$ |
| $-2V_{dc}$ | 0 | 1 | $-V_{dc}$ | 0 | 1 | $-V_{dc}$ |

pulses, both leading to output- and input-quality improvements, respectively.

*2) Multilevel Output-Voltage Generation:* Consider the inverter side of the power cells presented in Figs. 14 and 15. The switching state of one cell $S_k$ is determined by the logical value of two signals $(S_{k1}, S_{k2})$, which can be "1" and "0" representing the "ON" and "OFF" state of each switch, respectively. This leads to four different binary combinations that generate three different output voltages $+V_{dc}$, zero, and $-V_{dc}$. Since the cells are connected in series, the total inverter output voltage of one phase $x$ for an inverter with $k$ cells is given by

$$v_{xN} = \sum_{y=1}^{k} v_{xy} = \sum_{y=1}^{k} V_{dc}(S_{y1} - S_{y2}), \qquad x = \{a, b, c\}$$

(3)

where $k$ the number of power cells per phase, and $V_{dc}$ is the dc-link voltage of each cell.

The different output-voltage levels can be determined by replacing in (3) all the possible binary combinations of the switching states of each cell, obtaining in this way the inverter switching table. An example for one phase of a two-cell five-level CHB inverter is presented in Table IV.

Note that there is more than one switching state for some voltage levels (this is called inverter-output level redundancy), and this redundancy increases proportionally with the number of levels. These extra degrees of freedom can be used for control purposes.

More recently, CHB multilevel inverters with unequal dc-source, also known as hybrid or asymmetric CHB inverters, have been introduced [62]–[65]. Basically, the power circuit is very similar to the regular CHB shown in Fig. 15, the difference

is that the isolated dc sources have different values. When choosing unequal dc sources, some switching-state redundancies are avoided, and more different output-voltage levels are generated with the same amount of power cells. This reduces the size and cost of the converter and improves reliability since less semiconductors and capacitors are employed. An additional advantage is that the converter can be controlled appropriately to reduce the switching losses, which is very important in high-power applications. The main drawback is the fact that the modularity of the converter is lost, since the different power ratings of the cells force special design for each power cell (even different power-device families could be needed). In addition, no input-current harmonic cancellation can be achieved like in the equally fed case, since the power asymmetry disables the multipulse rectifier and transformer function.

The relation between the dc sources that leads to more output levels is to scale them in powers of three

$$\begin{bmatrix} V_1 & V_2 & \dots & V_k \end{bmatrix}^T = V_{dc} \cdot \begin{bmatrix} 3^0 & 3^1 & \dots & 3^{(k-1)} \end{bmatrix}^T \quad (4)$$

where $V_1, V_2, \dots, V_k$ are the dc-source voltages of the different power cells, and $V_{dc}$ the smallest dc-source voltage. This asymmetry produces $3^k$ different voltage levels; for example, a four-cell converter can generate 81 voltage levels, compared to the nine voltage levels generated with a four-cell CHB with equal dc sources. The multilevel-waveform generation for a two-cell nine-level inverter is shown in Fig. 16, and the corresponding switching states are listed in Table V.

Note how the large power cells commutates only a few times per cycle. Since the small power cells manage only 15% of the total power, a great reduction in switching losses is achieved [66], [67].

Another popular relation is to scale the dc sources in powers of two, which generates $2^{(k+1)} - 1$ different voltage levels. This reduces the number of output-voltage levels as compared to powers of three; however, it introduces some redundancies that can be used to reduce the switching transitions between levels, hence improving the converter efficiency.

Depending on the voltage relation and on the modulation index, this topology will present regenerative-power flow in the small power cells, even if the inverter, as a whole, is in motoring mode. This problem can be addressed by using a chopper circuit to keep the desired dc-source voltage (not efficient solution) or by using an AFE instead of the diode rectifier [68].

*3) Modulation Methods:* The three modulation techniques mentioned for the NPC topology can also be implemented for the CHB; however, they present some drawbacks that makes them not the preferred for this inverter. Level-shifted PWM and multilevel SVM produce an uneven usage of the different power cells of the CHB; this affects the power distribution among the cells, reducing the effectiveness of the multipulse rectifier and transformer, which leads to no current-harmonic reduction at the input. However, these methods can be considered when using an AFE rectifier at the input instead of the diode multipulse rectifier, since the input current can be controlled at will. Finally, SHE is slightly modified and referred as staircase modulation for CHB, which will be presented in
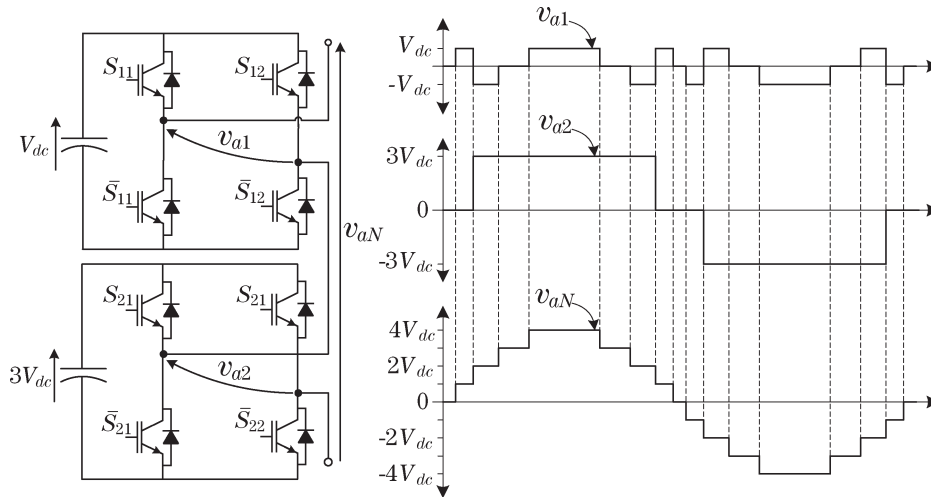
Fig. 16.   Nine-level asymmetric CHB inverter and output-voltage generation.

TABLE V
NINE-LEVEL CHB WITH UNEQUAL DC-SOURCES SWITCHING STATES

| Output Voltage | Cell 1 | | | Cell 2 | | |
|---|---|---|---|---|---|---|
| $v_{aN}$ | $S_{11}$ | $S_{12}$ | $v_{a1}$ | $S_{22}$ | $S_{22}$ | $v_{a2}$ |
| $4V_{dc}$ | 1 | 0 | $V_{dc}$ | 1 | 0 | $3V_{dc}$ |
| $3V_{dc}$ | 0 | 0 | 0 | 1 | 0 | $3V_{dc}$ |
|  | 1 | 1 | 0 | 1 | 0 | $3V_{dc}$ |
| $2V_{dc}$ | 0 | 1 | $-V_{dc}$ | 1 | 0 | $3V_{dc}$ |
| $V_{dc}$ | 1 | 0 | $V_{dc}$ | 0 | 0 | 0 |
|  | 1 | 0 | $V_{dc}$ | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|  | 0 | 0 | 0 | 1 | 1 | 0 |
|  | 1 | 1 | 0 | 0 | 0 | 0 |
|  | 1 | 1 | 0 | 1 | 1 | 0 |
| $-V_{dc}$ | 0 | 1 | $-V_{dc}$ | 1 | 1 | 0 |
|  | 0 | 1 | $-V_{dc}$ | 0 | 0 | 0 |
| $-2V_{dc}$ | 1 | 0 | $V_{dc}$ | 0 | 1 | $-3V_{dc}$ |
| $-3V_{dc}$ | 1 | 1 | 0 | 0 | 1 | $-3V_{dc}$ |
|  | 0 | 0 | 0 | 0 | 1 | $-3V_{dc}$ |
| $-4V_{dc}$ | 0 | 1 | $-V_{dc}$ | 0 | 1 | $-3V_{dc}$ |

this section together with the other established control and modulation techniques.

Phase-shifted PWM (PS-PWM) is the natural PWM method for CHB [58], mainly due to the modularity of this topology. Each cell is modulated independently using unipolar PWM with the same reference signal. A phase shift is introduced across all the carrier signals of each cell in order to produce the stepped multilevel waveform. The lowest output-voltage distortion is achieved with $180°/k$ phase shifts between the carriers, for a $k$-cell inverter. This operating principle is shown for a seven-level example in Fig. 17. Note how the inverter-output voltage has $k$ times the fundamental component of each cell. In addition, the frequency of the inverter-output-voltage switching pattern is $k$ times the cell switching frequency, since the phase shift introduces a multiplicative effect. This is very useful, since the device switching frequency (hence, the switching losses) is $k$ times lower than the apparent switching frequency perceived by the load. This means that, for the same output switching frequency, phase-shifted produces $k$ times less switching losses as compared to level-shifted. However, level-shifted leads to less distorted line voltages since all the carriers are in phase [69].
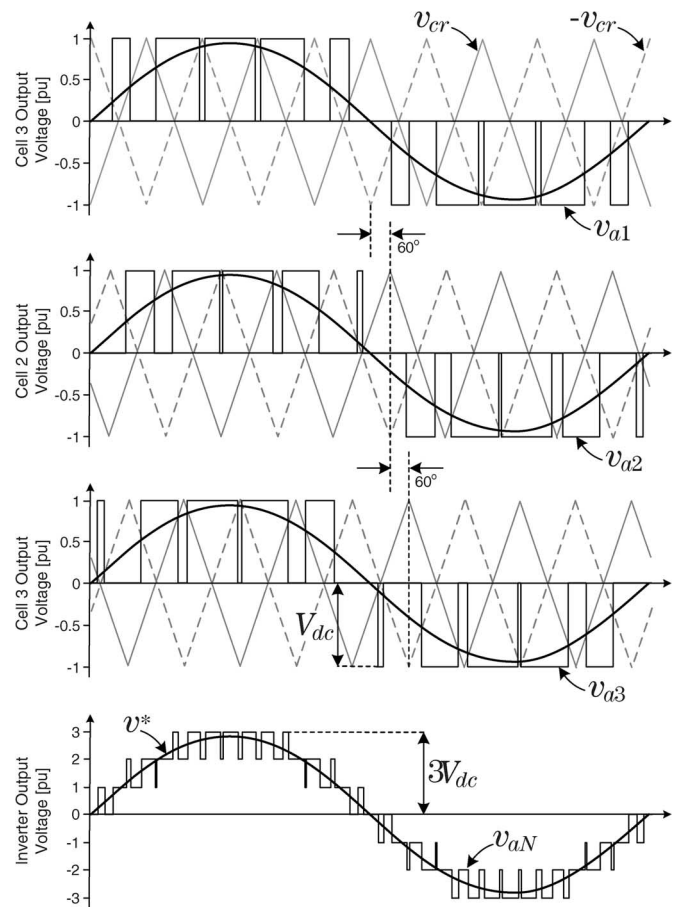


Fig. 17.   Three-cell (seven-level) PS-PWM waveform generation.

Since all the cells are controlled with the same reference and the same carrier frequency, the power is evenly distributed among the cells, achieving input-current harmonic reduction owing to the multipulse transformer–rectifier system [58].

For low-switching-frequency applications, the staircase modulation is used. The basic idea of this technique is to connect each cell of the inverter at specific angles to generate the multilevel output waveform, producing only a minimum of necessary commutations [70]. The operating principle is shown
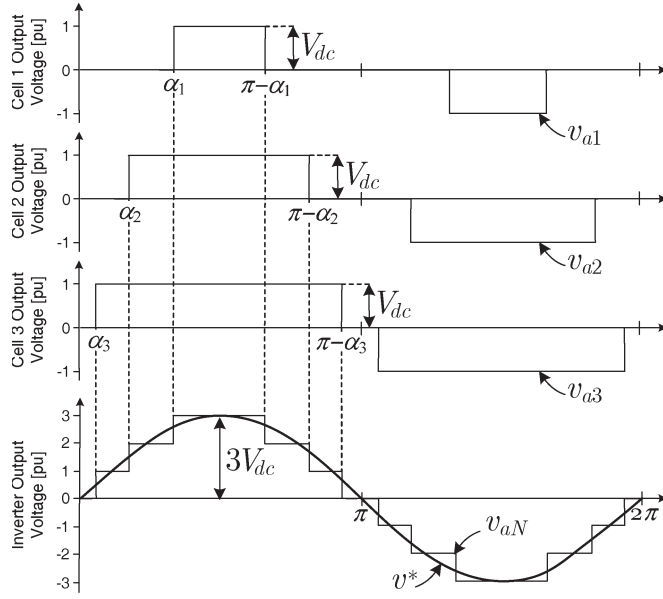
Fig. 18. Seven-level staircase modulation.

in Fig. 18; note that only one angle needs to be determined per power cell. These angles can be computed using the same principles of SHE. The output voltage, for the seven-level case shown in Fig. 18, can be expressed in Fourier series as

$$v_{aN} = \frac{4V_{\text{dc}}}{\pi} \sum_{n=1}^{\infty} \frac{1}{n}$$
$$\times \left\{ \cos(n\alpha_1) + \cos(n\alpha_2) + \cos(n\alpha_3) \right\} \sin(n\omega t) \quad (5)$$

where $n$ is uneven, and $0 \leq \alpha_3 < \alpha_2 < \alpha_1 \leq \pi/2$.

From (5), three coefficients of the Fourier series can be forced to a desired value; naturally, the first coefficient correspond to the fundamental component and is set to the desired modulation index while, usually, the fifth and seventh coefficient are set to zero (for fifth- and seventh-harmonic elimination)

$$M \cdot \frac{\pi}{4} = \cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3)$$
$$0 = \cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3)$$
$$0 = \cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) \quad (6)$$

where $M = \hat{v}_{aN}^f/(k \cdot V_{\text{dc}})$ is the modulation index, defined by the desired peak amplitude for the fundamental component of the output voltage $(\hat{v}_{aN}^f)$ and the number of cells, $k = 3$ for this example.

The main advantage, like in SHE, is that the converter switches very few times per cycle, reducing the switching losses to a minimum. In addition, low-order harmonics are eliminated, facilitating the output-filter design. However, also like SHE, this method needs important offline calculations to compute the angles for a variety of modulation indexes and is therefore not very suited for highly dynamic systems.

Another low-switching-frequency methods is multilevel space-vector control (MSVC) [71], where the basic idea is to take advantage of converters with high number of voltage

vectors (for inverters of at least seven levels) by simply approximating the reference to the closest voltage vector that can be generated. The nearest voltage-level (NVL) control is somehow the time-domain counterpart of MSVC. Basically, the same principle is applied by selecting the NVL that can be generated by the inverter to the desired output-voltage reference [67], [68]. These modulation methods are not effective for converters with a reduced number of levels, since the approximation error becomes relevant.

The hybrid modulation is particularly conceived for the CHB with unequal dc sources. The basic idea is to take advantage of the different power rates among the cells to reduce switching losses and improve the converter efficiency. For example, from Fig. 16, it is shown that the high-power cell will turn on and off only one time during a half reference cycle. The unmodulated part left by the square shape of the high-power cell output is then generated by the next power cell and so on, until the final unmodulated parts of the reference are modulated at high switching frequency (with unipolar sinusoidal PWM) by the smallest power cell. This completes the generation of a multilevel stepped waveform with a high-frequency component (similar to multicarrier-based PWM) but with the difference that fewer switching losses are produced to achieve it.

The aforementioned operating principle is shown in Fig. 19 for a three-cell converter. Note that the high-voltage cell commutates when the reference reaches a specific voltage level $\pm h_3$. This level has to be selected in a way that the unmodulated part can be generated by the lower power cells to avoid overmodulation. If we consider that the maximum amplitude that can be generated by the inverter is $V_1 + V_2 + V_3$, the only possibility to avoid overmodulation is that the unmodulated part does not exceed the total voltage left for the low-power cells of the inverter, i.e., $h_3 = V_1 + V_2$. Hence, $h_2 = V_1$ for the second power cell. Finally, the last unmodulated part is generated by the low-power cell with traditional unipolar PWM.

The relation between dc sources that gives a maximum of different output levels and that is possible to use with this modulation method is

$$\begin{bmatrix} V_1 & V_2 & V_3 \end{bmatrix}^{\text{T}} = V_{\text{dc}} \cdot \begin{bmatrix} 1 & 2 & 6 \end{bmatrix}^{\text{T}}. \quad (7)$$

Note that the optimal $(V_1, V_2, V_3) = (V_{\text{dc}}, 3\,V_{\text{dc}}, 9\,V_{\text{dc}})$ asymmetry is not suitable for this modulation, since $h_3 = 4\,V_1$, which will lead to an unmodulated reference for the second cell of $5\,V_{\text{dc}}$ of amplitude, which cannot be covered completely by the smaller power cells.

Typical output waveforms using this modulation are shown in Fig. 20, together with the inverter total output voltage. Note that the output has 19 different voltage levels given by all the possible combinations of the series connection of $(+V_1, 0, -V_1)$, $(+2\,V_1, 0, -2\,V_1)$, and $(+6\,V_1, 0, -6\,V_1)$.

## C. Flying Capacitor

*1) Topology Description:* The FC-VSC topology was proposed about 15 years ago [23], [72]. Currently, the four-level FC-VSC (4L FC-VSC) is produced by one manufacturer of industrial MV drives. The circuit configuration of the topology
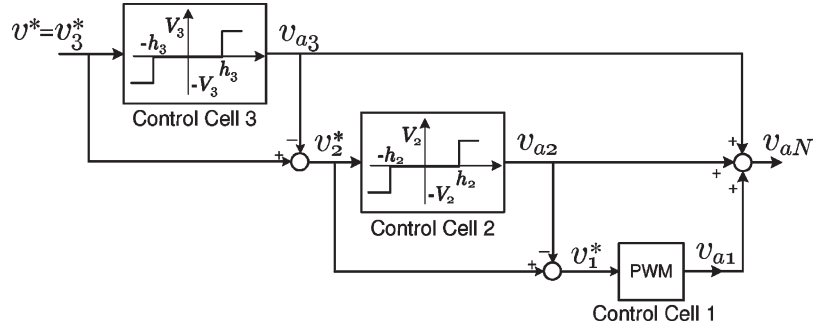
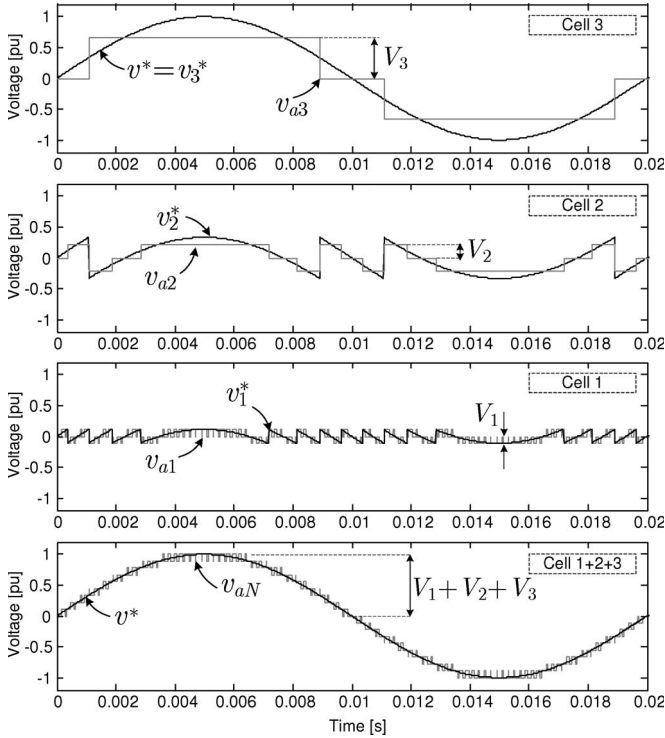Fig. 19.   Hybrid modulation for CHB with unequal dc sources.



Fig. 20.   Output voltages for CHB with unequal dc sources for hybrid modulation.



Fig. 21.   Circuit configuration of 4L FC-VSC.

is depicted in Fig. 21. This topology can be presented in a more modular way, also known as multicell, as shown in Fig. 22.

One converter phase leg consists of a series connection of three commutation cells. The nominal voltages of the FCs, $C_{x1}$ and $C_{x2}$, are $v_{cx1} = 2/3V_{dc}$ and $v_{cx2} = 1/3V_{dc}$, respectively. Meynard and Foch [73] describe a simple scheme to charge the FCs to the desired voltage level during the start-up procedure of the converter. The switching states of one phase of the 4L FC-VSC are shown in Table VI. The switches of each commutation cell (e.g., $S_{x1}$ for the upper switch position and $\overline{S}_{x1}$ for the lower switch position) commutate the phase current to the upper and the lower switch positions, respectively. The corresponding commutation voltage per cell is equivalent to one third of the dc-voltage ($V_{\text{com}} = V_{\text{dc}}/3$). Redundant switch states with a different polarity of the FC currents are used to balance the voltages across the FCs. Combining all three phases, the 4L FC-VSC features $n_{\text{ss}} = L^3 = 4^3 = 64$ different switching states.

*2) Modulation Methods:* As with the CHB, the preferred modulation strategy is PS-PWM, since a natural voltage
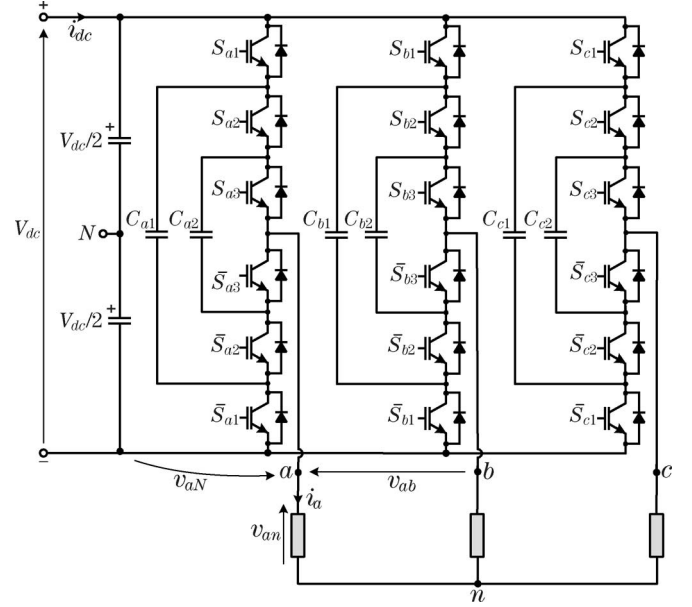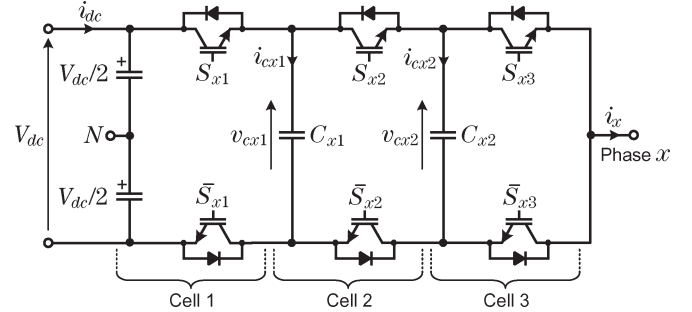


Fig. 22.   Circuit configuration of one phase leg ($x = a, b, c$) of 4L FC-VSC (multicell layout).

TABLE  VI
FOUR-LEVEL FC SWITCHING STATES (PHASE $x = a, b, c$)

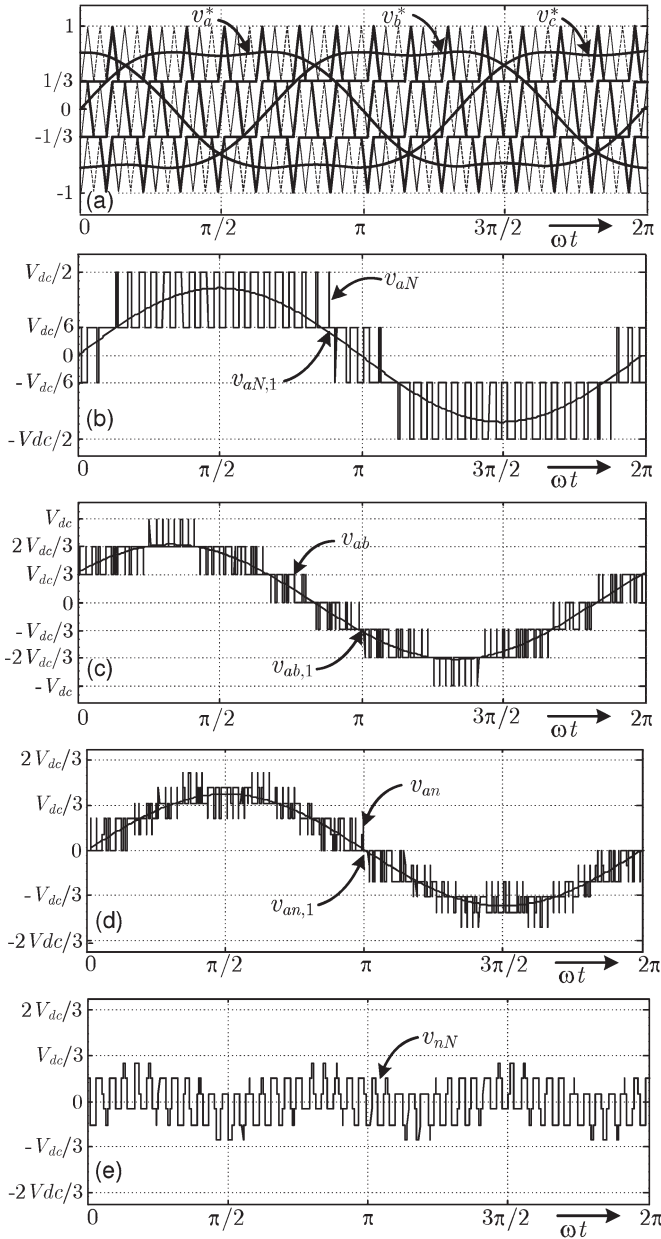| Output Voltage | Switching state | | | Capacitor current | |
|---|---|---|---|---|---|
| $v_{xN}$ | $S_{x1}$ | $S_{x2}$ | $S_{x3}$ | $i_{cx1}$ | $i_{cx2}$ |
| $V_{dc}/2$ | 1 | 1 | 1 | 0 | 0 |
| $V_{dc}/6$ | 1 | 1 | 0 | 0 | $+i_x$ |
| | 1 | 0 | 1 | $+i_x$ | $-i_x$ |
| | 0 | 1 | 1 | $-i_x$ | 0 |
| $-V_{dc}/6$ | 1 | 0 | 0 | $+i_x$ | 0 |
| | 0 | 1 | 0 | $-i_x$ | $+i_x$ |
| | 0 | 0 | 1 | 0 | $-i_x$ |
| $-V_{dc}/2$ | 0 | 0 | 0 | 0 | 0 |

Fig. 23. Waveforms of 4L FC-VSC applying a PD sine-triangle modulation with one-sixth-added third harmonics ($f_c/f_1 = 15$; $M = 0.8$).



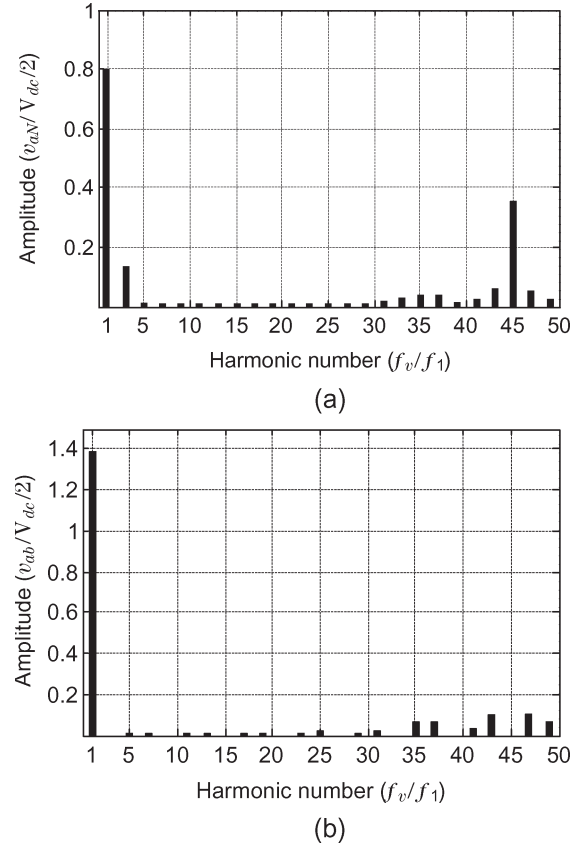Fig. 24. Voltage spectrum of 4L FC-VSC applying a PD sine-triangle modulation with one-sixth-added third harmonics ($f_c/f_1 = 15$; $M = 0.8$). (a) Phase-neutral voltage. (b) Line–line voltage.

balance of the FCs is achieved [73]. The main difference with the PS-PWM applied to CHB is that, for the FC, a $360°/k$ phase shift is introduced among the carriers for a converter with $k$ cells and that bipolar PWM is used instead of unipolar PWM. This is because the FC has two-level output voltages per cell, instead of the three-level outputs of the H-bridges. Other methods have also been presented, like a field-oriented control in combination with a PD-carrier-based sine-triangle modulation, applied to the 4L FC-VSC [74]. The waveforms for a PD sine-triangle modulation, where one sixth of third harmonics are added to the reference signals, can be appreciated in Fig. 23. To achieve a PD sine-triangle modulation with balanced capacitors, there are three $120°$ phase-shifted trapezoidal carriers in each of the three modulation bands (1 to 1/3, 1/3 to $-1/3$, and $-1/3$ to $-1$) [74], [75]. The voltage spectrum is shown in Fig. 24. Since three cells commutate the phase current

during one period of the carrier signal, the number of switching transients is increased by a factor of three in the 4L FC-VSC as compared to a 3L NPC-VSC at constant carrier frequency. Thus, the harmonic carrier bands appear at frequencies of $f_{cb} = 3 \cdot n \cdot f_c$, where $n$ is an integer ($n = 1, 2, 3, \ldots$) and $f_c$ is the frequency of the carrier signal.

*3) Latest Advances:* For the 4L FC-VSC, the extension of the converter voltage range ($v_{ll} > 4.16$ kV) is one important market driver. Keller and Jakob [76] describes the recent development of a 6-kV 4-MVA 4L FC-VSC on the basis of 6.5-kV 600-A IGBT modules.

*4) Applications:* Currently, the 4L FC-VSC is commercially available for converter voltages of 2.3, 3.3, and 4.2 kV in a power range of $S_C = 0.3-8$ MVA. The high expense of flying capacitors at low and medium switching frequencies (e.g., $f_{1cb} \leq 800-1800$ Hz) is the major disadvantage of FC topologies [25]. To enable a moderate expense of flying capacitors, typical switching frequencies of about $f_c \approx 1000$ Hz are usually applied in MV converters. Due to the resulting high switching frequency of the first carrier band of the output voltage (e.g., $f_{1cb} = 3 \cdot f_c = 3000$ Hz), the 4L FC-VSC is interesting in applications like high-speed MV drives and test benches, which require a high frequency of the fundamental output voltage and a very low-current THD, respectively.

The three multilevel topologies presented in this paper (3L NPC, 4L FC-VSC, and the CHB) have presence in the market,

and they cover different needs for different type of applications. These topologies have been compared in terms of structure, cost, and efficiency in [77]–[79].

The main drawbacks for the 3L NPC-VSC are the requirement of clamping diodes, the lack of modularity, and the unequal semiconductor-loss distribution. Furthermore, voltage-balancing problems and a reduced silicon utilization due to the increasing voltage-blocking stress of the clamping diodes are severe structural problems of diode-clamped converters with more than three levels. In contrast, the additional expense of flying capacitors, particularly at low carrier frequencies (e.g., $f_c < 800-1000$ Hz) and a high number of cells, is the main disadvantage of the FC topology.

For the CHB, the main disadvantage are the separate dc sources, usually provided by a bulky and nonstandard transformer. On the other hand, the FC and CHB have modular structures, enabling a more natural implementation of underfault operation, and design of power-electronics building blocks. The CHB is particularly attractive for reactive-power-compensation technologies since no complicated input transformer is necessary and, also, for very high-power applications since the series connection enables a natural increase of the power level of the converter. The FC has found its place in high-bandwidth applications, such as MV traction drives. Finally, the NPC has experienced a substantial market penetration in 2.3–4.16-kV applications that require a low switching frequency and high converter efficiency at a lower cost as compared to the other two topologies.

The continuous evolution and development of industrial processes comes together with an evolution of technical requirements. Therefore, despite the maturity reached by the multilevel-converter technology in terms of market solutions, there is still room for research and development of new or adapted topologies that should fulfill those particular needs, and perhaps, find their way to the industry as well. This is why, recently, many novel, hybrid, and variations of multilevel topologies have been reported [80]–[82].

## IV. FUTURE TRENDS

Substantial system advantages, such as increased availability, improved dynamic performance, extended operating range, reduced line harmonics, and an adjustable power factor at the point of common coupling, are the reasons to explain why VSCs have replaced thyristor-based converters in a wide range of applications.

The increase of the converter power of multilevel VSCs will enable a further replacement of thyristor-based CCVs and LCIs in the future. Availability, reliability, efficiency, size, and costs are key requirements for this development.

To cover a wide range of applications with different technical requirements, the modularization of the power part and of the control hardware and software is a further technological-development trend.

Finally, innovations in the field of high-power semiconductors and converter topologies, including modulation schemes and redundancy options, will strongly influence the future development of MV high-power converters.

## V. CONCLUSION

This paper presents a review of the state of the art and developments of 2L and multilevel VSCs for high-power-drive applications. The analyzed operating principles, relevant characteristics, established modulation methods, and latest developments of these converters show that all described topologies (2L VSCs, NPC, CHB, and FC multilevel VSCs) feature specific technical advantages and disadvantages which justify their existence on the market. The growing market size and increasing technical requirements of MV high-power drives for a large variety of applications will require substantial efforts and research in the future.

## REFERENCES

[1] S. Rizzo and N. Zargari, "Medium voltage drives: What does the future hold?" in *Proc. 4th IPEMC*, 2004, pp. 82–89.

[2] H. Brunner, M. Hieholzer *et al.*, "Progress in development of the 3.5 kV high voltage IGBT/diode chipset and 1200 A module applications," in *Proc. IEEE Int. Symp. Power Semicond. Devices IC's*, 1997, pp. 225–228.

[3] P. K. Steimer, H. E. Gruning *et al.*, "IGCT—A new emerging technology for high power, low cost inverters," *IEEE Ind. Appl. Mag.*, vol. 5, no. 4, pp. 12–18, Jul./Aug. 1999.

[4] W. C. Rossmann and R. G. Ellis, "Retrofit of 22 pipeline pumping stations with 3000-hp motors and variable-frequency drives," *IEEE Trans. Ind. Appl.*, vol. 34, no. 1, pp. 178–186, Jan./Feb. 1998.

[5] R. Menz and F. Opprecht, "Replacement of a wound rotor motor with an adjustable speed drive for a 1400 kW kiln exhaust gas fan," in *Proc. 44th IEEE IAS Cement Ind. Tech. Conf.*, 2002, pp. 85–93.

[6] B. P. Schmitt and R. Sommer, "Retrofit of fixed speed induction motors with medium voltage drive converters using NPC three-level inverter high voltage IGBT based topology," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2001, pp. 746–751.

[7] S. Bernert, "Recent developments of high power converters for industry and traction applications," *IEEE Trans. Power Electron.*, vol. 15, no. 6, pp. 1102–1117, Nov. 2000.

[8] H. Okayama, M. Koyama *et al.*, "Large capacity high performance 3-level GTO inverter system for steel main rolling mill drives," in *Conf. Rec. IAS Annu. Meeting*, 1996, pp. 174–179.

[9] J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galvan, R. C. Portillo Guisado, M. A. M. Prats, J. I. Leon, and N. Moreno-Alfonso, "Power-electronic systems for the grid integration of renewable energy sources: A survey," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1002–1016, Jun. 2006.

[10] S. Alepuz, S. Busquets-Monge, J. Bordonau, J. Gago, D. Gonzalez, and J. Balcells, "Interfacing renewable energy sources to the utility grid using a three-level inverter," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1504–1511, Oct. 2006.

[11] R. C. Portillo, M. M. Prats, J. I. Leon, J. A. Sanchez, J. M. Carrasco, E. Galvan, and L. G. Franquelo, "Modeling strategy for back-to-back three-level converters applied to high-power wind turbines," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1483–1491, Oct. 2006.

[12] J. Dixon, L. Moran, R. Rodriguez, and E. Domke, "Reactive power compensation technologies: State-of-the-art review," *Proc. IEEE*, vol. 93, no. 12, pp. 2144–2164, Dec. 2005.

[13] Y. Cheng, C. Qian, M. L. Crow, S. Pekarek, and S. Atcitty, "A comparison of diode-clamped and cascaded multilevel converters for a STATCOM with energy storage," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1512–1521, Oct. 2006.

[14] M. E. Ortuzar, R. E. Carmi, J. W. Dixon, and L. Moran, "Voltage-source active power filter based on multilevel converter and ultracapacitor DC link," *IEEE Trans. Ind. Electron.*, vol. 53, no. 2, pp. 477–485, Apr. 2006.

[15] H. Akagi, "Large static converters for industry and utility applications," *Proc. IEEE*, vol. 89, no. 6, pp. 976–983, Jun. 2001.

[16] J. K. Steinke and P. K. Steimer, "Medium voltage drive converter for industrial applications in the power range from 0.5 MW to 5 MW based on a three-level converter equipped with IGCTs," in *Proc. IEE Seminar PWM Medium Voltage Drives*, 2000, pp. 6/1–6/4.

[17] N. Zargari and S. Rizzo, "Medium voltage drives in industrial applications," in *Proc. Tech. Seminar, IEEE Toronto Section*, Nov. 2004, CD-ROM.

[18] S. Malik and D. Kluge, "ACS1000 world's first standard AC drive for medium-voltage applications," *ABB Rev.*, no. 2, pp. 4–11, 1998.

[19] T. Podlesak, D. Katsis, P. Wheeler, J. Clare, L. Empringham, and M. Bland, "A 150-kVA vector-controlled matrix converter induction motor drive," *IEEE Trans. Ind. Appl.*, vol. 41, no. 3, pp. 841–847, May/Jun. 2005.

[20] R. Emery and J. Eugene, "Harmonic losses in LCI-fed synchronous motors," *IEEE Trans. Ind. Appl.*, vol. 38, no. 4, pp. 948–954, Jul./Aug. 2002.

[21] J. Rodríguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[22] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.

[23] T. Meynard and H. Foch, "Multi-level choppers for high voltage applications," *Eur. Power Electron. J.*, vol. 2, no. 1, pp. 45–50, Mar. 1992.

[24] M. Marchesoni, M. Mazzucchelli, and S. Tenconi, "A non conventional power converter for plasma stabilization," in *Proc. Power Electron. Spec. Conf.*, 1988, pp. 122–129.

[25] S. Bernet, "State of the art and developments of medium voltage converters—An overview," *Prz. Elektrotech. (Electrical Review)*, vol. 82, no. 5, pp. 1–10, May 2006.

[26] J. Holtz, "Pulsewidth modulation for electronic power conversion," *Proc. IEEE*, vol. 82, no. 8, pp. 1194–1214, Aug. 1994.

[27] R. H. Baker, "Bridge converter circuit," U.S. Patent 4 270 163, May 26, 1981.

[28] A. Mertens, M. Bruckmann, and R. Sommer, "Medium voltage inverter using high-voltage IGBTs," in *Proc. EPE Conf. Rec.*, Lausanne, Switzerland, 1999. CD-ROM.

[29] M. Beuermann, M. Hiller, and R. Sommer, "Stromrichterschaltungen für Mittelspannung und deren Leistungshalbleiter für den Einsatz in Industriestromrichtern," in *Proc. VDE-ETG Conf.: Power Semicond. Appl.*, Bad Nauheim, Germany, 2006, pp. 151–160.

[30] P. K. Steimer, J. K. Steinke, H. E. Grüning, and S. Conner, "A reliable, interface-friendly medium voltage drive based on the robust IGCT and DTC technologies," in *Conf. Rec. IAS Annu. Meeting*, Phoenix, AZ, 1999, pp. 1505–1512.

[31] C. Meyer, C. Romaus, and R. W. DeDoncker, "Five level neutral-point clamped inverter for a dynamic voltage restorer," in *Proc. Eur. Conf. Power Electron. Appl.*, Sep. 2005, pp. 11–14.

[32] P. Lauttamus and H. Tuusa, "Comparison of five-level voltage-source inverter based STATCOMs," in *Proc. PCC*, Nagoya, Japan, Apr. 2–5, 2007, pp. 659–666.

[33] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel PWM method: A theoretical analysis," *IEEE Trans. Power Electron.*, vol. 7, no. 3, pp. 497–505, Jul. 1992.

[34] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858–867, Aug. 2002.

[35] T. Brückner, "The active NPC converter for medium-voltage drives," Ph.D. dissertation, Dresden Univ. Technol., Dresden, Germany, 2006.

[36] N. Celanovic and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 637–641, Mar./Apr. 2001.

[37] A. K. Gupta and A. M. Khambadkone, "A space vector PWM scheme for multilevel inverters based on two-level space vector PWM," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1631–1639, Oct. 2006.

[38] M. M. Prats, L. G. Franquelo, R. C. Portillo, J. I. Leon, E. Galván, and J. M. Carrascco, "A 3-D space vector modulation generalized algorithm for multilevel converters," *IEEE Power Electron. Lett.*, vol. 1, no. 4, pp. 110–114, Dec. 2003.

[39] L. G. Franquelo, M. M. Prats, R. C. Portillo, J. I. Leon, M. A. Perales, J. M. Carrasco, E. Galvan, and J. L. Mora, "Three-dimensional space-vector modulation algorithm for four-leg multilevel converters using abc coordinates," *IEEE Trans. Ind. Electron.*, vol. 53, no. 2, pp. 458–466, Apr. 2006.

[40] L. Li, D. Czarkowski, Y. Liu, and P. Pillay, "Multilevel selective harmonic elimination PWM technique in series-connected voltage inverters," in *Conf. Rec. IAS Annu. Meeting*, Oct. 1998, pp. 1454–1461.

[41] B. Ozpineci, L. Tolbert, and J. Chiasson, "Harmonic optimization of multilevel converters using genetic algorithms," *IEEE Power Electron. Lett.*, vol. 3, no. 3, pp. 92–95, Sep. 2005.

[42] Z. Du, L. Tolbert, and J. Chiasson, "Active harmonic elimination for multilevel converters," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 459–469, Mar. 2006.

[43] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level-neutral-point-clamped voltage source PWM inverters," *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 242–249, Mar. 2000.

[44] S. Ogasawara and H. Akagi, "Analysis of variation of neutral point potential in neutral-point-clamped voltage source PWM inverters," in *Conf. Rec. IAS Annu. Meeting*, Toronto, ON, Canada, 1993, pp. 965–970.

[45] C. Newton and M. Sumner, "Neutral point control for multi-level inverters: Theory, design, and operational limitations," in *Conf. Rec. IAS Annu. Meeting*, New Orleans, LA, 1997, pp. 1136–1343.

[46] J. E. Espinoza, J. R. Espinoza, and L. A. Moran, "A systematic controller-design approach for neutral-point-clamped three-level inverters," *IEEE Trans. Ind. Electron.*, vol. 52, no. 6, pp. 1589–1599, Dec. 2005.

[47] A. Bendre, G. Venkataramanan, D. Rosene, and V. Srinivasan, "Modeling and design of a neutral-point voltage regulator for a three-level diode-clamped inverter using multiple-carrier modulation," *IEEE Trans. Ind. Electron.*, vol. 53, no. 3, pp. 718–726, Jun. 2006.

[48] F. Blaschke, "The principle of field orientation as applied to the transvector closed-loop control system for rotating-field machines," *Siemens Rev.*, vol. 34, pp. 217–220, 1972.

[49] K. Hasse, "Drehzahlregelverfahren für schnelle Umkehrantriebe mit stromrichtergespiesten Asynchron-Kurzschlußläufermotoren," *Regelungstechnik*, vol. 20, pp. 60–66, 1972.

[50] I. Takahashi and T. Noguchi, "A new quick-response and high-efficiency strategy of an induction motor," *IEEE Trans. Ind. Appl.*, vol. IA-22, no. 7, pp. 820–827, 1986.

[51] M. Depenbrock, "Direct self control (DSC) of inverter fed induction machine," *IEEE Trans. Power Electron.*, vol. 3, no. 4, pp. 420–429, May/Jun. 1988.

[52] M. Malinowski, M. Kazmierkowski, and A. Trzynadlowski, "Comparative study of control techniques for PWM rectifiers in AC adjustable speed drives," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1390–1396, Nov. 2003.

[53] R. D. Klug and N. Klaassen, "High power medium voltage drives—Innovations, portfolio, trends," in *Proc. Conf. Rec. EPE*, Dresden, Germany, 2005, CD-ROM.

[54] S. Bernet, E. Carroll, P. Streit, O. Apeldoorn, P. Steimer, and S. Tschirley, "Design, test and characteristics of 10-kV integrated gate commutated thyristors," *IEEE Ind. Appl. Mag.*, vol. 11, no. 2, pp. 53–61, Mar./Apr. 2005.

[55] A. Nagel, S. Bernet, P. K. Steimer, and O. Apeldoorn, "A 24 MVA inverter using IGCT series connection for medium voltage applications," in *Conf. Rec. IAS Annu. Meeting*, Chicago, IL, 2001, pp. 867–870.

[56] T. Brückner, S. Bernet, and H. Güldner, "The active NPC converter and its loss-balancing control," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 855–868, Jun. 2005.

[57] P. Steimer, O. Apeldoorn, B. Ødegård, S. Bernet, and T. Brückner, "Very high power IGCT PEBB technology," in *Proc. IEEE PESC*, Recife, Brazil, 2005, pp. 1–7.

[58] P. Hammond, "A new approach to enhance power quality for medium voltage AC drives," *IEEE Trans. Ind. Appl.*, vol. 33, no. 1, pp. 202–208, Jan./Feb. 1997.

[59] R. Osman, "A medium-voltage drive utilizing series-cell multilevel topology for outstanding power quality," in *Conf. Rec. IAS Annu. Meeting*, 1999, pp. 2662–2669.

[60] J. Rodríguez, J. Dixon, J. Espinoza, J. Pontt, and P. Lezana, "PWM regenerative rectifiers: State of the art," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 5–22, Feb. 2005.

[61] P. Lezana, C. A. Silva, J. Rodriguez, and M. A. Perez, "Zero-steady-state-error input-current controller for regenerative multilevel converters based on single-phase cells," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 733–740, Apr. 2007.

[62] O. M. Mueller and J. N. Park, "Quasi-linear IGBT inverter topologies," in *Proc. APEC*, Feb. 1994, pp. 253–259.

[63] S. Mariethoz and A. Rufer, "Design and control of asymmetrical multi-level inverters," in *Proc. IECON*, Sevilla, Spain, Nov. 2002, pp. 840–845.

[64] C. Rech and J. R. Pinheiro, "Line current harmonics reduction in multipulse connection of asymmetrically loaded rectifiers," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 640–652, Jun. 2005.

[65] C. Rech and J. R. Pinheiro, "Hybrid multilevel converters: Unified analysis and design considerations," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 1092–1104, Apr. 2007.

[66] J. Dixon and L. Moran, "High-level multistep inverter optimization using a minimum number of power transistors," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 330–337, Mar. 2006.

[67] M. Pérez, J. Rodríguez, J. Pontt, and S. Kouro, "Power distribution in hybrid multi-cell converter with nearest level modulation," in *Proc. IEEE ISIE*, Vigo, Spain, Jun. 4–7, 2007, pp. 736–741.

[68] S. Kouro, R. Bernal, C. Silva, J. Rodríguez, and J. Pontt, "High performance torque and flux control for multilevel inverter fed induction motors," in *Proc. 32nd Annu. Conf. IEEE IECON*, Paris, France, Nov. 2006, pp. 805–810.

[69] D. G. Holmes and T. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. Piscataway, NJ: IEEE Press, 2003.

[70] B. Wu, *High-Power Converters and AC Drives*. Piscataway, NJ: IEEE Press, 2006.

[71] J. Rodríguez, L. Morán, P. Correa, and C. Silva, "A vector control technique for medium-voltage inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 882–888, Aug. 2002.

[72] T. A. Meynard and H. Foch, "Electronic device for electrical energy conversion between a voltage source and a current source by means of controllable switching cells," U.S. Patent 5 737 201, Apr. 7, 1998. (priority Jul. 1991).

[73] T. A. Meynard and H. Foch, "Electronic device for electrical energy conversion between a voltage source and a current source by means of controllable switching cells," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 955–964, Oct. 2002.

[74] S.-G. Lee, D.-W. Kang, Y.-H. Lee, and D.-S. Hyun, "The carrier based PWM method for voltage balancing of flying capacitor multilevel inverter," in *Proc. IEEE PESC*, Vancouver, BC, Canada, Jun. 2001, vol. 1, pp. 126–131.

[75] B. McGrath, T. Meynard, and G. Holmes, "Optimal modulation of flying capacitor and stacked multicell converters using a state machine decoder," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 508–516, Mar. 2007.

[76] C. Keller and R. Jakob, "Low power converters for high output voltages" in *Proc. Conf. Rec. EPE*, Dresden, Germany, 2005, CD-ROM.

[77] D. Krug, M. Malinowski, and S. Bernet, "Design and comparison of medium voltage multi-level converters for industry applications," in *39th Conf. Rec. IAS Annu. Meeting*, Seattle, WA, Oct. 2004, vol. 2, pp. 781–790.

[78] S. Bernet, D. Krug, S. Fazel, and K. Jalili, "Design and comparison of 4.16 kV neutral point clamped, flying capacitor and series connected H-bridge multi-level converters," in *40th Conf. Rec. IAS Annu. Meeting*, Hong Kong, Oct. 2005, pp. 121–128.

[79] R. Teichmann, M. Malinowski, and S. Bernet, "Evaluation of three-level rectifiers for low-voltage utility applications," *IEEE Trans. Ind. Electron.*, vol. 52, no. 2, pp. 471–481, Apr. 2005.

[80] J. Huang and K. A. Corzine, "Extended operation of flying capacitor multilevel inverters," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 140–147, Jan. 2006.

[81] A. Abu, S. Ming-yan, and W. K. Tian, "A hybrid capacitor-clamp cascade multilevel converter," in *Proc. IECON*, Paris, France, Nov. 2006, pp. 2031–2036.

[82] P. Lezana and J. Rodríguez, "Mixed multicell cascaded multilevel inverter," in *Proc. IEEE ISIE*, Jun. 4–7, 2007, pp. 509–514.

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