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1.	Authors:	Neha Thombare, Pallavi Deshmukh, Simantini Patil, Shailesh Jain	
	Paper Title:	Personalized Image Search	
	<p>Abstract: Personalized Search is a feature in which when a user is logged into a account, all of his or her searches on Personal Search are recorded into Web History. Then, when a user performs a search, the search results are not only based on the relevancy of each web page to the search term, but the service also takes into account what websites the user previously visited through search results to determine which search results to determine for future searches, to provide a more personalized experience. The feature only takes effect after the user has performed several searches, so that it can be calibrated to the user's tastes. Social sharing websites like facebook, twitter, YouTube they are allowing user to comment, tag, like and unlike the shared documents or images. Rapid Increase in the search services for social websites has been developed.</p> <p>Keywords: Personalized Search, Tagging, Topic Model.</p> <p>References:</p> <ol style="list-style-type: none">1. Learn to Personalized Image Search from the Photo Sharing Websites Jitao Sang, Changsheng Xu, Senior Member, IEEE, Dongyuan Lu2. B. Smyth, "A community-based approach to personalizing web search,"Computer, vol. 40, no. 8, pp. 42–50, 2007.3. Personalized Search on Flickr based on Searcher's Preference Prediction Dongyuan Lu, Quidan Li		1-3
2.	Authors:	Y.Shekar, B. Vasunayak, J. Sunil Kumar, A. Sanyasi Rao, Fathima Shireen	
	Paper Title:	Cryptographic Algorithms Implementation on RISC Processor	
	<p>Abstract: Security is one of the most important features in data communication. Cryptographic algorithms are mainly used for this purpose to obtain confidentiality and integrity of data in communication. Implementing a cryptographic algorithm on a general purpose processor it results lower throughput and larger power consumption. In this work we propose processor architecture to perform the cryptographic algorithms and also it speed up the encryption and decryption process of data. This processor will perform the cryptographic operations as like general instructions in GPP. The data size of this processor is 32-bit. The architecture of the processor designed using Verilog HDL.</p> <p>Keywords: Cryptographic Algorithms, GPP, Verilog.</p> <p>References:</p> <ol style="list-style-type: none">1. Jun-hong chen "A High-Performance Unified Field Reconfigurable Cryptographic Processor". IEEE-20102. Nima Karimpour Darav "CIARP: Crypto Instruction-aware RISC Processor.IEEE-2012"3. Antonio H. Zavala "RISC-Based Architecture for Computer Hardware Instruction" IEEE-20114. "Data Encryption Standard" 1999 october 25.5. "Advance Encryption Standard" November 26 20016. Imyong Lee, Dongwook Lee, Kiyoun Choi, "ODALRISC: A Small, Low power and Configurable 32-bit RISC processor," International SOC design Conference 2008.7. Wayne Wolf, FPGA Based System Design, Prentice Hall, 2005.8. National Institute of Standards and Technology (NIST), "Advanced Encryption Standard (AES), (FIP PUB 197)", November 26, 2001, http://csrc.nist.gov/publications/.9. Atri. Rudra, Pradeep k. Dubey, Charanjit S.Jutla, Vijay Kumar, Josyula R.Rao, Pankaj Rahotgi, "Efficient Implementation of Rijndael Encryption with Composite Field Arithmetic," Proceedings of Cryptographic Hardware and Embedded Systems (CHES), Vol. 2162, pp.175-188, 2001.10. Rohit Sharma, Vivek Kumar Sehgal, Nitin Nitin1, Pranav Bhasker, Ishita Verma, "Design and Implementation of 64-Bit RISC Processor using Computer Modeling and Simulation," Proceedings of UKsim, Vol. 11, pp. 568 – 573, 2009.11. R. Uma, "Design and performance analysis of 8-bit RISC Processor using Xilinx tool," International Journal of Engineering Research and Applications (IJERA), Vol. 2, Issue 2, pp.53-58, March-April 2012, ISSN: 2248-9622.12. Jean-Luc Beuchat, "FPGA Implementations of the RC6 Block Cipher," Laboratoire de l'Informatique du arall'elisme, Ecole Normale Sup'erieure de Lyon,46, All'ee d'Italie, F-69364 Lyon Cedex 07.13. Arturo Diaz-Perez, Nazar A. Saqib, Francisco Rodriguez-Henriquez, "Implementing Symmetric-Key Cryptosystems on Reconfigurable-Hardware," springer Nov 2006, ISBN : 0387338837.14. Imyong Lee, Dongwook Lee, Kiyoun Choi, "ODALRISC: A Small, Low power and Configurable 32-bit RISC processor," International SOC design Conference 2008.15. R. Razdan and M.D. Smith, "A High-Performance Micro architecture with Hardware-Programmable Functional Units," Proceedings of. Micro-27, pp. 172-180, 1994.16. Vincent P. Heuring, and Harry F. Jordan, "Computer Systems Design and Architecture," Second Edition, 6th Dec, 2003, ISBN-10: 0130484407.17. Dave Van den Bout "The Practical XILINX Designer Lab Book," pp.30-31, ISBN 0-13- 095502-7.18. XILINX datasheet library, http:// www.xilinx.com/ partinfo/4000.pdf19. Jonas Thor, "Evaluation of a reconfigurable computing engine for digital communication Applications," pp.12-17, ISSN 1402-1617.20. Rasset T.L, Niederland R.A, Lane J.H, Geideman W.A "A 32-b RISC Implemented in Enhancement-Mode JFET Ga As," Vol.3, pp.60-70, 9 Oct 1986.21. Dolle.M, Jhand. S, Lehner.W, Muller.O, Schlett.M. "A 32-b RISC/DSP microprocessor with reduced complexity," Proceedings of journals and magazines, Vol. 32, Issue 7, pp 1056-1066, 06 August 2002.22. Buhler, M. Baitinger "VHDL-based development of a 32-bit pipelined RISC processor," U.G. Stuttgart University, Vol 1, pp. 138-142, 06 August 2002.		4-8
	Authors:	Geethanjali Marri, P. Sri Padma, Ch. Ganapathi Reddy	
	Paper Title:	Conjugate Gradient Based MMSE Filter for Uplink Orthogonal Frequency Division Multiple Access Systems	

3.	<p>Abstract: Carrier Frequency Offset (CFO) compensation is very important for reliable detection of transmitted data in uplink Orthogonal Frequency Division Multiple Access (OFDMA) systems. In this paper we proposed a low-complexity CFO compensation algorithm based on the Minimum Mean Square Error (MMSE) criterion for uplink OFDMA systems. The proposed algorithm employs a Conjugate Gradient (CG) method which iteratively finds the MMSE solution. In this paper we are presenting the proposed method by comparing with the existing direct MMSE method and we show that CFO can be compensated with substantially reduced computational complexity by applying the CG method.</p> <p>Keywords: Carrier Frequency Offset (CFO), Orthogonal Frequency Division Multiple Access (OFDMA), Conjugate Gradient (CG).</p> <p>References:</p> <ol style="list-style-type: none">1. Cao, Z, Tureli, U, Yu-Dong Yao and Honan, P, "Frequency synchronization for generalized OFDMA uplink," 2004 IEEE GLOBECOM Proc, Vol. 2, pp. 1071-1075.2. "IEEE standard for local and metropolitan area networks, part 16: air interface for fixed and mobile broadband wireless access systems amendment 2: physical and medium access control layers for combined fixed and mobile operation in licensed bands," IEEE Std. 802.16e, Feb. 2006.3. J. R. Shewchuk, An Introduction to the Conjugate-Gradient Method Without the Agonizing Pain. Carnegie Mellon University, School of Computer Science, 1994.4. K. Etemad, "Overview of mobile WiMAX technology and evolution," IEEE Commun. Mag., vol. 46, pp. 31–40, Oct. 2008.5. Kilbom Lee, Sang-Rim Lee, Sung-Hyun Moon and Inkyu Lee, "MMSE-based CFO compensation for uplink OFDMA systems with conjugate gradient," IEEE Trans. Wireless Commun., vol.11, AUG 2012, pp. 2767-2775.6. Michele Moreli, Jay Kuo. C, "Synchronization techniques for orthogonal frequency division multiple access," IEEE Proc. Vol.95, no.7, July 2007, pp.1394-1427.7. Samuel C.Yang, " OFDMA system analysis and design," pp.1-92.8. Sreedhar. D and Chockalingam. A, " MMSE receiver for multiuser interference cancellation in uplink OFDMA," IEEE Trans. Wireless Commun., vol.6, Nov. 2008, pp. 2125-2129.	9-15				
4.	<table><tr><td>Authors:</td><td>Sreenivasa Reddy Mula</td></tr><tr><td>Paper Title:</td><td>Power Factor Correction</td></tr></table> <p>Abstract: In this paper, a new parallel-connected single phase power factor correction (PFC) topology using flyback converter in parallel with forward converter is proposed to improve the input power factor with simultaneously output voltage regulation taking consideration of current harmonic norms. Paralleling of converter modules is a well-known technique that is often used in medium-power applications to achieve the desired output power by using smaller size of high frequency transformers and inductors. The proposed approach offers cost effective, compact and efficient AC-DC converter by the use of parallel power processing. Forward converter primarily regulates output voltage with fast dynamic response and it acts as master which processes 60% of the power. Flyback converter with AC/DC PFC stage regulates input current shaping and PFC, and processes the remaining 40% of the power as a slave. A parallel-connected interleaved structure offers smaller passive components, less loss even in continuous conduction inductor current mode, and reduced volt-ampere rating of DC/DC stage converter. MATLAB/SIMULINK is used for implementation and simulation results show the performance improvement.</p> <p>Keywords: Ac-dc converter, pwm, pfc, simulink, matlab.</p> <p>References:</p> <ol style="list-style-type: none">1. R. Redl: "Power-factor correction in single-phase switching-mode power supplies-an overview", Int. J. Electronics, Vol. 77, No. 5, pp. 555-582, 1994.2. P. Tonti, G. Spiazzi: "Harmonic Limiting Standards and Power Factor Correction Techniques". Tutorial presented at the European Power Electronics Conference (EPE), Sevilla (Spain), September 1995.3. R. Redl, L Balogh : "RMS, DC, Peak and Harmonic Currents in High- Frequency Power-Factor Correctors with Capacitive Energy Storage". Proceeding of APEC '92, pp. 533-540.4. J. Zhang, M.M. Jovanovic, F.C. Lee: "Comparison between CCM single-stage and two-stage boost PFC converters". Proceeding of APEC '99, pp.335-41.5. Chow, M.H.L.; Siu, K.W.; Tse, C.K.; Yim-Shu Lee: "A novel method for elimination of line-current harmonics in single-stage PFC switching regulators". IEEE Transactions on Power Electronics, vol.13, (no.1), Jan. 1998. pp.75-83.	Authors:	Sreenivasa Reddy Mula	Paper Title:	Power Factor Correction	16-17
Authors:	Sreenivasa Reddy Mula					
Paper Title:	Power Factor Correction					
	<table><tr><td>Authors:</td><td>Raghava Yathiraju</td></tr><tr><td>Paper Title:</td><td>Acoustic Echo Cancellation Using Conventional Adaptive Algorithms</td></tr></table> <p>Abstract: An adaptive filter is a filter that self-adjusts its transfer function according to an optimization algorithm driven by an error signal. Because of the complexity of the optimization algorithms, most adaptive filters are digital filters. Adaptive filtering constitutes one of the core technologies in digital signal processing and finds numerous application areas in science as well as in industry. Adaptive filtering techniques are used in a wide range of applications, including, adaptive noise cancellation, echo cancellation, adaptive equalization and adaptive beamforming. Acoustic echo cancellation is a common occurrence in today's telecommunication systems. The signal interference caused by acoustic echo is distracting to users and causes a reduction in the quality of the communication. This paper focuses on the use of Least Mean Square (LMS), Normalised Least Mean Square (NLMS), Variable Step-Size Least Mean Square (VSLMS), Variable Step-Size Normalised Least Mean Square (VSNLMS) and Recursive Least Square (RLS) algorithms to reduce this unwanted echo, thus increasing communication quality.</p> <p>Keywords: Adaptive filters, Echo, Adaptive algorithms, Echo cancellation, Acoustic echo cancellation.</p> <p>References:</p> <ol style="list-style-type: none">1. Homana, I.; Topa, M.D.; Kirei, B.S.; "Echo cancelling using adaptive algorithms", Design and Technology of Electronics Packages,	Authors:	Raghava Yathiraju	Paper Title:	Acoustic Echo Cancellation Using Conventional Adaptive Algorithms	
Authors:	Raghava Yathiraju					
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	Authors:	Omar Turath Tawfeeq	
	Paper Title:	THD Reduction of A Current Source Rectifier-DC Motor Drive Using Single Tuned Filters	
6.	Abstract: A current source rectifier (CSR) is commonly used to supply a DC Motor with variable voltage for variable speed applications. A study of THD Reduction using single tuned filters employed to obtain the required low harmonic distortion and nearly unity power factor in A.C supply current over a wide range of operating shaft speed. The external performances of a three-phase CSR-fed separately excited DC motor drive such as power factor, harmonics factor, and efficiency using sinusoidal pulse width modulation (SPWM) control technique are obtained for different speeds and modulation indexes. Separately excited DC motors with armature voltage control provides constant torque operation. The effectiveness of the proposed system (2.3-kW 13A DC motor drive) was verified through computer Matlab simulations.		25-29
	Keywords: Current source rectifier, DC Drive, THD Reduction, Single tuned filters, SPWM.		
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7.	Authors:	Sainath A. Waghmare, Chandan D. Chaudhari, Sumit N. Gavande	
	Paper Title:	Numerical Analysis and Experimental Failure Mode Determination of Composite T -Joint	
	<p>Abstract: The use of fibre composite materials in more demanding roles is increasing due to increased performance requirements in various applications. One type of joint in a sandwich panels in superstructure is a T-joint. An existing design consists of panels joined by filler material and overlaminates of the same thickness as the skin laminates. The aim of the research was to determine the methodology to predict the failure mode of the T-Joint under a pull-off tensile loading using Finite Element model. The outcome of the research was that the Finite Element (FE) simulations were used in conjunction to determine the failure mechanism of the T-Joint in the presence of disbonds in the critical location. Stress distributions are investigated by both laboratory tests and numerical modeling, and design criteria for core pieces are presented.</p> <p>Keywords: Sandwich panels, Overlaminates, T-joint, Core pieces, FRP.</p> <p>References:</p> <ol style="list-style-type: none">1. Ferry Dharmawan. "The structural integrity and damage tolerance of composite t joint in naval vessel", School of Aerospace, Mechanical and Manufacturing Engineering, RMIT University, Melbourne, Victoria, Australia, November 2008.2. Toftgaard H, Lystrup A. "Design and test of lightweight sandwich Tjointfor naval ships". Compos A ApplSciManufact 2005;36:1055–65.3. Toftgaard, H &Lystrup, A. "Design and test of lightweight sandwich Tjoint for naval ships", Composites Part A: AppliedScience and Manufacturing ACMC/SAMPE Conference on Marine Composites (MarComp) 2003, vol. 36, no. 8, pp. 1055-1065.4. Shenoi RA, Hawkins GL. "Influence of material and geometry variations on the behaviour of bonded tee connections in FRP ships." Composites 1992;23:335–45.5. D.W. Zhou , L.A. Louca and M. Saunders, "Numerical simulation of sandwich T-joints under dynamic loading"Composites: Part B 39 (2008) 973–985 23 December 20076. Efsthathios E. Theotokoglou, "FAILURE MODES IN COMPOSITE JOINTS A FINITE ELEMENT STUDY" The National Technical University of AthensGR-157 73 Athens, Greece7. ST. JOHN, N, GRABOVAC, I, GELLERT, (2000) "Fiber-resin composite research in support of current and future Royal Australian Navy Vessels." International conference Construction Latest Development, London.8. Yadav S.S. and Chhapkane N. K., "Design and Testing of Lightweight sandwich T-joint of composite material using FEA and experimental technique", ISSN: 2278-0181, IJERT, Vol. 1 Issue 6, August- 2012.9. KIRSHAN K. CHAWLA, "Composite Materials", Springer publications, Second Edition , reprint (2006).10. David Cripps, Gurit, http://www.gurit.com11. M.D. Banea and L.F.M da Silva, "Adhesively bonded joints in composite materials: An overview", DOI: 10.1243/14644207JMDA219, Institution of Mechanical Engineers vol.223, 2009.12. Christian Berggreen, Christian Lundsgaard-Larsen, Kasper Karlsen, Claus Jenstrup and Brian Hayman, "Improving performance of polymer fiber vessels-Part I: Design aspects", 16th International Conference On Composite Materials, Kyoto Japan, 2007.13. S.M.R. Khalili and A.Ghaznavi, "Numerical analysis of adhesively bonded T-joints with structural sandwiches and study of design parameters", Elsevier, International Journal of Adhesion & Adhesives 31 (2011) 347–356, February 2011.14. www.azom.com15. X.X. Dai and J.Y. Richard Liew, "Fatigue performance of lightweight steel_concrete_steel sandwich systems", Elsevier, Journal of Constructional Steel Research 66 ,256_276, July 2009.16. http://www.dnv.com17. Keun-Il Song, Ji-Young Choi, Jin-HweKweon, Jin-Ho Choi and Kwang-Soo Kim, "An experimental study of the insert joint strength of composite sandwich structures", Elsevier, Composite Structures 86 (2008) 107–113, 200818. http://www.cetec.demon.co.uk19. A.P. Mouritz, E. Gellert, P. Burchill and K. Challis, " Review of advance composite structure for Naval ships and submarines ", Elsevier, Composite Structure 53 (2001) 21-41, 2001.20. E. Bozhevolnaya, A. Lyckegaard and O.T. Thomsen, "Novel design of foam core junctions in sandwich panels", Elsevier, Composites: Part B 39 (2008) 185–190.		
8.	Authors:	Kushal M. L, V. Venkateswarlu	
	Paper Title:	Design and Implementation of Phase Modulation Using PLL for Polar Transmitter	
	<p>Abstract: In this paper the phase modulation of polar transmitter has been implemented. The circuit for implementing phase modulation consists of Phase Lock Loop (PLL), Sigma Delta Modulator (SDM) and differentiator. The input signal is applied at the differentiator which will convert phase component to the frequency of the signal. The obtained frequency signal is given to the SDM which will convert the analog signal to the digital signals. The SDM should have four bits of resolution, equivalently 36 dB signal-to-noise-and-distortion-ratio (SNDR) for a 200 kHz bandwidth. For supply voltages from 2.5 V to 3 V, the current supply is desired to be less than 20 mA. The PLL consists of the reference signal of 125MHz, and output voltage around 2-3GHz with the VCO gain of 0.277GHz/V. The circuit of PLL, SDM and differentiator are implemented on the Cadence Virtuoso platform.</p> <p>Keywords: Polar transmitter, phase modulation, Phase lock loop, Sigma delta modulator, differentiator.</p> <p>References:</p> <ol style="list-style-type: none">1. John Groe., "Polar Transmitters for Wireless Communications," IEEE Communications, pp. 58-63, Sept. 2007.2. G. Brenna et al., "A 2-GHz Carrier Leakage Calibrated Direct-Conversion WCDMA, 2002.3. Transmitter in 0.13-mm CMOS," IEEE J. Solid-State Circuits, pp. 1253–62, Aug. 2004,4. T. Sowlati et al., "Quad-band GSM/GPRS/EDGE Polar Loop Transmitter," IEEE J. Solid State Circuits, pp. 2179–89, Dec. 2004.5. S Cripps, "Advanced Techniques in RF Power Amplifier Design," Norwell, MA: Artech House, 20026. Michael Youssef, Alireza Zolfaghari, Behnam Mohammadi, Hooman Darabi and Asad A., "A Low-Power GSM/EDGE/WCDMS Polar Transmitter in 65-nm CMOS," IEEE J. Solid State Circuits, pp. 3061-3074, Dec. 2011.7. T. A. D. Riley, M.A. Copeland, and T. A. Kwasniewski, "Delta-Sigma modulation in fractional frequency synthesis," IEEE J. Solid State Circuits, vol. 28, no. 5, pp 553-559, May 1993.8. J.Groe, "Highly Linear Phase Modulation," US patent 10/420,952.9. B.Razavi, "Monolithic Phase-Locked Loops and Clock-Recovery Circuits", IEEE Press, 1996.10. J. Maneatis, "Self-Biased, High-Bandwidth, Low-Jitter 1-to-4096 Multiplier Clock Generator PLL", IEEE J. Solid-State Circuits, vol. 38, no.11, pp. 1795-1803. Nov. 2003.		

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9.	Authors:	G. Anuradha
	Paper Title:	Self Automated Tool in Vehicular System That Identifies the Air Pollution and the Future of E-Governance
	<p>Abstract: Air pollution is a major issue that we face today. Pollution zone in during earlier century was low but keeps growing towards the current. Studies revealed the fact the concentration in organic and inorganic toxic elements keeps growing depending upon the region and vehicle type. There is a growing demand for the environmental pollution monitoring and control systems. Gas sensors help to detect gas molecules and the concentration of the gas analytical methods of identifying the gases has greater disadvantage than with fairly accurate and selective gas reading.</p> <p>Keywords: Embedded control, Monitoring system, Remote monitoring, sensor.</p> <p>References:</p> <ol style="list-style-type: none"> 1. "The use of electrochemical sensors for monitoring urban air quality in low-cost, high-density networks", M. I. Mead^{1*}, O.A.M. Popoola¹, G. B. Stewart¹, P. Landshoff³, M. Calleja², M. Hayes², J. J. Baldovi¹, T.F.Hodgson¹, M. W. McLeod¹, J. Dicks⁴, A. Lewis⁴, J. Cohen⁵, R. Baron⁶, J. R. Saffell⁶, and R. L. Jones^{1*}. 2. "A study on air pollution by automobiles in Bangalore city", Mahadevappa harish, iisc, management research and practice Vol.4 Issue 3(2012) PP: 25-36. 3. "A mobile GPRS-sensors Array for Air pollution monitoring", Imran Zuakernan, Fadi Aloul, IEEE sensors Journal, Vol.10, No.10, October 2010. 4. "Pollution Monitoring system using wireless sensor network in Visakhapatnam", P.Vijnatha Raju, RVRS.Aravind, B.Sangeeth Kumar, IJETT, Volume4 Issue4-April 2013. 5. "Smart sensor networks: Technologies and application for green growth", OECD, 2009. 6. "Automated control system for air pollution detection in vehicles", chandrasekaran, sudharshan muthukumar, sabeshkumar rajendran, 2013 4th International conference on intelligent systems, modeling and simulation. 7. "Implementation of web server using ARM for intelligent monitoring", pratik padia, R.Manohari, Sandeep Kethi redid, ASAR International Conference, ISBN:978-81-927147-0-7. 	