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S. No			Page No.
1.	**Authors:**	**Vibha Mishra, Vinod Kapse**	
	Paper Title:	**Hardware Implementation of 64 Bit Floating Point Arithmetic Using VHDL**	
	Abstract: Many of the scientific applications rely on floating point (FP) computation, often requiring the use of the 64 bit Floating Point format specified by the IEEE standard 754. The use of double precision (D.P.) data type improves the accuracy and dynamic range of the computation, but simultaneously it increases the complexity and performance of the arithmetical computation of the module. The design of high performance 64-Bit floating point units (FPUs) is thus of interest in this Document. **Keywords:** IEEE, (D.P.) (FP). **References:** 1. P. Belanovic and M. Leeser, ―A Library of Parameterized Floating-Point Modules and Their Use‖, in 12th International Conference on Field-Programmable Logic and Applications (FPL- 02). London, UK: Springer-Verlag, (2002) September, pp. 657–666. 2. K. Hemmert and K. Underwood, ―Open Source High Performance Floating-Point Modules‖, in 14th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM-06), (2006) April, pp. 349–350. 3. A. Malik and S. -B. Ko, ―A Study on the Floating-Point Adder in FPGAs‖, in Canadian Conference on Electrical and Computer Engineering (CCECE-06), (2006) May, pp. 86–89. 4. D. Sangwan and M. K. Yadav, ―Design and Implementation of Adder/Subtractor and Multiplication Units for Floating-Point Arithmetic‖, in International Journal of Electronics Engineering, (2010), pp. 197-203. 5. M. K. Jaiswal and R. C. C. Cheung, ―High Performance FPGA Implementation of Double Precision Floating Point Adder/Subtractor‖, in International Journal of Hybrid Information Technology, vol. 4, no. 4, (2011) October. 6. B. Lee and N. Burgess, ―Parameterisable Floating-point Operations on FPGA‖, Conference Record of the Thirty-Sixth Asilomar Conference on Signals, Systems, and Computers, (2002). 7. M. Al-Ashrafy, A. Salem, W. Anis, ―An Efficient Implementation of Floating Point Multiplier‖, Saudi International Electronics, Communications and Photonics Conference (SIECPC), (2011) April 24-26, pp. 1-5.	**1-4**
2.	**Authors:**	**R. Dhayabarani, R. S. D. Wahida Banu**	
	Paper Title:	**Performance Analysis of Multiplier using Full Adder**	
	Abstract: Addition is one of the fundamental arithmetic operations, which is used extensively in many VLSI systems such as application-specific DSP architectures and microprocessors. The adders determine the overall performance of the circuits in most of those systems. This paper introduces a novel low power and high-speed 8-Transistor 1-bit full adder cell, which is proposed. In this design, a novel low power and high speed 8-Transistor 1-bit full adder cell have six MOS transistors and multiplexer using two MOS transistors are applied to minimize the transistor count and reduce the power consumption and delay. The power dissipation and delay of the new design against other designs are analyzed via HSPICE simulations. The results feature that the proposed adder has both lower power consumption and high-speed operation. The combination of low power and low transistor count makes the new 8T full adder cell a viable option for an efficient design. **Keywords:** Full-adder design, low power, CMOS circuit, multiplexer, Very Large-Scale Integration (VLSI) **References:** 1. A. P. Chandrakasan, et al., "Low-power CMOS digital design," IEEE Journal of Solid-State Circuits, vol. 27, pp. 473-484, 1992. 2. J. M. Rabaey and M. Pedram, Low Power Design Methodologies. Norwell: Kluwer Academic Publishers, 1996. 3. R. Shalem, et al., "A novel low power energy recovery full adder cell," Ninth Great Lakes Symposium on VLSI, Proceedings, pp. 380-383, 1999. 4. R. Zimmermann and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," in 26th European Solid-State Circuits Conference (ESSCIRC 96), Neuchatel, Switzerland, 1996, pp. 1079-1090. 5. N. Zhuang and H. M. Wu, "A new design of the CMOS full adder," IEEE Journal of Solid-State Circuits, vol. 27, pp. 840-844, May 1992. 6. E. Abu-Shama and M. Bayoumi, "A new cell for low power adders," in 1996 IEEE International Symposium on Circuits and Systems. ISCAS 96, Atlanta, GA, 1996, pp. 49-52 vol.4. 7. A. M. Shams, et al., "Performance analysis of low-power 1-bit CMOS full adder cells," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 10, pp. 20-29, 2002. 8. J. F. Lin, et al., "A novel high-speed and energy efficient 10-transistor full adder design," IEEE Transactions on Circuits and Systems I-Regular Papers, vol. 54, pp. 1050-1059, 2007. 9. T. Lynch and E. E. Swartzlander, "A spanning tree carry lookahead adder," IEEE Transactions on Computers, vol. 41, pp. 931-939, Aug 1992. 10. J. M. Wang, et al., "New efficient designs for XOR and XNOR functions on the transistor level," IEEE Journal of Solid-State Circuits, vol. 29, pp. 780-786, Jul 1994.	**5-8**
3.	**Authors:**	**Neelam T. Rakate, U. A. Patil**	
	Paper Title:	**Iris Biometric for Person Identification Using Dual- Tree Complex Wavelet Transform**	
	Abstract: Technologies that exploit biometrics have the potential for application to the identification and verification of individuals for controlling access to secured areas or materials. A wide variety of biometrics has been marshaled in support of this challenge. Resulting systems include those based on		**9-18**

automated recognition of retinal vasculature, fingerprints, hand shape, handwritten signature, and voice. Unfortunately, from the human factors point of view, these systems are highly invasive. One possible alternative to these methods that has the potential to be less invasive is automated iris recognition. Interestingly, the spatial patterns that are apparent in the human iris are highly distinctive to an individual. The iris has unique features and is complex enough to be used as a biometric signature. Therefore, in order to use the iris pattern for identification, it is important to define a representation that is well adapted for extracting the iris information content from images of the human eye. Here we represent a new algorithm for extracting unique features from images of the iris of the human eye and representing these features using two-dimensional dual-tree complex wavelet transform (DTCWT). This representation is then utilized to recognize individuals from images of the irises of their eyes. The proposed technique is translation & shift invariant. For the dual filter tree, we have selected two linear phase biorthogonal filter sets of same lengths (based on Selesnick's approach) which are used to filter each signal for quantization to 375 byte iris feature codes. Then the Hamming distance is used to match two iris codes. The experimental results on UPOL database shows good reliability and performance, so it is promising to be used in a personal identification system.

Keywords: Biometrics, Complex Wavelet Transform, Feature extraction, Hamming distance.

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Authors:	**C. Jena, Amruta Das, C. K. Panigrahi, M. Basu**
Paper Title:	**Modelling and Simulation of Photovoltaic Module with Buck-Boost Converter**

Abstract: This paper presents a unique step-by-step procedure for the simulation of photovoltaic modules with Matlab/ Simulink. The objective is to design & simulate a controller for the unlimited solar power drawn from the sun & produce a higher voltage o/p through the d.c. to d.c. (Buck-boost) converter .One-diode equivalent circuit is employed in order to investigate i-v and p-v characteristics of a typical 36W solar module. The proposed module is designed with different icons, dialogue box like simulink block libraries. This PV module is interfaced to the buck boost converter and the performance has been studied by the matlab simulink.

Keywords: Photovoltaic (PV), Buck-Boost Converter, simulation of PV model, simulation results.

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