

AUTOMATED DEFECT PATTERN RECOGNITION: AN APPROACH TO DEFECT CLASSIFICATION AND LOT CHARACTERIZATION

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ABSTRACT

The especially complex and precise nature of semiconductor fabrication often results in low yield across industry (Van Zant 2000). To identify the root cause of a defective chip, a Capstone team of undergraduate students from the University of Virginia began work with Dominion Semiconductor for the development of an automated system that classifies clusters of defective chips and characterizes a group of wafers known as a lot. Work from a previous team began developing a tool that clusters and identifies groups of defective chips on a wafer. With cluster recognition algorithms already implemented, this year's Capstone team developed a system that takes the coordinates of clustered defective chips and proceeds to classify the defect. Each defect cluster is categorized as a specific defect type. Lastly, the system employs the results of classification and determines whether a dominant defect is present within the lot, and characterizes the lot accordingly.

A set of metrics were developed to numerically represent defect clusters. As each defect that is classified using this approach is a cluster or blob of defective memory chips, the metrics shall be referred to a Blob Identification Metrics (BIMs). Next, a set of common defect types for classification is defined. Defect clusters that do not correspond to one of the defined defect categories are designated as "other." Accordingly, metrics that extract signature features of each defect type are applied to the data provided by DSC. In addition, the system determines the predominant defect cluster type present within a lot. The primary criterion for lot characterization is the number of defective chips resulting from each defect type.

INTRODUCTION

Dominion Semiconductor (DSC) produces between 200 and 300 memory chips on silicon wafers. Wafers travel through the fabrication process in a group of up to 25 known as a lot. Functional and electrical tests are conducted on every completed chip to identify defective memory chips. Due to the micro-scale and complex nature of semiconductor manufacturing, fabrication often results in several defective chips on an individual wafer. In an effort to better understand why defects occur, DSC's Integration and Characterization group visually observes groups of wafers to identify and classify any emergent patterns or clusters of defective chips (Spinelli 2001). This project has developed a prototype automated tool that automates the analysis of groups of defective chips or defect clusters. Specifically, defect clusters are identified and lots are characterized according to the predominant type of defect present. This concept may then be extrapolated to characterization across lots.

To achieve this goal, a series of metrics that numerically represent defect clusters, Blob Identification Metrics (BIMs), have been developed. Characterization experts at DSC have defined a set of common defect types for recognition. These metrics are applied to our project in a three-step process. First, BIM values are generated for each defect cluster found on a wafer. Next, BIMs are interpreted for the classification of a defect cluster. Lastly, defect clusters of the same type are compared to determine whether or not they have the same root cause. The most common defect is denoted as predominant defect pattern for that lot. This approach to defect classification and lot characterization was applied to the data provided by DSC.

Due to the large scale of this problem, this project builds on the work of previous undergraduate students. Last year's Capstone team presented an automated system that detects defect clusters on individual wafers. Their approach consisted of three phases. First, several statistical tests were used to determine if defect patterns occurred randomly. Random defects do not need to be considered when evaluating defect patterns because their classification is complete. Next, data filtration focuses on the removal of irrelevant information from wafer maps. Lastly, hierarchical and non-hierarchical clustering algorithms are used to locate the clustered defects (Amin 2001).

METHODOLOGY

Figure presents a system-level flow for the project. Accordingly, it incorporates both past and recent work. The upper portion of Figure 1 describes the work completed by last year's Capstone team. The lower portion explains the approach developed by this year's Capstone team to achieve lot characterization.

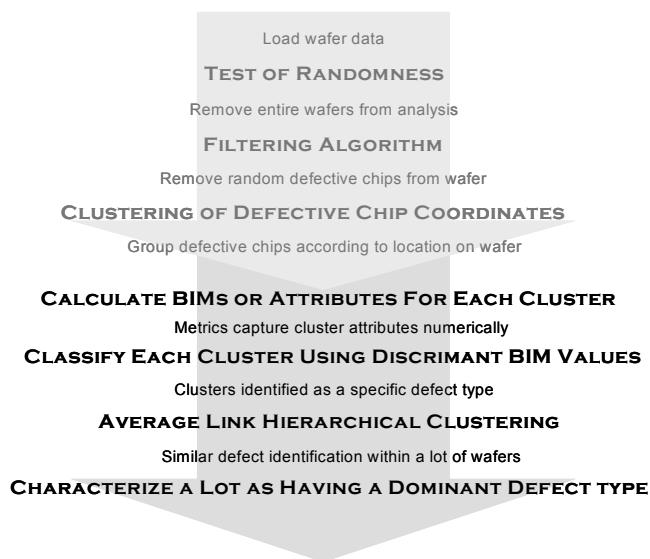


Figure 1 System Level Flow Chart

Defect Classification. Once defect clusters have been identified on an individual wafer, the next step is to classify the defects. After analysis of the data and discussions with the client, several common clustered defect types emerged as illustrated in Figure 2. Different defect types are the result of various errors that occur during fabrication.

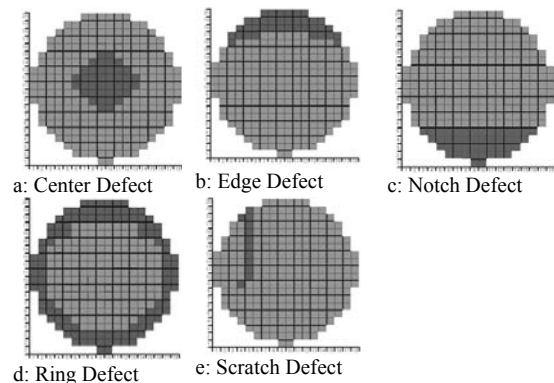


Figure 2: Defect Types

All of these defect clusters or “blobs” share common traits. Features of the various defect types can be described by using a common set of metrics. These metrics are called Blob Identification Metrics (BIMs). The complete set of BIMs are listed below and are graphically described in Figures 3 and 4.

- X Moment
- Y Moment
- Center of Mass
- X Length
- Y Length
- Span
- Regions
- Mass
- Span/Mass Ratio

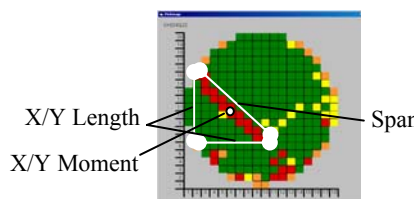


Figure 3: BIMs

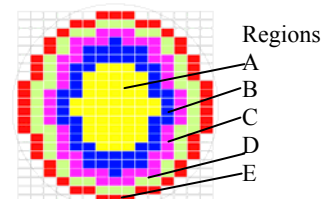


Figure 4: Region BIMs

Once BIM values are known, the system analyzes them to determine the significant differences that exist. Specific BIMs called *Signature Features* emerge as important values that provide evidence for a specific defect type. The BIMs essentially act as writing tools for leaving signature markings. By calculating and analyzing the BIM values for each defect type, the signature features for each defect type were identified:

Ring Defect

- Regions: Large defective chip to total number of chips in the D and E region
- Center of Mass: may not be located within defect

Edge Defect

- A and B Regions less than D and E Regions

Scratch Defect

- Span/Mass Ratio: value close to 1
- Regions: Ratio of bad chips to total number of chips in a region will be small

Center Defect

- Center of Mass: close to center
- Span/Mass Ratio: small and close to 0
- Regions: Low yield in region A, yield may remain low in regions B and C

Notch

- The notch chips must be defective
- X and Y moments: X moment will be close to center, and Y moment is located in the lower half of the wafer

Lot Characterization. Once the system has classified all the clusters of defective chips in a lot, the system determines a predominant defect type for lot characterization. If the lot has several ring, center, or notch defects, the system automatically characterizes the lot by the reoccurring defect type. Otherwise, if several edge or scratch defects occur within a lot, the system compares the defects within the specific defect type in order to determine if they have the same root cause. The system utilizes variations of BIM values as inputs for average link hierarchical clustering. The clustering algorithm outputs groups of similar defects within a defect type. These defects are considered to have the same root cause. Figures 5 and 6 illustrate the clustering used to determine similar defects. Specifically, Figure 5 represents visual groupings of similar edge defects.

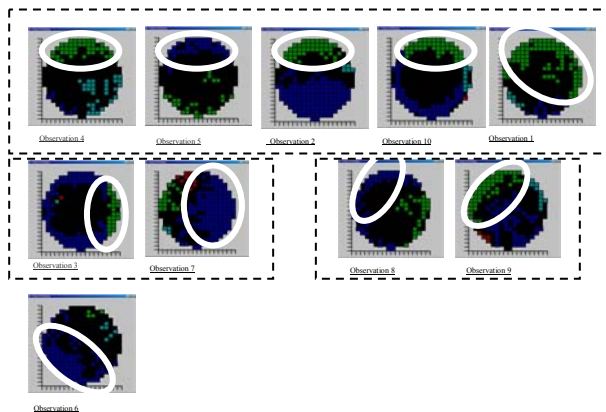


Figure 5: Hierarchical Clustering of Similar Edge Defects

The similar edge defects visually grouped in Figure 5 correspond to the statistical software clustering output in Figure 6. SAS was employed for clustering.

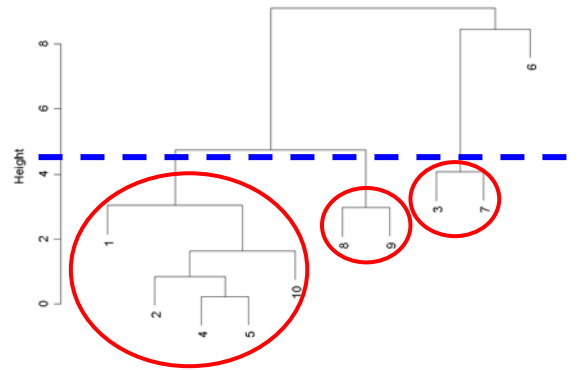


Figure 6: Visual Grouping of Similar Edge Defects

EXPEREMENT AND TESTING

This section describes the test statistics and procedures used to evaluate the system classification accuracy. The procedure analyzes all defects types separately and gives a statistical accuracy score for each. Totaling the accuracy scores provides a mathematical statistic rating for the entire system. The results of each defect characterization test the null hypothesis.

Null Hypothesis = H_0 = Defect Cluster is classified by the system the same as expert human observation.

Type I Error: The system says it is NOT a specific defect type when in fact expert opinion would say it IS.

Type II Error: The system says it IS a specific defect type when expert opinion says it IS NOT any specific type.

The test assumes the null hypothesis (H_0) is true until the results reject it as false. Lots previously characterized by Dominion engineers provide a standard for understanding the system results. The null hypothesis is rejected if the system makes either of the two error types described previously. Table 1 presents the accuracy rates for each defect type classification. Table 2 summarizes the error percentages for each error type.

Ring	Notch	Edge	Other
71%	67%	100%	36%

Table 1 Accuracy Rate Per Defect Type

Type I Errors	20.7%
Type II Errors	64.0%

Table 2 Error Summary

Center/Scratch. The lots used for testing contained very few center defects. Therefore, the test sequence did not analyze center defects. Additionally, the inadequacies of the clustering algorithms in detecting scratches made testing the accuracy of that interpretation difficult. The test procedure did not analyze the accuracy of the scratch interpretation.

INTERPRETATION OF RESULTS

The results show the system's capability of detecting several types of defects on a relatively consistent basis. The system classifies rings, notches, and edges combined with an almost 80% accuracy. The high error percentage score for type 2 errors creates some concern. This indicates that while the broad tolerance ranges sufficiently detect a wide variety of defects within types, they over characterize and recognize clusters that have no type as one of the predefined types.

The results showed a 100% accuracy rating for edge defect classification. However, the system commonly mischaracterized defect types as edges. These two facts lead to the conclusion that the edge interpretation is too broad. Tightening of the edge definition may reduce a large percentage of the type 2 errors. The system only classified notches correctly 67% of the time. This indicates that the notch interpretation and signature features values are too narrow. This leads to the improper classification of many notches. Overall, the system performs well at detecting specific defect types. The edge and notch interpretations need to undergo further analysis to determine if a better way exists.

Testing Lot Characterization. Two cases exist for lot characterization. The first case requires multiple occurrences of one of three specific defect types, notch, center or ring. The lot is simply characterized by the predominant defect type. For reoccurring scratch or edge defects within a lot, further analysis is required to characterize the lot as having a predominant defect type. Not all scratch or edge defects have the same root cause; consequently, the location, size and orientation on the wafer must be considered. In order to determine similar defects within these types, three hierarchical clustering algorithms were tested. Also, three combinations of BIM values were used as inputs for each algorithm.

Null Hypothesis: All defects in the same cluster are the "same" defect for the purpose of lot characterization.

Type I Error: S Plus excludes an observation that belongs in a specific cluster.

Type II Error: S Plus includes an observation that does not belong in a specific cluster.

Table 3 displays the results of testing single link (S – Link), complete link (C – Link) and average link (A – Link) hierarchical clustering for edge defects.

Input Variables	Method	Type I	Type II	Total
All BIMs	A-link	3	3	6
	C-link	3	3	6
	S-link	3	3	6
Signature BIMs	A-link	0	0	0
	C-link	0	0	0
	S-link	2	0	2
xmom, ymom, & mass	A-link	3	3	6
	C-link	3	3	6
	S-link	3	4	7

Table 3 Edge Clustering Results

In conclusion average link clustering determines similar defects within a lot of wafers most accurately. For edge defects, the clustering algorithms uses signature BIMs as variable inputs and produces the most accurate results. On the other hand, for scratch defects, the clustering algorithm uses all of the BIMs as variable inputs and produces the most accurate results. The discrepancy in the variable inputs according to defect type takes into account the different nature of each defect. Scratch defect clustering uses all of the BIMs because scratches are more tightly defined and in order to characterize them as the same defect within a lot, all of their BIM values must match to a certain degree. Since experts at Dominion Semiconductor define similar edge defects more loosely, the same machine or process could cause a repeated edge defect to occur in a lot and the edge defects could be relatively different.

CONCLUSION

This project served as a proof of concept for a tool that Dominion Semiconductor may develop in the future. Although the automated tool developed by this project locates and classifies defect patterns in individual wafers and across wafer lots, additional work will be required to ensure successful

implementation of a comprehensive tool aimed at using characterization techniques to increase yield.

DSC expects that the use of automated tools for defect pattern recognition and lot characterization will aid in efforts to significantly increase their yield. Simply stated, the fabrication process will become more efficient and a greater number of viable chips will be produced. In its final form, an automated tool will identify faulty machinery for repair. As a result, a reduced number of wafers and memory chips will be damaged during fabrication.

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BIOGRAPHIES

Megan Elizabeth Guise is a fourth-year Systems Engineering major from Midlothian, VA, concentrating in economic systems. Her principal contribution to the project was in the area of lot characterization using hierarchical clustering.

Deborah Kimberly Poe is a fourth-year Systems Engineering major. As the daughter of a career naval officer, she has traveled the globe and lived in places like Hawaii and Singapore. Her principal contribution to the project was in concept development and organization of the implementation. She has accepted a position working for Dell Computer Corporation in Austin, TX, and will begin work as a Systems Test Engineer following graduation.

Joshua Stafford is a fourth-year Systems Engineering major from Medford, NJ, concentrating in computer and information systems. His principal contribution to the project was interface design and implementation of the functionality into a Visual Basic application. He is graduating in May of 2002.

Andrew Wahba is a fourth-year Systems and Electrical Engineering double major from Crofton, MD. The concentration of his undergraduate studies at the University has been communication and control systems. His principal contribution to the project was in the area of metrics for defect classification. He has held internship positions at Northrop Grumman Corporation.

