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CPLD Based Speed Controller of a DC Motor Operated Through Cellphone

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Abstract*— In this paper a new method has been developed to control the operation of a DC motor remotely. It becomes very much advantageous if a DC motor is controlled using a cellphone. In order to do that the proposed method uses a complex programmable logic device (CPLD). The control input of CPLD is given by Dual Tone Multi-Frequency Signaling (DTMF) decoder. The decoder is connected with a cellphone. It becomes very much beneficial as range of controlling becomes very much wider i.e equivalent to coverage area of the service provider. It is known that CPLD provides quick implementation and fast hardware verification. It gives facilities of reconfiguring the design construct unlimited number of times. The function of CPLD is to process the data coming from the output of DTMF decoder and to create proper duty cycle PWM output, which will control the speed of DC Motor. Hardware is implemented using CPLD trainer kit (model: UNI-BSX-M1) and software is written using VHSIC hardware description language *(VHDL) as a pattern tool.

***Index Terms*— DC motor, CPLD, VHDL, PWM, DTMF.**

I. INTRODUCTION

There are various techniques used for controlling the operation of DC Motors [1-2]. In the modern era of technology sophisticated methods are used for controlling the motion of motors. In this paper speed of the motor is controlled by using a CPLD based system. Controlling of DC motor using CPLD instead of microcontroller or microprocessor based system has several numbers of advantages

i The design is written in a high-level language, such as VHDL[3] using software development tool, but it is not available in microcontroller based system where program must be written in assembly language.
ii VHDL enables to express the concurrent as well as sequential behavior of a digital system [5].
iii. Test waveform can also be generated using the same constructs.
iv Microprocessor demands to power up which slower the switching sequence in the motor operation.[6]
v. The design is modeled for timing correctness.
vi. The design is programmed into the physical device.

Due to these numbers of advantages the proposed technique used CPLD based system.

PLAs and PALs are useful for implementing small digital circuits. For implementation of circuit that require more inputs or outputs, either multiple PLAs or PALs can be employed or else a more sophisticated type of chip, called a Complex Programmable Logic Device (CPLD) can be used. Fig. 1 shows the structure of a CPLD which comprises multiple circuit blocks on a single IC chip with internal wiring resources to connect the circuit blocks. Each circuit block is similar to a PAL (PAL-like block).

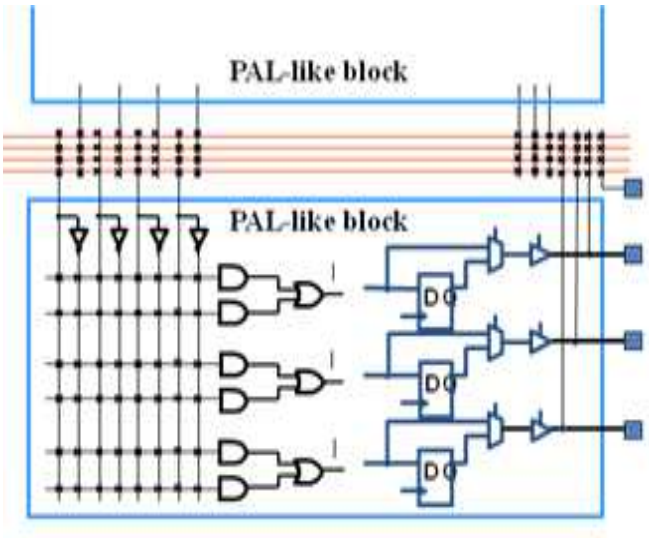

Fig. 1: Structure of CPLD

The design technique also takes advantages of Pulse Width Modulation (PWM). PWM has now a day's become an important part of every electronics system. One of the most used techniques of PWM is found as a voltage controller. Its use in controlling output voltage of DC motor is the most frequently used application.

Fig. 2 represents the block diagram representation of the proposed design.

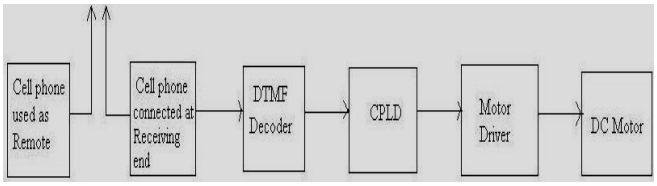

Fig. 2: Block Diagram of Speed controller using CPLD and mobile as a Remote

II. PRINCIPLES OF PWM BASED DC MOTOR DRIVE

Pulse width modulation (PWM) widely used for digitally controlling analog motor circuitry, the time period of the square wave is constant, and the time of the signal remaining high (T_{ON}), is varied or modulated. The duty cycle and average DC value of the signal can be varied in this way. Using the digital system, PWM becomes a powerful technique to control analog circuits.

The PWM method of switched-mode voltage control is used to armature current control, and hence output torque control, of DC motors. The design of a pulse width modulated drive is affected by the characteristics of the DC motor. [6]

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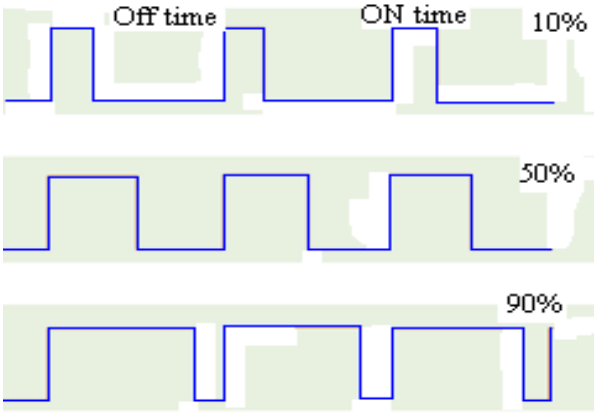

Fig. 3: PWM Waveform for various Duty Cycle

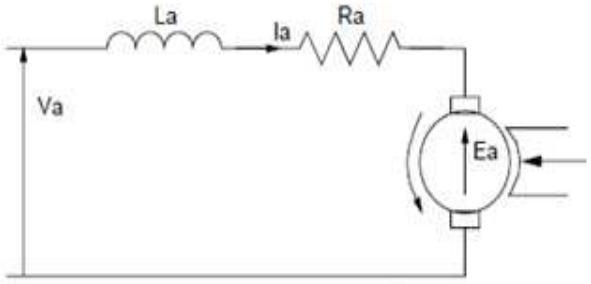

Fig. 4: Equivalent Circuit of a DC motor

From the above fig. 2 La denotes the equivalent armature inductance; Ra is the total series resistance, and Ea the armature back emf. The part of the total incoming energy Ea is transferred to corresponding mechanical output. The motor speed depends on value of armature emf. Average motor Current is a function of the electrical time constant of the motor, τ_a where τ_a=La/Ra (1)

For a PWM waveform with a period T the ratio of pulse width to switching period is denoted by δ. The average pulse current will depend upon the ratio of the current pulse-width, δT to the motor electrical time constant, τ_a. The DC motor having an electrical time constant, τ_a nearer to the duration of the applied waveform T. (τ_a = kT where k is small).

The initial motor current is given by

$$L_a.di_a/dt + R_a i_a = V_{dc} \quad (2)$$

Duty cycle ratio, controlled using V_{REF}, is given by δ, then the duration of the 'ON' pulse is simply given by δ_T.

$$i_a = V_{dc}/R_a(1-e^{t/\tau_a}) \quad (3)$$

$$i_a = I_1.e^{-(t-\delta T)/\tau_a} \quad (4)$$

In general motor equation becomes

$$L_a.di_a/dt + R_a i_a = V_{dc} - E_a \quad (5)$$

In order to obtain desire result H-Bridge Electronic Circuit is used which acts as a motor driver. Fig.5 allows Motor to run forward and backward direction. Here S1, S2, S3 and S4 are the switching elements. These switches are turns in pairs either S1 and S4 or S2 and S3.If both of one side turns on then it creates short circuit, which is not desirable for proposed technique. To turn on the motor diagonal switches has to be turned on.

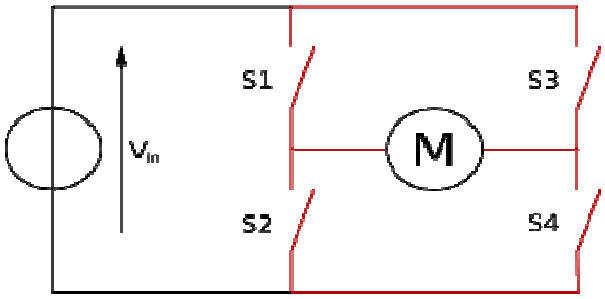

Fig. 5: H-bridge construction

When the switches S1 and S4 are closed S2 and S3 remain open then the motor rotates in one direction and whenever the switches S2 and S3 are closed S1 and S4 remain open the motor rotates in another direction. This concept has been taken to operate the motor either in forward or reverse direction according to the pin configuration and the function table of the one most popular Motor driver IC L293D. It is a Quadruple H-bridge driver IC which can be used in several purposes. It is used to drive inductive loads like DC motor, solenoids, relays, bipolar stepping motors etc [9].

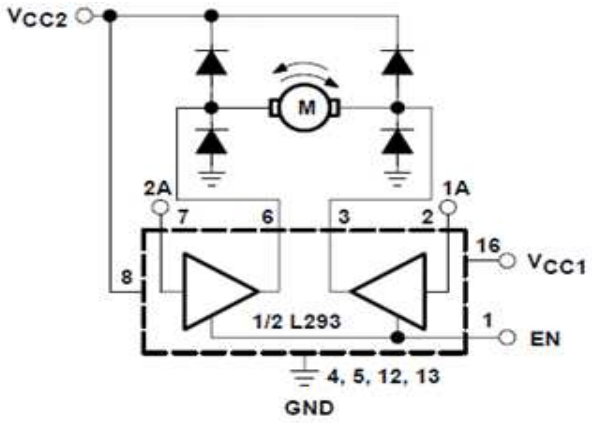

Fig. 6: Internal Circuit diagram of L293D

Table I shows the function table of the motor driver IC L293D.

Table I: Function Table of Motor Driver IC L293D

EN	1A	2A	Function
High	Low	High	Turn Right
High	High	Low	Turn Left
High	Low	Low	Fast motor stop
High	High	High	Fast motor stop
Low	Don't Care	Don't Care	Fast motor stop

Keeping time period constant if the ON time and OFF time of the clock pulse is changed then the duty cycle will be varied accordingly. Depending upon the different duty cycle generated by the CPLD through VHDL program motor will be operating and the speed will be increased or decreased in both the direction of operations.

III. CIRCUIT DESCRIPTION

In this method a mobile phone initiates a call for the other mobile connected with the receiver end. During this outgoing call if any button is pressed the associated button generates dual tone multiple frequency (DTMF) tone at the other end [7]. The received tone is processed by the CPLD (Family: XC 9500, Device: XC 9572, Package: PC84) with the help of DTMF decoder MT8870. A specific frequency consisting of two separate tones is assigned by the DTMF

decoder. It produces two different frequencies from lower band and upper band frequencies. For an example pressing a button '2' will send a tone comprises of 697 Hz and 1336 Hz to the other end of the system. Then the decoder produces an equivalent binary digit after decoding the DTMF tone. This binary number goes to the CPLD which is programmed to take a decision for any given input and produces the output for the motor driver (L293D) [9] whether to drive the motor either in forward or backward motion and to increase or decrease the speed of the motor. DTMF keypad layout and their frequencies are shown in table II.

Table II: DTMF Keypad layout and their frequencies

Frequency	1209 Hz	1336 Hz	1477 Hz	1633 Hz
697 Hz	1	2	3	A
770 Hz	4	5	6	B
852 Hz	7	8	9	C
941 Hz	*	0	#	D

IV. FUNCTIONAL DESCRIPTION OF DTMF UNIT

Dual tone multi-frequency signaling (DTMF) employs a mixture of two pure tone (pure sine wave) sound. The frequency protocol is devised by CCITT. The architecture of DTMF decoder consists of a bandsplit filter section to separate the high and low group tones, followed by a digital counting section. The frequency and duration of the received tones are verified by the counting section before passing the related code to the output bus.

Table III: Function assigned for the key

Key pressed by user	Action performed
2	Forward Motion
8	Backward Motion
5	Stop
4	Speed Decrement
6	Speed Increment

Among the keys Specified in Table IV, only 5 different keys have been taken to serve our purpose of controlling the speed. The table III shows the action performed corresponding to the keys pressed.

Table IV: Function Table of DTMF decoder MT8870

Low Group Freq. (Hz)	High Group Freq. (Hz)	Digit	Binary Output			
			Q4 (MSB)	Q3	Q2	Q1 (LSB)
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0

V. HARDWARE IMPLEMENTATION & SIMULATION OVERVIEW

A number of steps are to be followed for successful implementation of PWM generator design on CPLD. Design entry is the first step of designing on CPLD, followed by Behavioral simulation using Xilinx ISE simulator [8]. Then the design is synthesized using Xilinx XST, which maps the behavioral design to gate level design. The design flow is shown in fig. 7

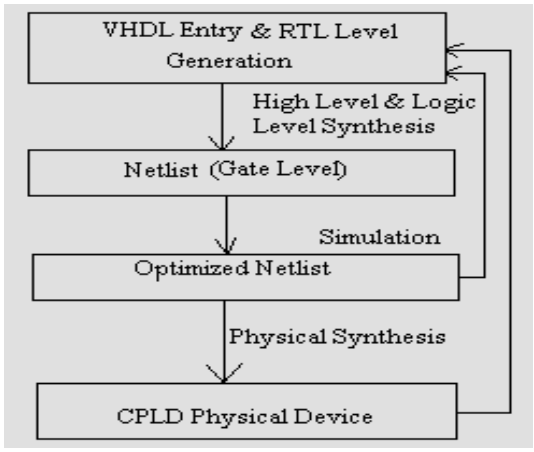

Fig. 7 CPLD based system Design flow

User Constrained file (UCF) is created to assign pin configuration of the CPLD to be connected with the DTMF decoder and the motor driver properly. After generating the suitable file the program is downloaded into the CPLD which is connected to the PC via JTAG cable. CPLD usually support the ISP technique. A small connector is included on the PCB and is connected to a computer system. CPLD is programmed by transferring the programming information from the CAD tool to into the CPLD. The circuitry on the CPLD that allows this type of programming is called JTAG, Joint Test Action Group port, and is standardized by the IEEE. JTAG is a non-volatile type of programming i.e programmed state is retained permanently (for example, in case of power failure, CPLD retains the program). The resulting simulation for 4-bit binary input combination corresponding to the key pressed to generate PWM signal of different duty cycle is shown below in the following figures.

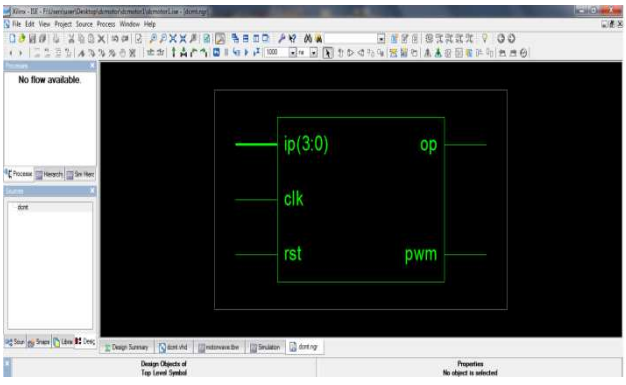

Fig. 8: RTL schematic of the proposed design

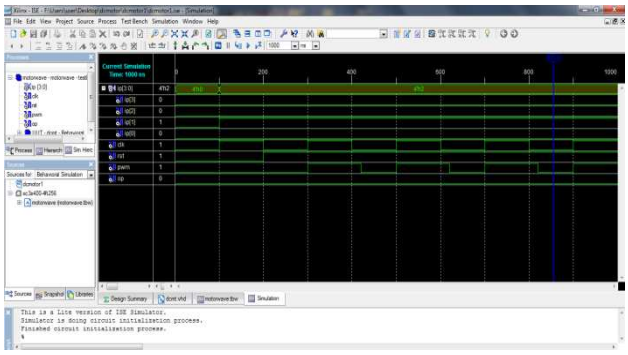

Fig. 9: For binary input of "0010" and duty cycle = 60%

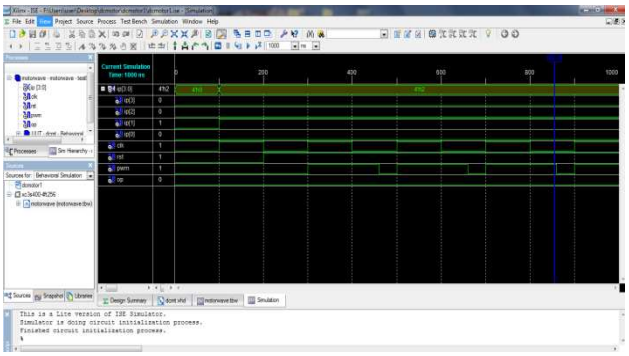

Fig. 10: For binary input of "0010" and duty cycle = 80%

VI. CONCLUSION

This paper presents a unique idea of creating control hardware through the programming language of VHDL. Build up of wireless control hardware modules connected with CPLD also provides a new idea of controlling method. This module offers precise timing to control motor. As open Loop control is CPLD based it completely eliminates the disadvantages of using Microprocessor or Microcontroller unit used to control the motor.

VII. ACKNOWLEDGMENT

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