DOI 10.1515/aee-2016-0034

Low cost, high accuracy real-time simulation used for rapid prototyping and testing control algorithms on example of BLDC motor

MARCIN BASZYŃSKI

Department of Power Electronics and Energy Control Systems AGH-University of Science and Technology Mickiewicza 30, 30-059 Kraków, Poland e-mail: mbaszyn@agh.edu.pl

(Received: 17.06.2015, revised: 04.01.2016)

Abstract: This article presents the simulation of a BLDC motor and its closed control system in FPGA. The simulation is based on a mathematical model of the motor, including the electromagnetic torque, phase currents, back electromotive force, etc. In order to ensure calculation precision, the equations describing the motor were solved using a floating point representation of real numbers, and a small step of numerical calculations of 1 μ s was assumed. The time step selection methodology has been discussed in detail. The motor model was executed with the use of Textual Programming Languages (with HDL codes).

Key word: BLDC, FPGA, real time simulation

1. Introduction

The development of BLDC motors [1-6] and their control algorithms have brought the need for developing methods of their simulation. The simplest power electronic and mechatronic system simulators are soft computing techniques (off-line) based on specialized computer programs such as Spice, Matlab or Saber software [7, 8]. Their advantages are: ease of simulation execution (often not requiring professional knowledge of the simulation program), access to numerous predefined models with the capability to perform even very complicated simulations, and high calculation precision. Some programs enable the determination of semiconductor element temperatures. The disadvantages of simulations of this type are the relatively long time required to make the calculations (the results are not obtained in real time) and the fact that the results include a narrow time window.

This problem can be solved by the Real-Time simulation (RTs). The use of these simulation methods enables the integration of the power circuit simulation with the control system

M. Baszyński	Arch. Elect. Eng.

[8-13] (electronic control units (ECUs). Examples of such solutions are dSpace [8], RTLAB from Opal-RT Technologies [9], RSCAD [14], FPGA implemented simulations [9, 15, 16] and combined analog-digital simulations [10]. The simulation environments enable the generation of source codes in the C language [8] or the HDL language (in combination with the Altera DSP Builder or Xilinx System Generator blockset for Simulink) [9]. The generated codes can be used directly in the target device, which simplifies the construction of the new controller.

An important aspect of the RTs is the possibility to test not only algorithms and control systems, but also protections, e.g. overcurrent protections (system shutdown, blocking transistor control pulses when circuit overcurrent is detected) [10, 13].

The RTs also enables inexpensive verification of new control algorithms [10, 11, 16], and is particularly useful for testing systems such as HVDC or STATCOM before connecting these devices in the field [10, 15, 17, 18]. Validation of control systems using the FPGA-based RTs model can be realized as: the tested control system and the physical model of the object (BLDC motor) are implemented in a single FPGA chip (Fig. 1). This approach requires a specialized board equipped with an FPGA chip with large LE numbers and with D/A converters (permitting the recording of simulation results on an oscilloscope screen). The exchange of data (currents, voltages, etc.) between the BLDC motor model and the control system is realized by the internal digital buses of the FPGA chip.

The control system validation method presented in the paper has been realized in accordance with the schema presented in Fig. 1.



Fig. 1. The control system validation method

The development of FPGAs [18, 19] offering the possibility to carry out numerous calculations simultaneously and having in their structures specialized calculation supporting blocks (DSP Block, hardware multipliers) have resulted in the capability of executing the HIL simulation and Rapid Control Prototyping (RCP) [18-21]. The multithreading and the high speed of FPGAs enable the carrying out of very complex calculations in real time. References cite two main methods of simulation execution in FPGA: a) using Textual Programming Language (TPL);

b) using Schematic Block (SB).

The first of these methods requires a considerable amount of knowledge of the organization and operating principle of FPGAs, but it offers high description capabilities of simulated systems (including physical properties of semiconductor structures of power electronic switches) [18-20].

The other method, SB, is based on library elements made available by FPGA manufacturers [10, 11]. The simulation employs predefined arithmetic operation blocks which are connected by the user and form a calculation model. This method is simple and does not require specialized knowledge of FPGA programming. The development of this method allows for model creation using Altera DSP Builder or Xilinx System Generator blocksets within Matlab/ Simulink [12]. In this method, the model of the analyzed object is created in the Matlab/Simulink environment. The advantages of the SB method are the use of numerical calculation methods applied in the Matlab environment and the capability of constructing even very complex models in a short time, with or without the knowledge of FPGA programming principles.

This paper presents a model of the BLDC motor, feeding inverter and closed control system. The motor model was executed using the HIL method and a floating point description. The motor model and the control system were executed in a single FPGA using the VHDL language. An advantage of this approach in relation to the aforementioned solutions is the capability to test control system algorithms and protections in the form of an environment in which they will actually operate (Quartus II). This is a capability not offered by any off-line method. In this paper, an inexpensive method of validation of the control systems of electronic power converters with the example of a BLDC motor control system is presented. The described method is characterized by very high calculation accuracy (64-bit floating-point type has been used for the description of the mathematic model of the BLDC motor). Moreover, it does not require the purchase of expensive software or an IP Core license (no IP Core has been used in the presented solution). Free software (Quartus II Web Edition) and an FPGA chip from the inexpensive Cyclone III family are sufficient in order to realize this method.

2. Motor mathematical model



Fig. 2 shows a substitute diagram of a brushless motor in a linear range with the inverter.

Fig. 2. BLDC motor substitute diagram

M. Baszyński

In the model, it was assumed that the motor is fully symmetrical (each of phase parameters is identical). On the basis of this assumption, the equation describing the substitute diagram shown in Fig. 2.

_

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} L_a & M_{ab} & M_{ac} \\ M_{ab} & L_b & M_{bc} \\ M_{ca} & M_{cb} & L_C \end{bmatrix} \begin{bmatrix} \frac{di_a}{dt} \\ \frac{di_b}{dt} \\ \frac{di_c}{dt} \end{bmatrix} + \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} - \begin{bmatrix} u_n \\ u_n \\ u_n \end{bmatrix},$$
(1)

where: u is a motor phase voltage, L is an inductance, M is a mutual inductance, i is a phase current, e is a back electromotive force, R is a phase resistance.

Voltage of neutral point (u_n) is determined from the relationship:

$$u_{n} = \frac{1}{3} \left(\sum_{i=a}^{c} u_{i} - \sum_{i=a}^{c} e_{i} \right).$$
⁽²⁾

The motor movement equation is described by the following relationship:

$$J\frac{\mathrm{d}\omega_m}{\mathrm{d}t} = T_e - T_{lt} - T_{lo}\,,\tag{3}$$

where ω_m is an angular velocity, T_e is an electromagnetic torque, T_{lt} is a load torque, T_{lo} is a mechanical loss torque, T_m is a total mechanical loss torque, J is a moment of inertia.

In order to simplify the motor model, a quantity of the Ψ_k – relative excitation coefficient associated with *k* phase winding was introduced. The excitation coefficient value changes with the angle of the rotor rotation and is described by the following relationship:

$$\Psi_k(\vartheta) = f_k(\vartheta),\tag{4}$$

whereby the relationship between the electrical angle and the rotor angular velocity is described by the following relationship:

$$\omega_m = \frac{1}{p} \frac{\mathrm{d}\vartheta}{\mathrm{d}t},\tag{5}$$

where: ϑ is an angle of rotor rotation,

The relative value of the excitation coefficient in relation to the angle of the rotor rotation is shown in Fig. 3.

The relative values of the excitation coefficient for individual phases are shifted in relation to each other by $2\pi/3$:

$$\Psi_a(\vartheta) = f(\vartheta), \tag{6}$$

$$\Psi_b(\vartheta) = f\left(\vartheta - \frac{2}{3}\pi\right),\tag{7}$$



Fig. 3. Relative excitation coefficient in relation to the angle of rotation

The BLDC motor electromagnetic torque is determined on the basis of the following relationship:

$$T_e = \frac{1}{\omega_m} \left(e_a i_a + e_b i_b + e_c i_c \right). \tag{9}$$

The motor back electromotive force is linearly related to the angular velocity:

$$e_k = p \Psi_b(\vartheta) k_{\Psi} \omega_m \,. \tag{10}$$

By substituting Equation (10) to (9) and including (6)-(8), an equation describing the electromagnetic torque is obtained:

$$T_e = pk_f \left[f(\vartheta)i_a + f\left(\vartheta - \frac{2}{3}\pi\right)i_b + f\left(\vartheta + \frac{2}{3}\pi\right)i_c \right], \tag{11}$$

where:

$$t_e = \frac{L}{R}, \qquad (12)$$

$$t_m = \frac{R \cdot J}{k_f k_{\Psi}},\tag{13}$$

where: f_k is a relative k phase flux coefficient, k_f is a torque constant, p is a pole pair number. Table 1 lists the motor parameters assumed for the simulation.

> - 10.1515/aee-2016-0034 Downloaded from De Gruyter Online at 09/19/2016 10:49:37AM via free access

467

(8)

11	D		
1/1	8/187	vnsi	ĸı
111.	Dusz	$v i \omega i$	vı

Item	Type name	Value
1	maximum speed	1,500 rad/s
2	inductance	1 mH
3	mutual inductance	0.5 mH
4	rotor moment of inertia	$45 \cdot 10^{-3} \text{ kg m}^2$
5	excitation coefficient	0.025 V/rad/s ⁻¹
6	winding resistance	1 Ω
7	maximum load torque	$1.5 \cdot 10^{-3} \text{Nm}$
8	electromechanical time constant (t _m)	6 s
9	electrical time constant (t _e)	$1 \cdot 10^{-3} s$

Table 1. List of motor parameters used in the simulation

3. Numerical calculation

3.1. Floating point operations

Assuming that the model state variables are described by 64-bit numbers, and assuming a fixed point representation with an 11-bit integer part and a 52-bit fractional part, the smallest writeable value in this format is $1 \cdot 2^{-52}$. On the other hand, for a 64-bit floating point representation compliant with IEEE 745-1985, the notation precision is $5 \cdot 2^{-324}$.

The basic type used for storing floating point numbers and performing arithmetic operations [22, 23] on them is the *SIGNED*-type with a size of 64 bits.

3.2. Numerical calculation method

The mathematical model realization of FPGA requires the implementation of a numerical method enabling the calculation of differential equations. Equations describing the mathematical model of the BLDC motor are first order linear differential equations.

A solution that offers better results than Euler methods [13] is employing a method of a higher order, e.g. the Runge-Kutta method or the Adams-Bashforth method. Unfortunately, this entails greater simulation complexity [13]. The major advantage of the Adams-Bashforth method over the Runge-Kutta method is that only one evaluation of the integrand is performed for each step. Therefore the Adams-Bashforth multistep method was chosen for the implementation, with a small time step of $T_s=1 \ \mu s$. The adopted time step complies with the recommendations for the simulation of Ultra Fast Transient objects presented in [24].

The sampling time was selected taking into account:

1) The Kotelnikov-Shannon theorem. The frequency of the highest harmonic of the analyzed waveform must be at least two times lower than the sampling frequency. The frequency of the base harmonic of the BLDC motor current is equal to the motor rotation frequency. Moreover, there are also four consecutive frequencies in the current (2nd, 3rd, 4th and 5th), and the highest harmonic with the frequency of transistor switching. The highest

frequency of the harmonic (f_h) connected with the motor rotational speed for the analyzed case is equal to 1.2 kHz (f_h = 5· f_r where f_r is the frequency of the rotor for the maximum rotational speed from Table 1). On the other hand, the frequency of the current harmonic originating from transistor switching (15 kHz) is 66 times lower than the sampling frequency ($1/T_s$). This implies that the sampling frequency has been selected properly in relation to the switching frequency.

2) Excessive increasing of the calculation frequency results in the lowering of the precision of the obtained results. This ensues from the method's calculation errors, and the errors connected with inaccurate digital representation of the real numbers being summed up in successive steps. The time step should be selected on the basis of estimating the calculation method errors. If decreasing this step does not cause a significant reduction of the method error, then the frequency should not be increased, because this would cause an increase of the summed error of real number rounding. Therefore, the calculation frequency can only be increased if the accuracy of real number representation permits it [26]. In the presented solution, it has been determined experimentally that increasing the calculation frequency above 1 MHz does not cause a significant reduction of the method errors, therefore this calculation frequency has been adopted.

Table 2 presents a comparison of the absolute values of the errors after 30 minutes of calculations originating from real number rounding and determined by the Adams-Bashforth method at various calculation steps for fixed-point (Q52) and floating-point notations (both for 64-bit notation).

Time step	Floating point	Fixed point
1 µs (1 MHz)	$1.58 \cdot 10^{-87}$	$2.39 \cdot 10^{-6}$
0.5 µs (2 MHz)	$3.16 \cdot 10^{-87}$	$4.79 \cdot 10^{-6}$
0.2 µs (5 MHz)	$7.9 \cdot 10^{-87}$	11.99·10 ⁻⁶

Table 2. Absolute values of errors

3. Ensuring numerical stability with respect to the time constants of the object. Stability condition for integration steps for selected numeric method [27]:

$$T_n \cdot \lambda < 1 \,, \tag{14}$$

where λ is the eigenvalue (circuit time constant).

Due to the high circuit time constant values (6 s and 100 ms) this step is sufficient, and the numerical operation stability (the numerical stability condition (14) is fulfilled for both time constants).

4. Closed control system

In the simulation, a classic closed control system was used with a speed regulator and a current regulator. Fig. 4 shows a system of this type.



Fig. 4. Inverter control system diagram

The master speed regulator has a proportional structure (P) and a slave current regulator with proportional integral structure (PI). The diagram shown in Fig. 4 assumes the following labels: H_A , H_B , H_C are signals from the Hall effect sensor determining the rotor position in relation to the stator; *SAW* is a symmetrical sawtooth course generator; *ABS* is an absolute value; *KS* is a sign comparator; i_{xF} is the phase current of phase $x \{a, b, c\}$; U_d is DC link voltage; ω_{zs} is a speed reference.

An overcurrent protection was employed in the control system, blocking transistor control pulses if a momentary current value of any of the phases exceeded the allowable value (i_{ov}) . If the value of the link circuit capacitor voltage (U_d) was lower than the assumed minimum value (u_{min}) , the speed set to the speed regulator equaled zero. This functionality was realized by the multiplexer (*MUX*) and the "*DC Link Monitoring*". The aim of this operation is to prevent the motor from starting until the front-end converter sets the correct voltage on the capacitor and to force switching to the generator operation when the DC link circuit capacitor voltage drops below the assumed value (e.g. in the event of the mains converter damage). The "dead time" of the converter is executed by a program and is changed globally for all three blocks.

For the implementation of the current and speed regulators algorithms, the VHDL language was used. To simplify the regulator structure, the regulator algorithm described in [28] was used.

The "speed measurement" block (Fig. 4) was developed using the VHDL language according to the speed determination algorithm, based on signals from all shaft position sensors and providing six measurements for one revolution [28] for the motor with one pair of poles.

5. Simulation implementation in the FPGA

5.1. Back electromotive force

To solve equation (1), an instantaneous value of back electromotive force (back EMF) is required. On the basis of Equations (6)-(8) and the Look Up Table (LUT) method, it is possible to define one common table storing instantaneous EMF values depending on the current

angle of the rotor rotation of the motor. The angle of the rotor rotation can be calculated by the transformation of Equation (5) into the form of continuous time or within the scope of discrete time (k):

$$\vartheta = \int \omega_m dt + \vartheta_0 , \qquad (15)$$

$$\vartheta(k) = T_s \sum_{i=0}^{k-1} \omega_m(i), \qquad (16)$$

Since the course of the relative value of the flux coefficient is symmetrical, it suffices to store only 1/6 of the rotation period in the table. In the simulation, it was assumed that the table stores 1.023 points of the relative value of flux coefficient (4), which ensures sufficient resolution. Additionally, the number of table elements is divisible by three, which enables the precise realization of the phase shift.

5.2. Mechanical losses in a real BLDC

In the motor movement Equation (3), the mechanical loss torque and coefficient of friction appear. In order to ensure the realism of the simulation, these parameters were determined experimentally in a drive with parameters similar to the simulated one. During free coasting, the motor electromechanical torque (T_e) equals zero. Hence, Equation (3) is reduced to the following form:

$$J\frac{\mathrm{d}\omega_m}{\mathrm{d}t} = -T_m(\omega_m). \tag{17}$$

On the basis of (17), by the knowledge of the moment of inertia of the rotor and by recording the speed during free coasting, it is possible to determine the mechanical loss torque of the drive. The recorded characteristics were approximated using the square error minimization method with the function:

$$\omega_m(t) = -0.3158t^3 + 17.98t^2 - 106.14t + 1582.95.$$
⁽¹⁸⁾

Using (18) and Equation (17), the mechanical loss torque was determined in the speed function and approximated with the following equation:

$$T_m(\omega_m) = 3 \cdot 10^{-9} \,\omega^2 + 8 \cdot 10^{-6} \,\omega_m + 0.0271 \,. \tag{19}$$

The final Equation (3) for a sample motor takes the following form:

$$J\frac{\mathrm{d}\omega_m}{\mathrm{d}t} = T_e - T_{lt} - \left(3 \cdot 10^{-9}\,\omega^2 + 8 \cdot 10^{-6}\,\omega_m + 0.0271\right). \tag{20}$$

5.3. Converter model

In order to execute the simulation of the motor feeding a converter power circuit, a behavioral model was assumed. The motor feed method and inverter transistor numbering are shown in Fig. 2. Table 3 lists the values of the voltages u_a , u_b , u_c , depending on the switched on transistors [30].

After the transistor opening, the current flow in the circuit is supported by the energy accumulated in the motor inductances, input chokes and back EMF. The current then flows through the diodes located in the branch of the previously conducting transistors and the link circuit capacitor (e.g. after opening transistors T_1T_2 , diodes D_4D_6 begin conduction (Fig. 2)). In this topology, the voltage bias on the motor terminal changes, while the value of this voltage remains unchanged. The diodes conduct the current until the transistor switches on or when the current value decreases to zero. The converter model does take into account the transistor/diode switch on/switch off times or the voltage drops on the structures thereof. However, dead times were taken into account, executed by a program within the control system structure.

Closed transistors	u _a	u _b	u _c
$T_{1}T_{2}$	$+U_{d}/2$	$i_b = 0$	$-U_d/2$
$T_{2}T_{3}$	$i_a = 0$	$+U_{d}/2$	$-U_d/2$
T_3T_4	$-U_{d}/2$	$+U_{d}/2$	$i_c = 0$
T_4T_5	$-U_{d}/2$	$i_b = 0$	$+U_{d}/2$
T_5T_6	$i_a = 0$	$-U_{d}/2$	$+U_{d}/2$
T_6T_1	$+U_{d}/2$	$-U_{d}/2$	$i_c = 0$

Table 3. Inverter state

5.4. Realization of the simulation

Since in the real system, the ADC measurement time interval is 20 times shorter than the assumed motor model time step (T_p) , in order to provide the control system with conditions similar to the actual ones, a zero-order hold (ZOH) was used. The ZOH simulates the operation of the real ADC. The ZOH operation frequency and the trip points are synchronized with a sawtooth generator (PWM modulator).

Fig. 5 shows connection diagram in BLDC motor model execution, generated by RTL (Register Transfer Level) Viewer tool from the Quartus II suite [29]. Fig. 5 also presents physical connections and relationships between individual simulation elements. The clock frequencies are utilized by the simulation fragments. The block responsible for motor model numerical calculations uses two clocks, 1 MHz and 50 MHz. All the processes performing the floating point calculations are timed by the 50 MHz clock, while the 1 MHz clock is used to synchronize the results between the processes and for the timing of the registers storing calculation results for successive numerical operation steps.

The "emf_BLDC_table" block is responsible for the generation of the waveform of the relative values of the excitation coefficient (Eqs. (6)-(8)). This coefficient values are transmitted in the fixed point format (Q31) to the "speed_emf" block, which determines the motor electromotive force on the basis of the motor speed.



Fig. 5. Connection diagram of BLDC motor generated by RTL tool

473

174	M. Baszyński		Arch. Elect. Eng.
-----	--------------	--	-------------------

Table 5 presents the execution times of the floating-point operations for two different clocks: 50 MHz and 450 MHz (the FPGA maximum PLL output frequency). On the basis of data from Table 4 the maximum time necessary for executing one step of the Adams-Bash-forth numerical method was determined: with a 50 MHz clock, a single step takes 740 ns; and with 450 MHz, a single step takes 86.7 ns.

Operation	50 MHz	450 MHz
Add/sub	300 ns	33.3 ns
Multiplication	240 ns	26.7 ns

Table 4. Floating point operation execution time

6. FPGA board

In the implementation of the motor model and control system, the Cyclone III FPGA Development Board is equipped with the Altera Cyclone III FPGA (symbol: EP3C120F780C7N). Table 5 lists data on the use of logic elements and multipliers in the simulation. The Development Board was accompanied by a digital-to-analog converter (DAC) circuit.

Item	Feature	Multipliers	Logic elements
1	Control system	0	410
2	Motor model	118	67.541
3	Back EMF table	24	783
4	Angle counter – Eq. (14)	6	310
5	Inverter model	0	3
6	Digital-to-analog interface	0	405

Table 5. List of FPGA used resources

6.1. Simulation results

6.1.1. Open feedback loop

The model was validated by the studies performed using an open feedback loop. Fig. 6 show EMF courses for different rotational speeds.

High level of noise is caused by an accepted analog data acquisition method. To ensure the high speed of processing, the output voltage of the digital-to-analog converter was settled at a relatively low value.

Fig. 7a and Fig. 7b show phase current courses for different recording time bases. In the courses in Fig. 7b, the current commutation points are marked during the current switching between successive motor windings. The comparison between a real motor phase current and a phase current from mathematical model was made to validate the quality of the RTs (Fig. 7c). The parameters of the model were similar to the real motor. Duty cycles for both

via free access

experiments were equal to 0.7. The ripple current and time constant for both courses are identical. This proves correctness of the RTs.

Fig. 6. Back EMF courses for: a)10,512 rpm speed; b) 6,852 rpm speed

Fig. 7. Phase current courses recorded at 5,450 rpm speed at a) time base 2 ms/div b) 400 us/div c) phase current of the real motor and RTs

Fig. 8 shows (phase current, angular velocity, mechanical torque) courses recorded at the constant duty cycle and a step change of the load torque.

Fig. 8. Current, rotational speed and load torque courses

The courses in Fig. 8 correspond to the expected ones. At the constant duty cycle and the step change of the load torque of the motor, the rotational speed decreases and thereby the maximum value of rotation electromotive force decreases, which in turn results in an increase of the momentary value of the phase current. After the mechanical load torque decreases, the speed and back EMF increase while the value of the current decreases.

	D		
<u> </u>	Race	11200	21
1111	1111.5/	vnn	\ ./
		,	**

6.1.2. Closed feedback loop

The control system has been verified with respect to the delays introduced by its individual elements. Table 6 presents the worst cases of delays determined using the TimeQuest Timing Analyzer tool.

Item	Name	Delay
1	Speed regulator	6.694 ns
2	Current regulator	21.294 ns
3	PWM generator	8.702 ns

Table 6. Delays of the control system

It ensues from the table that the total delays introduced by the control system do not exceed 36.69 ns. Regarding the operation frequency of the control system, this is a negligibly short time.

Fig. 9a shows courses of set speed (ω_{zs}), rotational speed (ω_m) and the current of one of the motor phases. Fig. 9b presents courses of the current of one of the motor phases, load torque and angular velocity.

Fig. 9 a) phase current, set speed and rotational speed courses b) step change of the load

Fig. 10a shows the courses of the back EMF values and the phase current during the motor operation and Fig. 10b presents the same courses during the generator operation.

Fig. 10. Phase current and back EMF courses during a) the motor operation; b) generator operation

The delay in increasing of the motor phase current after the step change of the load torque (Fig. 10) is caused by the algorithm used for the motor speed measurement [26] (measurement result after 1/6 revolution).

7. Conclusions

This article presents the BLDC motor simulation execution based on its FPGA-implemented mathematical model. To solve the differential equations describing the motor, the Adams-Bashforth method was used. To describe the variables representing of the motor state, the floating point notation was used, allowing the obtaining of a higher calculation precision (with regard to the fixed point description). The model's functioning was verified in both open and closed feedback loops.

Additionally, the paper presents the methodology and the RTs execution method that enable the testing of the control system and protections for the BLDC motor. The main advantage of the described method is the fact that it only utilizes the standard tools offered by FPGA manufacturers. Owing to that and to the use of inexpensive FPGAs (Cyclone III family), it is possible to execute the simulation without additional costs for purchasing a specialized program or simulation platform. In order to execute the described simulation, a free version of the Quartus II software is sufficient.

Acknowledgements

This work is supported by Narodowe Centrum Badań i Rozwoju (NCBR) under the program of GEKONGenerator Koncepcji Ekologicznych, a common initiative of Narodowy Fundusz Ochrony Środowiska i Gospodarki Wodnej (NFOŚiGW) under the project: nr GEKON1/02/213877/31/2015 pt "Rewitalizacja prosumenckich mikroinstalacji energoelektrycznych".

References

- Dziadecki A., Grzegorski J., Skotniczny J., Sensorless control system of SRM drive, Przegląd Elektrotechniczny 88(8): 317-322 (2012).
- [2] Chun T.W., Tran Q.V., Lee H.H., Kim H.G., Sensorless Control of BLDC Motor Drive for an Automotive Fuel Pump Using a Hysteresis Comparator, IEEE Trans. on Power Electronics 29(3): 1382-1391 (2014).
- [3] Nikam S.P., Rallabandi V., Fernandes B.G., A High-Torque-Density Permanent-Magnet Free Motor for in-Wheel Electric Vehicle Application, IEEE Trans. on Industrial Application 48(6): 2287-2295 (2012).
- [4] Joice C.S., Paranjothi S.R., Kumar V.J.S., Digital Control Strategy for Four Quadrant Operation of Three Phase BLDC Motor With Load Variations, IEEE Trans. on Industrial Informatics 9(2): 974-882 (2013).
- [5] Berrached D., Tilmatine A., Miloua F., Bengrit M., Modeling of a two stages electrostatic air precipitation process using response surface modeling, Archives of Electrical Engineering (63): 609-619 (2014).
- [6] Gawrylczyk K.M., Banaszak S., Modeling of frequency response of transformer winding with axial deformations, Archives of Electrical Engineering 63(4): 5-17 (2014).

11	D	/ 1	
M	Rasz	vnsk	1
	Dusz	ynon	r i

- [7] Ta M.C., Dufour C, Real-time simulation and control of reluctance motor drives for high speed operation with reduced torque ripple, IECON - 37th Annual Conference on IEEE Industrial Electronics Society, pp. 4176-4181 (2011).
- [8] Xu S., Liu X., Sun W., Modelling of power metal-oxide semiconductor field-effect transistor for the analysis of switching characteristics in half-bridge converters, IET Circuits, Devices & Systems 4(4): 327-336 (2010).
- [9] Jia K., Bohlin G., Enohnyaket M., Thottappillil R., *Modelling an AC motor with high accuracy in a wide frequency range*, IET Electric Power Applications 7(2): 116-122 (2012).
- [10] Dufour C., Belanger J., Lapointe V., FPGA-based ultra-low latency HIL fault testing of a permanent magnet motor drive using RT-LABXSG, Proc. IEEE Int. Power Sys. Tech. Conf., pp. 1-7 (2008).
- [11] Dong L., Guang-fu T., Zhi-yuan H., Hui P., A New Type Real-Time Simulation Platform for Modular Multilevel Converter Based HVDC, Power and Energy Engineering Conference (APPEEC), pp. 1-5 (2012).
- [12] Olivieri C., Di Leonardo L., Fabri G., Tursini M., A DSP-based real-time simulation equipment for fast motor control development, Education and Research Conference (EDERC) 5th European DSP, pp. 208-212 (2012).
- [13] Kokenyesi T., Varjasi I., Comparison of real-time simulation methods for power electronic applications, Energy 4th International Youth Conference on (IYCE), pp. 1-5 (2013).
- [14] Montoya L.A., Montenegro D., Ramos G., Adaptive protection testbed using real time and hardware-in-the-loop simulation", PowerTech (POWERTECH), Grenoble, pp. 1-4 (2013).
- [15] Bazargan D., Filizadeh S., Hardware-in-loop real-time simulation of a battery storage system in a wind generation scheme, Electric Power and Energy Conversion Systems (EPECS), 3rd International Conference on, pp. 1-6 (2013).
- [16] Wang C., Li W., Belanger J., Real-time and faster-than-real-time simulation of Modular Multilevel Converters using standard multi-core CPU and FPGA chips, Industrial Electronics Society (IE-CON), 39th Annual Conference of the IEEE, pp. 5405-5411 (2013).
- [17] Hanif M., Khadkikar V., Xiao W., Kirtley J.L., Two Degrees of Freedom Active Damping Technique for LCL Filter-Based Grid Connected PV Systems, IEEE Trans. on Industrial Electronics 61(6): 2795-2803 (2014).
- [18] Stala R., Stawiarski L., Real-time models of PV arrays implemented in FPGAs, Przeglad Elektrotechniczny 86(2): 358-363 (2010).
- [19] Pirog S., Baszynski M., Single phase, three cells AC/DC converter with sinusoidal current source, Przegląd Elektrotechniczny 85(3): 42-47 (2009).
- [20] Chen Y., Dinavahi V., Digital Hardware Emulation of Universal Machine and Universal Line Models for Real-Time Electromagnetic Transient Simulation, IEEE Trans. on Industrial Electronics 52(59): 1300-1309 (2012).
- [21] Myaing A., Dinavahi V., FPGA-Based Real-Time Emulation of Power Electronic Systems With Detailed Representation of Device Characteristics, IEEE Trans. on Industrial Electronics 58(1): 358-368 (2011).
- [22] Sohn J., Swartzlander E. E., *Improved Architectures for a Fused Floating-Point Add-Subtract Unit*, IEEE Trans. on Circuits and Systems 59(10): 2285-2291 (2012).
- [23] Chong Y.J., Parameswaran S., *Configurable Multimode Embedded Floating-Point Units for FPGAs*, IEEE Trans. on Very Large Scale Integration (VLSI) Systems 19(11): 2033-2044 (2011).
- [24] Menghal P.M., Laxmi A.J., *Real time simulation: Recent progress & challenges*, Power, Signals, Controls and Computation (EPSCICON) International Conference on, pp. 1-6 (2012).
- [25] Hasanzadeh A., Edrington C.S., Stroupe N., Bevis T., Real-Time Emulation of a High-Speed Microturbine Permanent-Magnet Synchronous Generator Using Multiplatform Hardware-in-the-Loop Realization, IEEE Trans. on Industrial Electronics 61(6): 3109-3118 (2014).
- [26] Myaing A., Faruque M.O., Dinavahi1 V., Dufour C., Comparison of insulated gate bipolar transistor models for FPGA-based real-time simulation of electric drives and application guideline, IET Power Electronics 5(3): 293-303 (2011).

- [27] Chua L.O, Lin PenMin, Computer-aided analysis of electronic circuits: algorithms and computa tional techniques, Prentice-Hall (1975).
- [28] Baszynski M., Pirog S., A Novel Speed Measurement Method for a High-Speed BLDC Motor Based on the Signals From the Rotor Position Sensor, IEEE Trans on Industrial Informatics 10(1): 84-91 (2014).
- [29] http://www.altera.com/literature/hb/qts/qts_qii51013.pdf, accessed April 2015.
- [30] Gurumurthy S.R., Agarwal V., Sharma A., Optimal energy harvesting from a high-speed brushless DC generator-based flywheel energy storage system, IET Electric Power Applications 7(9): 693-700 (2013).