8. VLSI System Design

Module	Topics	Hrs	Fees (Rs.)
Integrated Circuit Analysis and Design	1. **Semiconductor device physics:** Introduction, concepts of basic semiconductors, operation of diode and its terminal characteristics, analysis of diodes, physical structure and operation of BJT, characteristics of BJT, small signal models and second order effects. Case study. 2. **MOS transistor theory:** Introduction, structure, operation of enhancement and depletion type MOS transistor, current-voltage characterization of MOS transistor, biasing of MOS transistor, small signal model of MOS transistor, second order effect- body effect, channel length modulation, subthreshold effect, hot electron effect, tunnelling, punch through. MOS transistor capacitances, model parameters, different level of MOS model equations, modelling of MOS transistors using SPICE and scaling of MOS transistors. Case study of modelling MOS devices and extracting model parameters. 3. **CMOS inverter design:** Introduction, types MOS inverter, resistive load inverter, depletion load inverter, CMOS inverter, design of CMOS inverter, DC (static) characteristic analysis - voltage transfer characteristic and noise margin. Transient (dynamic) analysis - propagation delay, rise time and fall time calculation. CMOS inverter static and dynamic power, CMOS inverter load capacitance and interconnection parasitic. Case study of CMOS inverter design for noise margin, speed, power and timing 4. **Combinational and sequential CMOS logic circuits:** Introduction, CMOS logic circuits, complex logic circuits, clocked CMOS logic, pass transistor logic, CMOS transmission gates, problems of charge sharing, precharging techniques. Behaviour of bistable elements, timing metrics, SR latch and flip-flop circuits, mux based latches, clocked latch and flip-flop circuit. Case study of combinational and sequential circuits for timing, area and power 5. **Logical effort:** Introduction, transistor sizing, delays in CMOS logic gates, fan-in and fan-out consideration, fast complex gate techniques, computing of logical effort, path and branch effort, multistage delay and best stage effort. Case study of CMOS circuit design using logical effort. 6. **Memory design :** Introduction, need for memories, classification of memories, Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM), memory architectures, 6T SRAM memory cell architecture, peripheral memory circuitry - sense amplifier,	80Hrs	Rs.12000.00

	read/write circuitry, bit line precharge circuitry, row and column decoders and memory timing. 7. **Data path subsystem:** Introduction, arithmetic logic circuits, classification of adders, design of mirror adder, ripple carry adder, Manchester carry chain adder, carry skip adder, comparison of adders, multipliers and shifters. Case studies of data path subsystems. 8. **Low Power CMOS design:** Introduction, power dissipation, static and dynamic power dissipation, techniques for reduction of power dissipation, low power design through voltage scaling, estimation and optimization of switching activity, reduction of switched capacitance. Case study of optimizing power in CMOS circuits. 9. **Tools used:** Synopsys HSPICE, Cadence Virtuoso, Nanosim, Cadence Pspice, LTspice, Microwind, HSIM		
Full Custom Physical Design	1. **Full custom physical design:** Introduction, challenges and opportunities, nanometre designs, design flow, libraries, technology files, tool set up, industry practices and CAD tools. VLSI fabrication process and DSM/UDSM. Case study. 2. **Layout introduction:** Introduction, MOS transistor layers, varies design styles, stick diagram, symbolic diagram, design rules-lambda and micron rules 180nm, 90nm, 65nm, 45nm. Layout and physical verification, type's full custom layout - data path layout, custom digital layout, cell layout and analog layout. Case study. 3. **Digital layout design:** Introduction, guide line of transistor layout, pMOS and nMOS transistor layout, CMOS transistor layout, sharing diffusion methods, optimization of schematic diagram using dual graph methods and Euler's path. Combinational and sequential circuit layout, guard ring protection for digital circuits. Case study. 4. **Analog MOS circuits:** Introduction, MOS Device characterization, CMOS current mirrors, single stage amplifier – common source amplifier, common drain amplifier and common gate amplifier. Design of differential amplifier and two stages CMOS Opamp. Design of resistors, capacitors and inductors. Case study. 5. **Analog layout design:** Introduction, analog layout techniques, multi finger, interdigitization, axis of symmetry, common centroid, centroid of array, matched device technique, dummy devices on surrounding. Passive component layout - capacitor, resistor and inductor. Case study. 6. **Mixed signal layout issues:** Introduction, floor planning of analog and digital components, power supply and ground pin issues, matching, shielding, interconnection issues. Case study	80Hrs	Rs.12000.00

	7. **Standard cell layout:** Introduction, classification of STD cell, standard cell design consideration, cell setting, STD cell layout template creation. STD cell Performance for varies process corners, Case study 8. **Reliability issues:** Introduction, electro migration, electro migration reduction techniques, cross talk, effects of cross talk, IR drop, antenna effect, hot electron effect, latch up problem and latch up prevention. Case study 9. **Nanometer design issues and Layout:** Introduction, mask error, optical proximities correction, phase shift masking, resolution enhancement technique, gate oxide integrity, metal erosion and metal over etching. Case study. 10. **Tools used:** Synopsys HSPICE , Cadence Virtuoso, MATLAB, NanoSim, HSIM		
Field Reconfigurable Hardware Systems	1. **Introduction:** Introduction to VLSI systems, Introduction to reconfigurable systems, Need for reconfigurable systems, Introduction to design flow, Two competing implementation - ASIC & FPGA , Major FPGA vendors, The reconfigurable marketplace, PLD market share, Std Cell ASIC Development Cost Trend, Today's typical design, Importance of reconfigurable systems in VLSI design, Application for reconfigurable systems, Future of reconfigurable systems, Introduction to FPGAs, Need of FPGAs in DSP Applications, DSP Processors vs. FPGAs, Product Roadmap, Review of PLA, PAL, Introduction to PLDs, Concept of CLB, Interconnect structure, ROM, PROM, Introduction to FPGA, FPGA vendors, FPGA structures 2. **RTL Coding for Synthesis:** Introduction to RTL coding, Introduction to synthesis, Rules for combinational circuit's synthesis, Avoiding unwanted latches, Rules for sequential circuit's synthesis, Position dependent code, Resource sharing,, case, casex, casez etc.., Synthesizable and non synthesizable constructs, Case study – UART 3. **Advanced Digital Design:** Multipliers, Booth encoding scheme, Wallace tree, FIFO modelling, Finite state machines, FSM modelling in Verilog, Functions and Tasks, UDPs, Case study – FIFO 4. **FPGA Architectures:** XILINX FPGA Architectures, Anti-fuse and SRAMS, Logic elements and Look-up Tables, Dedicated multipliers, Reconfigurability, Distributed RAM, Shift registers, Digital Clock Managers, Macros, Spartan III and Virtex Architectures 5. **FPGA Implementation:** FPGA programming, Translate, Map, Floorplan, Place and Route, Post map and Post P&R simulation, UCF constraints, Manual mapping and placement, Reading and analysing reports-post synthesis, Post map simulation, Post P&R simulation, Configuring	80Hrs	Rs.12000.00

	FPGAs, FSM Extraction, Case study - Dual elevator controller 6. **Constraints:** Timing analysis, Area Constraints, Slack calculation, Data loss due to large skew, Maximum skew calculations with examples, Period constraints, OFFSET IN, OFFSET OUT Constraints, Multi cycle path, Timing constraints priority 7. **FPGA Debugging and Advanced FPGA:** Introduction to FPGA Debugging, Debugging using chip scope, Dual edge triggered FFs, Clock domains, Reset circuits, IP cores 8. **Tools Used:** Xilinx ISE, ModelSim, ChipScopePro, System Generator		
Reliable Power Aware ASICs	1. **Introduction to semi custom design flow:** Introduction to semi-custom ASIC design flow, Challenges and opportunities, Need for semi-custom ASICS, Scope of semi-custom ASICs, Industry Trends, Market reach and market share of semi-custom ASICs in VLSI (Very Large Scale Integrated Circuit) Industry, Overview of industry standard tools, Salient features of semi-custom ASICs, Levels of abstraction in VLSI designs, and Semi-custom oriented HDL coding 2. **Standard Cell Libraries for DSM:** Different kinds of libraries and their relevance, Operating conditions, Wire-load models, Timing models, Timing arcs, Kinds of standard cells at 130nm, Cell attributes, Footprints, Naming conventions 3. **Timing Analysis in Digital Designs:** Terminologies in timing analysis, Various kinds of timing paths, Properties of clock, Clock skew, Timing window and timing violations, Remedies for timing violations, Concept of slack, Critical path, Equations for timing calculations, Solving complex timing problems 4. **Synthesis and Constraints:** Synthesis requirements, Synthesis process, Pareto points, Realization of constraints from specifications, Classes and significance of constraints, Environmental & optimization constraints, Design rule constraints, Timing and power constraints, Point-point exceptions, Chip level constraints, Case study - Complex sequential designs e.g., Systolic Array Multiplier 5. **Optimization & Low Power Techniques:** Two level Optimization, Multi-Level optimization, Scheduling and allocation algorithms, Design abstraction levels, Representation domains, Control flow graph, Data flow graph, High level transformations, Low power techniques, Dynamic and leakage power optimization, Multi-VDD, Multi VTH, Retention registers, Top-down and bottom-up synthesis, Characterizing and propagating the constraints,	80Hrs	Rs.12000.00

	Register pipelining, Multi-Cycle paths, Case study - Communication block e.g., QAM 6. **Introduction to VLSI Testing**: Need for testing, Importance of testing, Role of testing, Trends in testing, Test cost estimates, DFT cycle, Basic definitions like defect, fault and error, Testing at different levels, Difficulties and challenges of VLSI testing, VLSI chip yield, Fault coverage and defect level, Discussion of reliability issues, Basics of DFM 7. **Fault Modelling & Fault Simulation:** Importance of fault modelling, Single stuck at fault, Multiple stuck at faults, Bridging faults, Pattern sensitive faults, Transistor faults, Cross point fault, Delay fault, Test and test set, Fault collapsing, Fault simulation concepts, Fault simulation approaches 8. **Design For Testability (DFT):** DFT Introduction, Controllability, Observability, Need for DFT, DFT techniques, Adhoc DFT, Structured DFT, Scan based design, Scan flip-flop, Different scan types, Scan design rules, RTL for DFT, Test mode vs. Scan mode, DFT DRC rules, Scan clock skew, Multiple test insertion, Adding scan structure, Scan overheads, Testing scan registers - Case study Asynchronous FIFO/ NCO 9. **Static Timing Analysis (STA):** Necessity of STA, Advanced timing analysis, Recovery time, Removal time, Importance and consequence of timing exceptions, False paths, Directed acyclic graphs, Bottleneck analysis, Case analysis, Mode analysis, Path groups, DFT aware timing schemes, Timing analysis of low power designs, On-Chip variation - Case study QAM / NCO 10. **Built In Self Test (BIST):** BIST Architecture, Pseudo-Random generators, Signature analysis, Liner Feedback Shift Registers (LFSR) as pattern generators, LFSR as signature analyzers, Built In Logic Block Observers (BILBO) 11. **SYNOPSYS:** Design Compiler, PrimeTime, Formality, DFT Compiler 12. **CADENCE:** RTL Compiler		
IC Planning and Implementation	1. **Introduction:** Introduction to semi-custom ASIC flow, need and importance of physical design flow, overview of EDA tools for semi-custom IC design flow 2. **Data Preparation process:** Introduction to data preparation functions performing essential tasks for cell libraries which includes creating cell libraries, importing cell data, translating and loading CLF timing data, specifying technology information, power and ground port types, optimizing the standard cell layout, extracting pin and blockage information, setting place and route boundaries and define wire tracks	80Hrs	Rs.12000.00

	3. **Chip input and output pads:** Introduction to IO cells, types of analog and digital IO cells available in library physical specification of a standard IO cell, IO power and ground rail structure arrangement for regular and high tolerant IO cells , types of bond pad structures in the IO cell, simultaneous switching noise (SSN), Simultaneous switching output (SSO), driving index (DI) and factor (DF), concept and types of IO packaging, Flip chip IO cell and EM enhancement 4. **Floorplanning and implementation:** Introduction to floor planning, differentiating between core limited and pad limited design flow, TDF/IO constraint files, defining best aspect ratio, core utilization, chip utilization, flat and hierarchical design flow, partitioning based on timing and interconnects information for hard macros, creating a physical layout. 5. **Power Planning and Management:** Need for power management, core and IO level power estimation, limitation of core level and IO level power, top to bottom, bottom up approaches, estimating power budget for flattened and hierarchical designs, placement of power mesh (rectangular rings, straps, trunks) and power pads based on IR and EM based criteria 6. **Setup and Analyze Design Timing:** Checking design data, loading timing constraints, setting up the environments for library, delay model, parasitics, optimizations, clock and net transition, maximum capacitance constraints on clock domains, TLU+ capacitance and resistance model, analyzing and probe timing paths 7. **Placement and optimization:** Introduction to placement, standard cell and macro/DEF placement, timing driven and taming the congestion, detaching scan chains, location constraints, high fan-out net synthesis, placement optimization tasks, power optimization, area recovery 8. **Clock Tree Synthesis (CTS):** Introduction to CTS, physics of CTS, algorithms for CTS, single and distributed driver scheme, path length and its delay models for skew analysis, balanced clock tree, buffer insertion, constraints and device sizing under process variation in CTS, clock distribution network, low skew and power based global, local and useful skew analysis and optimization methodologies. 9. **Routing and Optimization techniques:** Taxonomy of routing, routing algorithms, channel and switch box routing, balanced, and H tree clock routing, routing operations and optimization, density driven routing, post route optimization for timing, performing design finishing processes, optimizing yield, interactively cleaning up routing DRC, LVS check and errors, antenna checking and fixing violations, crosstalk prevention, analysis and fixing		

	10. **Design Signoff:** Introduction to design signoff, data preparation flow for power sign off, checking Physical and logical connectivity power information, preparing data for hard/soft macro extracting PG parasitics, performing power and rail analysis based on IR and EM criteria, performing design rule checking and connectivity verification, generating output for back annotation, performing various ECO analysis, industry standard GDII generation 11. **SYNOPSYS:** Astro, Formality, PrimeTime, StarRC-XT, Jupiter XT, Hercules, IC Compiler 12. **CADENCE:** SOC Encounter, First Encounter, FMS, Nanoroute, Voltage storm, Celtic IC		
Full Chip Functional Verification	1. **Introduction to design verification:** Need for verification, verification process, challenges in verification, cost involved, time involved, verification methodologies and techniques, mission and goals of verification, verification plans, verification flow, verification guidelines, HDL, HVL, HDVL, System Verilog for design and verification, verification methodology manual, industry standard verification tools, Low power verification techniques. 2. **Introduction to System Verilog:** System Verilog enhancements to Verilog 2001, Generations of System Verilog standard and enhancements for hardware design, System Verilog dot name and dot star enhancements, Case study on instantiation example for complex ALU. 3. **System Verilog verification features:** Built- in data types, new data types and operators, user defined types, enumerated data types, System Verilog 2 state and 4 state data types, static and automatic variables, verification advantages of 2 state date types, synthesis guidelines, structure declarations, assigning values, passing structures through ports-synthesis guidelines, packed and unpacked arrays, array of structures, unions and packed unions, dynamic & associative arrays, Case study on verification of memory. 4. **System Verilog procedural blocks:** System Verilog specialised procedural blocks, latched procedural blocks, sequential logic procedural blocks, synthesis guidelines, task and function enhancements, passing task/function arguments by name. System Verilog procedural statements for design verification. Enhanced for loops, do while loops, continue and break, unique if else and priority if else, modeling FSM with System Verilog, Case studies on complex FSM implementations 5. **Object Oriented Programming for verification:** OOP terminologies, local and global variables, scoping rules, System Verilog's class data type-defining class objects,	80Hrs	Rs.12000.00

	public Vs private, class methods-inheritance, single inheritance, data hiding, building an object oriented test bench, Case studies on OOP. 6. **System Verilog assertions and interfaces:** Assertions in System Verilog, assertion concepts, immediate and concurrent assertions, controlling assertion messages, case studies on assertion based verification, System Verilog interfaces, interface methods, verification with interfaces, Case study on ATM router interface. 7. **System Verilog randomization:** Introduction, verification strategy using VMM, constraint details, common randomization problems, random control, random generators, random device configuration, agent, scoreboard, checker, driver, monitor and other functional layers, building a complete verification environment, Case study 8. **SystemVerilog functional coverage:** Introduction, coverage types, functional coverage strategies, simple functional coverage example, cover group, coverage options, analyzing coverage data, measuring coverage statistics during simulation, Case study on functional coverage 9. **Advanced verification techniques:** Save verification cycles, bootstrapping the verification process, high-level modeling concepts, coverage directed generation, verification coverage, threads and mail boxes, program and clocking blocks, active and reactive regions, interprocess communication, advanced interfaces, Case study. 10. **Tools Used:** Synopsys and Cadence Tools, NCSIM, ModelSim, VCS		
Reconfigurable Embedded Platforms with FPGA	1. **Introduction to modern embedded system design and SOC design:** Definition and examples of Embedded digital systems with emphasis on communication and networking, SOC design for embedded systems, VLSI design issues for embedded systems – Power, Homogenous and Heterogeneous COREs, Instructions sets, and Addressing concepts for embedded processors – Example Xilinx, MicroBlaze and ARM Thumb instruction sets, Power PC and MicroBlaze register organization, Cache organization for MicroBlaze, interrupt controllers for Embedded processors – example of Power PC and ARM Interrupt controller, memory space for embedded processors like Power PC and MicroBlaze, Pipelines for modern embedded processors e.g. Power PC pipeline 2. **Architectures of common embedded processors:** How to pick the right embedded processor for the application example in network processing, Overview of ARM Architecture overview, ARM AHB/AIX overview for connect	80Hrs	Rs.12000.00

	and buses, AHB, APB, bus protocols. Case study of architecture of a basic AHB/APB bus bridge 3. **Bus architectures and protocols:** Modern on chip interconnect for embedded processors, Need for on chip buses from power and throughput standpoint, Concept of OCP protocol, OCP sockets, Discussion of simple OCP socket design, OCP Core bridges, Case study of designing simple memory controller using OCP interface, Industry standard connect AMBA and its derivatives AXI bus protocol, Hierarchical AHB 4. **Implementation of on chip buses:** Overview of Element interconnect Bus in CELL processor and overview of concepts behind high performance buses on SOCs, Case study of an actual NOC implementation for a high end communication processor with low power implementation, various methods of bus arbitration and implementation of practical low-power bus arbiters on FPGA, Case study of implementation of DMA controller on FPGA 5. **Implementation of communication and networking algorithms on FPGA systems:** Dissecting communication algorithms for HW-SW co-design, Basic elements for executing communication algorithms in embedded Code, optimizing embedded systems through optimization of SW and HW, Case study of implementation of a Wireline MAC on an embedded processor on FPGA 6. **Integration of Embedded processors on FPGAs:** Integration of Xilinx MicroBlaze Core in FPGA. Key issues for CORE integration, Integration of a MicroBlaze core with an on chip bus. Address space optimization for system implementation, JTAG controller with IEEE 1149.1 7. **Power-PC for communication applications:** Example of integration of Power PC in Xilinx FPGA- Key issues for integration –like interfacing, power, memory addressing, interrupt handling, Case study of a communication system example- low cost router for integration of Power PC on FPGA- the design cycle 8. **Xilinx MicroBlaze for networking applications:** Anatomy of a network traffic management application, Ingress Queue and Egress queues, Queue depth, network traffic management, Use of MicroBlaze for managing traffic management, Packet flow control and its implementation on FPGA 9. **Software tools for embedded processors on FPGAs:** Overview of SW tools like compilers, linkers and loaders and methodologies to integrate COREs in FPGA- specific case of Xilinx Micro-Blaze, Case study of design flow and integration of a Xilinx 32 bit processor CORE on FPGA, usage of Xilinx EDK (Embedded Development Kit)		

	10. **Future direction for embedded VLSI systems:** Summary of current technology for embedded processors on FPGA, Future trends including issues of integrating multiple processor CORES on FPGA- case study 11. **Tools Used:** MATLAB/Simulink , Xilinx ISE, Xilinx uCos, Xilinx EDK		
High Speed Systems and Interconnects	1. **Introduction to High Speed Board Design:** PCB Design Environment, History of PCB, Challenges in Modern PCBs, Importance of Interconnect design, PCB Design Considerations, Major types of PCBs, Issues in high speed boards, PCB Design Process, High Speed Design Constraints 2. **Fundamentals of High Speed Design :** Frequency, Time and Distance, Lumped Versus Distributed Systems, Four Kinds of Reactance, Ordinary and Mutual Capacitance & Inductance 3. **Printed Circuit Board Design:** What is PCB, Parts of PCB, Various Chip packages, multilayer PCB, Inductive Coupling, Capacitive coupling, Steps in PCB Design, Physical design Issue. 4. **Transmission Lines:** Basic definitions, Electromagnetic Signal, Time and Frequency domain concepts, Transmission Lines, Lumped Vs Distributed Transmission Line, Microstrip & Stripline, Odd and Even Transmission Line, Reflection and Transmission Lines, Reflection calculations by mathematical analysis. 5. **Crosstalk in High Speed Board:** What is Crosstalk, Near-end and Far-end Crosstalk, Crosstalk Induced Noise, Effect of crosstalk on transmission line parameters, Termination technique to reduce crosstalk, Crosstalk Trends, Design Guidelines and Rules of Thumb 6. **Signal Integrity:** What is signal integrity, Effect of Signal Integrity on Transmission Line, Effect of Crosstalk, Termination, reflection and field solver, Analysis of Signal Integrity, Modeling and Simulation. 7. **Routing of High Speed Signal:** Main issues for routing, Routing topologies, Rise and fall time degradation, Signal Skew, Line Termination, Power distribution and de-coupling, PCB Stackup, Return Path Discontinuities, Ground/Power Bounce, Decoupling Caps. 8. **Basics of Electro-Magnetic Compatibility (EMC) and Electrostatic Discharge (ESD):** Introduction to EMC, Aspects of EMC, EMC and High Speed Design, Electro Magnetic Interference, Various Sources of EMI, Conducted Emissions and Susceptibility, Test and Measurement of EMI, EMC standards , Electro-static Discharge (ESD), ESD Sensitivity, ESD prevention, EMC Vs ESD. 9. **High Speed Board Design for EMI/EMC Compliances:** Definitions, Impact of EMI, EMC Fundamentals, Radiation	80Hrs	Rs.12000.00

	and Conduction, Types of EMI, EMI characterization, Interference due to Signal Integrity, EMI Suppression, Bypassing & Decoupling, Grounding techniques & Trace Routing to protect Interference and ESD Protection. 10. **PCB Materials & Fabrication Process:** Materials used in FPCB, Direct Materials, Indirect Materials, Manufacturing Processes for a Multi-layer PCB, Inner Layer Processing Material Selection, Laminating and Imaging of Internal Layers, Etch Process, Remove Laminating Film, Completed Inner Layer Core, Layer stackup, Bonding Heat and Electro-plating and The designer and manufacturer interaction. 11. **Tools Used:** ORCAD, Allegro full suite		
High Frequency Mixed Signal Circuits	1. **CMOS modeling and process characterization:** Introduction to analog CMOS modelling and process characterization, RF modelling, equivalent circuit representation of MOS transistor, high frequency behavior of MOS transistor and AC small signal modeling, requirements for MOS modeling for RF application, modeling of intrinsic components, HF behavior, extrinsic components, non quasi static behavior, parameter extraction, RF measurements, NQS model for RF applications, noise source in MOS, physical mechanism of flicker and thermal noise models, HF noise parameters, analytical calculation of the noise parameters, induced gate noise and simulations, RF model, gate electrode and intrinsic input resistance model, substrate resistance model, junction diode models, I-V and capacitance model 2. **Data converters:** Introduction to data converters fundamentals, converting, analog signals to digital signals, sample and hold characteristics, DAC specifications, ADC specifications, data converter architectures, DAC architectures, resistor string DAC, R-2R ladder networks, current steering, charge scaling, cyclic DAC and pipeline DAC, ADC architectures, flash ADC, two step flash ADC, pipeline ADC, integrated ADC, successive approximation ADC and over sampling ADC Case study: Step wise design and analysis of delta sigma modulators and SAR ADC's 3. **CMOS RF IC design principles:** Introduction to CMOS RF IC design principles, standards RF wireless communications multi standard RF transceivers, RF front end architectures, frequency down conversion, image rejections, synthesis of a generic front end architectures, single and two path front end architectures, selection criteria, broad band poly phase filters and topology, RC polyphase and IF image reject filters, I/Q generators design consideration of image rejections, voltage gain RC filters, noise and voltage gain analysis in low IF front end voltage gain, noise factor,	80Hrs	Rs.12000.00

	passive RF blocks, linearity analysis, RF building block specifications, and noise figure IIP3, Case study : RF wireless transceivers at 2.4 GHz 4. **Circuit design for RF Transceivers:** Introduction to RF transceivers, RF specifications, RF device technology, transmitter architectures like direct conversion transmitters, two step transmitters, receivers architectures like heterodyne receivers, homodyne receivers, image reject receivers, digital IF receivers and sub sampling receivers, Case studies: Motorola's FM receivers: Modelling of building blocks 5. **Low noise amplifiers and Mixers:** Introduction to LNA and mixers, general consideration, input matching, biplolar LNA, CMOS LNA design, measurements, single transistor LNA, design steps, simulation and measurements, classical LNA. mixer specification, bipolar mixers, CMOS mixers, active mixers, passive mixers, 1/F noise in mixer transistor, IF amplifiers and switched capacitor behavior models, Case Study : Common source stage with resistive load LNA, Single and balanced mixers 6. **RF power amplifiers and oscillators:** Introduction to RF power amplifiers and oscillators, specification, efficiency, generic amplifier, heating, linearity and ruggedness, bipolar PA design, CMOS PA design, classifications of PA, types of PA's, linearization principles, predistrotion techniques, phase correcting feedback, envelope elimination restoration and Cartesian feedback, ideal and non ideal oscillators, oscillators condition and amplitude stabilization, frequency tuning and linearity, phase noise to carrier ration, power dissipation, spurious emission SNR degradation of FM signals, harmonics, I/Q Matching, LC and RC oscillators Case study : Class B power amplifier, An 830MHZ monolithic LC oscillators, an 10GHz I/Q RC oscillators with active inductors 7. **Frequency Synthesizers :** Introduction to Frequency Synthesizers, integer N PLL architectures, tuning system specifications, system level aspects of PLL building blocks, VCO, frequency dividers, phase- frequency detector/charge pump combination, loop filter, dimensioning the PLL parameter, spectral purity performance, phase noise performance, Case study: Linear Model PLL Analog CMOS filters for very high frequencies : Introduction to analog CMOS filters for very high frequencies, filter synthesis for high frequencies, cascaded, signal flow, state space, gyrator and coupled generated bandpass filters, effect of idealities, transconductance design, VHF transconductance, detail analysis and measurements, tuning, VCO tuning loop, quality factor, supply voltage unit, filter realizations, TV		

	filters, IF filters, and third order elliptical filters, Case Study : Monolithic analog continuous time filters 8. **Analog baseband architectures for low voltage wireless application:** Introduction to baseband architectures for low voltage wireless application , low voltage analog based band techniques, system design of SIP receivers IEEE 802.11A/B/G WLAN, Case study :SIP receivers IEEE 802.11A/B/G WLAN 9. **Practical design techniques for sensor signal conditioning:** Introduction to design techniques for sensor signal conditioners, bridge circuits, strain, force, pressure and flow measurements, high impedance sensors, position and motion sensors, temperature sensor, ADC's for signal conditioning, smart sensors, and hardware techniques 10. **Mixed Signal Testing :** Introduction to mixed signal testing, DSP based and Model based analog and mixed signal test, delay test, analog test bus standard, oscillation-based built-in self-test (OBIST) techniques 11. **Tools Used:** MATLAB, HSPICE, Virtuso, SpectreRF, NanoSim, HSIM, ADS, Qualnet		