32-bit Microcontroller
FR Family FR81S
MB91570 Series DS Major Changes

MB91F575B/F575BS/F575BH/F575BHS
MB91F577B/F577BS/F577BH/F577BHS

This material covers the major changes from DS705-00009-0v01 to DS705-00009-1v0.
### MAJOR CHANGES MADE IN THIS EDITION

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<td>General</td>
<td>The following products are added. MB91F575B/F575BS/F575BH/F575BHS MB91F577B/F577BS/F577BH/F577BHS</td>
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<td>FEATURES</td>
<td>Descriptions are changed.</td>
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<td>4</td>
<td>FEATURES</td>
<td>Names of the following item are corrected. - Up/Down counter ↓ - Up/Down counter: 2 channels - Power on reset / internal low-voltage detection reset ↓ - Power on reset - Low-voltage detection reset ↓ - Low-voltage detection reset (external low-voltage detection) - Low-voltage detection reset (internal low-voltage detection)</td>
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<td>5, 37</td>
<td>FEATURES Peripheral Functions, PRODUCT LINEUP, BLOCK DIAGRAM</td>
<td>Note: In this series, the HS-SPI function is prohibited</td>
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<td>5, 6</td>
<td>PRODUCT LINEUP</td>
<td>Product lineup is changed in accordance with addition of those products.</td>
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- Items added  
  - Sub clock  
  - DMA Transfer → DMA Controller  
  - 16-bit Base Timer → Base Timer (16bit)  
  - Free-run Timer → Free-run Timer (32bit)  
  - Input capture → Input capture (32bit)  
  - Output Compare → Output Compare (32bit)  
  - 16-bit Reload timer → Reload Timer (16bit)  
  - PPG → PPG timer (16bit)  
  - D/A → D/A converter  
  - A/D → A/D converter (8bit/10bit)  
  - Multi-Function → Multi-Function serial communication  
  - Internal low-voltage detection reset → Low-voltage detection reset (Internal low-voltage detection)  
  - On Chip Debug: Built-in OCD → On Chip Debug: Yes
### PIN DESCRIPTION

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<td>PIN DESCRIPTION</td>
<td>Terminologies are unified</td>
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<td>- DEBUG I/F → DEBUG I/F pin (&quot;pin&quot; is added)</td>
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<tr>
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<td>- ## Power Supply → ## Power Supply pin (&quot;pin&quot; is added)</td>
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<tr>
<td></td>
<td></td>
<td>- ## GND → ## GND pin (&quot;pin&quot; is added)</td>
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<tr>
<td></td>
<td></td>
<td>- ## Reference Voltage → ## Reference Voltage pin (&quot;pin&quot; is added)</td>
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<td></td>
<td></td>
<td>- OSC Input pin, OSC Output pin → oscillation Input pin, oscillation Output pin</td>
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<td>20</td>
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<td>The function of MD0 of pin number 114 is changed.</td>
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<td>Mode Pin → Mode Pin 0</td>
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<td>20</td>
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<td>The function of MD1 of pin number 115 is changed.</td>
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<td>Mode Pin → Mode Pin 1</td>
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<td>20</td>
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<td>The I/O circuit type and function of MD2 of pin number 116 are changed.</td>
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<td>A → R2</td>
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<td>Mode Pin → Mode Pin 2</td>
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<td>23</td>
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<td>The function description of AVSS/AVRL of pin number 82 is changed.</td>
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<td>ADC GND / Low Reference Voltage ↓</td>
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<td>ADC, DAC GND pin/ Low Reference Voltage pin</td>
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<tr>
<td>24-26</td>
<td>I/O CIRCUIT TYPE</td>
<td>As to the I/O circuit types, H, I, I2, I3, J, K, L, M, and N, the circuit diagrams are corrected. (The hysteresis symbol on TTL is deleted.)</td>
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<tr>
<td>27</td>
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<td>As to the I/O circuit type B, the circuit diagram is corrected. (The hysteresis symbol on TTL is deleted.)</td>
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<td>27</td>
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<td>The I/O circuit type, R2, is added.</td>
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<td>Remarks for X and Y in the I/O CIRCUIT TYPE are the same as those of other series of the devices.</td>
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<td>Main clock → Main oscillation I/O</td>
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<td>Sub clock → Sub oscillation I/O</td>
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| 37   | BLOCK DIAGRAM | Name of the on-chip Flash Memory is corrected.  
Work Flash → WorkFlash (No space between letter k and F)  
Names of the I/O pins of CAN are corrected.  
CANRX0-2, CANTX0-2 → RX0-2, TX0-2  
Names of the I/O pins of A/D converter are corrected.  
ADTG, AN0-40  
↓  
ADTG, AN0-39  
The following is added to I/O pins of A/D converter.  
ADC enabled (ADER)  
Description of the Low Voltage Detection is corrected.  
Low Voltage Detection  
↓  
Low Voltage Detection (External Power Supply)  
Low Voltage Detection (Internal Power Supply) |
| 38, 39 | MEMORY MAP | The memory map is changed in accordance with addition of those products. |
| 41   | I/O MAP | The data access attribute of address 000044H DICR is corrected.  
B,H,W → B |
| 49   |         | The address 000318H IPVAR is deleted. |
| 55, 76 |         | The address 00031EH IPVSR is deleted. |
| 81   | ELECTRICAL CHARACTERISTICS 1. Absolute Maximum Ratings | Assignment of the corresponding pins described in note *8 are corrected.  
P050 to P056 → P050 to P053 |
| 83   | 3.DC characteristics | Description of conditions for V_{Hi}, V_{Ish} are corrected  
CMOS schmitt → CMOS hysteresis  
Description of V_{Hi} (Pin name: X0, X1, X0A, X1A) are deleted. |
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<td>3.DC characteristics</td>
<td>Pin name of VIL₅ to VIL₈ are corrected. P036 → P037</td>
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<td>Minimum value of VIL₉, VIL₁₀, VIL₁₁ are corrected. Vₜₛ → Vₜₛ₋₀.₃</td>
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<td>Maximum value of VIL₁₀ is corrected. 0.5×V₉₅ → 0.3×V₉₅</td>
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<tr>
<td></td>
<td></td>
<td>Maximum value of VIL₁₁ is corrected. 0.5×V₉₅ → 0.₈</td>
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<tr>
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<td></td>
<td>Description of VIL₁₂ (Pin name: X₀, X₁, X₀A, X₁A) are deleted.</td>
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<td>85</td>
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<td>Condition of VOH₁, VOH₂, VOH₃ are corrected. V₉₅ₑ → V₉₅ₑ = 3.₀V</td>
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<td>86</td>
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<td>Condition of VOL₁, VOL₂, VOL₃ are corrected. V₉₅ₑ = 3.₀V → V₉₅ₑ = 3.₀V</td>
</tr>
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<td>89</td>
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<td>Pin name of VOL₄, VOL₅ are corrected. P036 → P037</td>
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<td>90</td>
<td>4. AC characteristics</td>
<td>The minimum value of the Internal operating clock cycle time, F₆₇₇, F₆₆₆₇, F₆₆₇₇ is determined. - → 2 ( MHz )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The maximum value of the Internal operating clock cycle time, t₆₇₇, t₆₆₆₇, t₆₆₇₇ is determined. - → 5₀₀ ( ns )</td>
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<td>91</td>
<td>(1-2) Sub Clock Timing</td>
<td>Comment on a part number of the products is added. (1-2) Sub clock timing ↓ (1-2) Sub clock timing (products without S-suffix)</td>
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<td>92</td>
<td>Guaranteed operation range</td>
<td>The following note is added: Note: The CPU will be reset at the power supply voltage 4V ± 0.₃V or less.</td>
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<td>92</td>
<td>Example of an oscillation circuit</td>
<td>Capacitance of the C₁ and C₂ in the circuit diagram is corrected. C₁=27pF → 10pF C₂=27pF → 10pF</td>
</tr>
<tr>
<td></td>
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<td>The following note is added: Note: As to the product with its clock supervisor’s initial value is &quot;ON&quot;, when the oscillator is unable to start within 20ms from the stop state the clock supervisor will detect the oscillation stop. As a result, the CPU moves to the fail safe operation. Design your print circuit board so that the oscillator can start oscillation within 20ms.</td>
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<td>95</td>
<td>ELECTRICAL CHARACTERISTICS 4. AC characteristics (3) Power-on Conditions</td>
<td>The table (3) Power-on Conditions is corrected. The descriptions of the following parameters are deleted: Power supply on rise time, Power supply start voltage, and Power supply peak voltage. Descriptions of the following parameters are added: Level detection voltage, Level detection hysteresis width, Level detection time, and Slope detection undetected standard.</td>
</tr>
<tr>
<td>95</td>
<td></td>
<td>The item number of the notes under the table of (3) Power-on Conditions is corrected. *: This time is to start the slope detection↓ *3: This time is to start the slope detection↓ The following are added under the table (3) Power-on Conditions. *1: If the fluctuation of the power supply is faster than the low voltage detection time, there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range. *2: When setting the power supply fluctuation to this standard or less, it is possible to suppress the slope detection. This is the standard when the power supply fluctuation is stable.</td>
</tr>
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<td>95</td>
<td></td>
<td>The diagram under the table (3) Power-on Conditions is deleted.</td>
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<td>96</td>
<td>ELECTRICAL CHARACTERISTICS 4. AC characteristics (4) Multi-function Serial (4-1) UART timing</td>
<td>The following is added to the Bit setting in (4-1) UART timing: SCR:SPI=0 Table in (4-1) UART timing is changed. Parameter: [Valid SIN→SCK↑] → [Valid SIN→SCK↑setup time] (IVSHI, IVSHE) Remarks: Internal shift clock mode output pin: C&lt;sub&gt;L&lt;/sub&gt;=50pF Internal shift clock mode: C&lt;sub&gt;L&lt;/sub&gt;=50pF (When drive capability is 2mA or more.) C&lt;sub&gt;L&lt;/sub&gt;=20pF (When drive capability is 1mA) External shift clock mode output pin: C&lt;sub&gt;L&lt;/sub&gt;=50pF External shift clock mode: C&lt;sub&gt;L&lt;/sub&gt;=50pF (When drive capability is 2mA or more.) C&lt;sub&gt;L&lt;/sub&gt;=20pF (When drive capability is 1mA)</td>
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</table>
| 98   | ELECTRICAL CHARASTERISTICS 4. AC characteristics (4-1) UART timing | The following is added to the Bit setting in (4-1) UART timing: SCR:SPI=0 Table in (4-1) UART timing is changed. Parameter: [Valid SIN→SCK ↓] is corrected to [Valid SIN→SCK ↓ setup time] (tIVSLI , tIVSLE) Remarks: Internal shift clock mode output pin: 
\[ C_{IL}=50pF \] 
Internal shift clock mode: 
\[ C_{IL}=50pF \text{ (When drive capability is 2mA or more.)} \]
\[ C_{IL}=20pF \text{ (When drive capability is 1mA)} \] 
External shift clock mode output pin: 
\[ C_{IL}=50pF \] 
External shift clock mode: 
\[ C_{IL}=50pF \text{ (When drive capability is 2mA or more.)} \]
\[ C_{IL}=20pF \text{ (When drive capability is 1mA)} \] |
<p>| 99   | (4) Multi-function Serial (4-1) UART timing | The diagram, External shift clock mode, in (4-1) UART timing is corrected. Serial clock “L” pulse width tSLSH which a double-headed arrow shows is corrected from the interval between ( V_{IL}-V_{IH} ) to ( V_{IL}-V_{IL} ). |
| 100, 101 | (4) Multi-function Serial (4-1) UART timing | In (4-1) UART timing, the following bit setting is added: Bit setting: SMR: MD2=0, SMR: MD1=1, SMR: MD0=0, SMR: SCINV=0, SCR:SPI=1 |
| 102, 103 | (4) Multi-function Serial (4-1) UART timing | In (4-1) UART timing, the following bit setting is added: Bit setting: SMR: MD2=0, SMR: MD1=1, SMR: MD0=0, SMR: SCINV=1, SCR:SPI=1 |
| 104 | (4) Multi-function Serial (4-2) External clock (EXT=1) | (4-2) External clock (EXT = 1): asynchronous only is added. |</p>
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| 105  | (4-3) I²C timing | In (4-3) I²C timing, the following is corrected:  
The title number is corrected as shown below.  
(4-2) I²C timing → (4-3) I²C timing  
One of the symbols is corrected as shown below.  
t_{BUS} → t_{BUF}  
Condition of Noise filter is corrected to [-].  
Conditions:  
C_{L}=50pF  
→ C_{L}=50pF (When drive capability is 2mA or more.)  
→ C_{L}=20pF (When drive capability is 1mA.)  
The first note “*1” under the table is corrected as shown below:  
*1: R and C represent the pull-up resistance and load capacitance of the SCL and SDA output lines.  
↓  
*1: R and C represent the pull-up resistance and load capacitance of the SCL and SDA output lines. |
| 107  | (5)LIN-UART timing | In the bit setting, ESCR: SCES=0 & ECCR: SCDE=0, the following are corrected.  
Parameter:  
[Valid SIN→SCK↑] → [Valid SIN→SCK↑setup time]  
(t_{IVSHI}, t_{IVSHE})  
Parameters and symbols are corrected as shown below.  
Serial clock "H" pulse width, t_{SHSL}  
↓  
Serial clock "L" pulse width, t_{SLSL}  
↓  
Serial clock "L" pulse width, t_{SLSH}  
↓  
Serial clock "H" pulse width, t_{SHSL}  
Remarks:  
Internal shift clock mode output pin:  
C_{L}=80pF+1·TTL  
↓  
Internal shift clock mode:  
C_{L}=80pF+1·TTL  
External shift clock mode output pin:  
C_{L}=80pF+1·TTL  
↓  
External shift clock mode:  
C_{L}=80pF+1·TTL |
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| 109  | (5)LIN-UART timing | In the bit setting, ESCR: SCES=1 & ECCR: SCDE=0, the following are corrected.  
Parameter:  
[Valid SIN→SCK ↓] → [Valid SIN→SCK ↓ setup time]  
(t_{IVSLI}, t_{IVSLE})  
Remarks:  
Internal shift clock mode output pin:  
C_L=80pF+1·TTL  
Internal shift clock mode:  
C_L=80pF+1·TTL  
External shift clock mode output pin:  
C_L=80pF+1·TTL  
External shift clock mode:  
C_L=80pF+1·TTL |
| 110  | (5)LIN-UART timing | The diagram, External shift clock mode, in (5)LIN-UART timing is corrected.  
Serial clock “L” pulse width t_{SLSH} which a double-headed arrow shows is corrected from the interval between V_{IL}-V_{IH} to V_{IL}-V_{IL} |
| 111  | (5)LIN-UART timing | In the bit setting, ESCR: SCES=0 & ECCR: SCDE=1, the following are corrected.  
Parameter:  
[Valid SIN→SCK ↓] → [Valid SIN→SCK ↓ setup time]  
(t_{IVSLI})  
Remarks:  
Internal shift clock mode output pin:  
C_L=80pF+1·TTL  
Internal shift clock mode:  
C_L=80pF+1·TTL  
The figure title is added to the timing chart.  
·Internal shift clock mode |
In the bit setting, ESCR: SCES=1 & ECCR: SCDE=1, the following are corrected.

Parameter:
\[
[\text{Valid } \text{SIN} \rightarrow \text{SCK} \uparrow] \rightarrow [\text{Valid } \text{SIN} \rightarrow \text{SCK} \uparrow \text{setup time}] \\
(t_{IVSHI})
\]

Remarks:
Internal shift clock mode output pin:
\[C_L=80pF+1\cdot\text{TTL} \quad \downarrow\]
Internal shift clock mode:
\[C_L=80pF+1\cdot\text{TTL}\]

The figure title is added to the timing chart.

Internal shift clock mode

The title name is corrected as shown below.

(9) Low voltage detection

The specification table of (9) Low voltage detection (External low-voltage detection) is corrected.

The figure under the specification table of (9) Low voltage detection (External low-voltage detection) is deleted.

The parameter "Power-supply voltage fluctuation rate" and its note (*2) are added.

The title name is corrected.

(10) Internal low voltage detection

The specification table of (10) Low voltage detection (Internal low-voltage detection) is corrected.

The figure under the specification table of (9) Low voltage detection (Internal low-voltage detection) is deleted.

The specification of the analog port input current \(I_{AIN}\) is determined.

Min. \(-5\) (\(\mu\)A)  
Max. \(+5\) (\(\mu\)A)

The note under the table is corrected.

Note: Be sure to use the clock with a frequency between 8MHz and 17MHz for the ADC compare clock in order to ensure its accuracy.
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**Section**: ELECTRICAL CHARACTERISTICS 5. A/D converter

In the diagram of an analog circuit model, part numbers and the maximum value of C are corrected.

- MB91F575/MB91F577 → MB91570 series
- $C = 15\text{pF}(\text{MAX})$
- → $C = 16.5\text{pF}(\text{MAX})$*
- *: except DA shared pin

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**Section**: 6. D/A converter

The remark about the reference voltage supply current, $I_{DVR}$, is corrected.

- Per 1ch → Per 1ch*

The following note is added below the specification table.

*: Reference voltage supply current ($V_{CC} = AV_{CC} = 5.0 \text{ V}$) is specified.

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**Section**: 7. Flash memory

The values of the following items in the specification table are corrected.

- Sector erase time
- Erase cycle/Data retain time

Remarks and notes are corrected.

The title "(1) Electrical characteristics" are put on the specification table.

Notes for power-off during Flash writing are added as (2).

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**Section**: Ordering part number

Ordering part numbers are changed in accordance with the additions to our product lineup.