# A New Approach to the Modulation and DC-Link Balancing Strategy of Modular Multilevel AC/AC Converters 

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#### Abstract

Modular multilevel AC/AC converters have been examined for high powers and voltages applications such as traction converters and interphase power controllers. It can also operate directly on a transmission line for voltage regulation and reactive power control. This paper presents a modulation technique aiming at an independent control over the AC voltages as well as reactive power of the AC/AC converter, having the capability of controlling the transferred active power from the input source to the load. Moreover, the DC-links of a modular AC/AC converter needs to be regulated for proper operation under various load conditions. The proposed modulation technique embraces a DC voltage balancing strategy based on the engaged switching instants. PSCAD simulation results are presented to validate the proposed modulation technique for both open-loop and closed-loop control.


Keywords-Multilevel AC/AC Converters, modulation, DC-link balancing, switching states

## I. INTRODUCTION

Usage of nonlinear loads in power systems are growing sharply, which is being coincided with the use of wind and solar energy in line with distributed generations that require switching power converters. Consequently, this situation needs more attention on control of reactive power and power losses in addition to the filtering issues. Modular multilevel AC/AC converters (MMLC) have already been applied to traction converters can potentially be contributed to power systems.

In practice, transformerless connection of a converter to the grid system needs increasing the number of the DC voltage levels to achieve higher AC voltages [1-2-3-4-5]. Benefits and reasons to use the MMLC are described in [1] and [2]. Fig. 1(a) shows the configuration of a single-phase MMLC, which consists of full-bridge modules (depicted in Fig. 1(b)) in four arms. For a simple case each arm of the AC/AC converter includes one full-bridge module, each producing three voltage levels $V_{d c}, 0$, and $-V_{d c}$. Table 1 describes switching states of a module along with corresponding sign of AC current and DC voltage variation.

In [3] the MMLC is employed to control the power flow of a power system, while the voltages of the modules are treated
as synchronous phasors. Each module is modulated in a way that having a fundamental voltage perpendicular to its current likes either a capacitor or an inductor. Moreover, the two voltage located in each arm are also at a 90 degree angle. This method introduces control neither on input reactive power nor on the DC-link of the modules.

Another proposal in [6], based on phasor relationships, suggests that always the module voltages obey the rules $\mathrm{Val}=$ $V_{a t}$ and $V_{a 2}=V_{a 3}$. A problem with this method is that the module currents would tend to infinity when input and output AC voltages are in phase. Here we concentrate on a modulation technique, which works on switching instants to achieve desirable input/output references for the MMLC. This proposal considers switching instants that not only satisfy circuit relationships but also improve the DC-link voltage balancing to an acceptable level. The whole modulation and balancing technique have been simulated with PSCAD. Various simulation results are illustrated to confirm the validity of the proposed modulation objectives.

TABLE I. SWITCHING STATES AND SIGNS OF DC VOLTAGE VARIATIONS and AC Current for a full-bridge module illustrated in Fig. 1(b)

| $\mathbf{V}_{\mathbf{a}}$ | $\mathbf{S}_{\mathbf{1}}$ | $\mathbf{S}_{\mathbf{2}}$ | $\mathbf{S}_{\mathbf{3}}$ | $\mathbf{S}_{\mathbf{4}}$ | $\mathbf{i}_{\mathbf{a}}$ | $\mathbf{d} \mathbf{V}_{\mathbf{d c}} / \mathbf{d t}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathbf{V}_{\mathrm{dc}}$ | On | Off | Off | On | + | + |
| - | $\mathbf{V}_{\mathrm{dc}}$ | Off | On | On | Off | + |
| 0 | On | Off | On | Off | + |  |
| - | + |  |  |  |  |  |
| - |  |  |  |  |  |  |
| 0 | Off | On | Off | On | + <br> - <br> - | $\times$ <br> $\times$ |

## II. PROPOSED MODULATING PRINCIPLES

Let the AC/AC converter of Fig. 1(a) be composed of four full-bridge modules. Then, there exit 81 possible switching states. Nevertheless, the KVL circuit obligation in the form of

$$
\begin{equation*}
v_{a 1}(t)+v_{a 2}(t)=v_{a 3}(t)+v_{a 4}(t) \tag{1}
\end{equation*}
$$

has to be satisfied to avoid sudden charge or discharge of the full-bridge modules. Additionally, the inductance $L_{i}$ limits the circular currents when modules transit from one switching


Figure 1. (a) Left picture: General diagram of a modular multilevel AC/AC converter suitable for power system applications; (b) Right picture: A full-bridge module as a three-level converter
state to another. To balance voltage drops on branches, these four small inductances (typically about $1 \mu \mathrm{H}$ ) are chosen to be equal.

In this paper, the proposal is restricted to a three level input/output case. Thus, the feasible numbers of switching instants are reduced. Table 2 gives these selected switching states in which $V_{\text {in }}^{\prime}$ and $V_{\text {out }}^{\prime}$ are the internal input and output voltages respectively (see Fig. 1(b)). There are twelve states in Table 2 that can be divided into three groups of four, having the following common characteristics:

$$
\left\{\begin{array}{lll}
V_{\text {in }}^{\prime}=0 & \& & V_{\text {out }}^{\prime} \neq 0  \tag{2}\\
V_{\text {in }}^{\prime} \neq 0 & \& & \text { states } 1-4 \\
V_{\text {out }}^{\prime}=0 & \text { states } 5-8 \\
V_{\text {in }}^{\prime} \neq 0 & \& & V_{\text {out }}^{\prime} \neq 0
\end{array} \quad \text { states } 9-12\right.
$$

TABLE II. RESULTANT VOLTAGES OF THE MODULES ALONG WITH INTERNAL INPUT/OUTPUT VOLTAGES FOR THE FIFTEEN SELECTED STATES

| No. | $\mathbf{V}_{\text {in }}^{\prime}$ | $\mathbf{V}_{\text {out }}^{\prime}$ | $\mathbf{V}_{\mathrm{al1}}^{\prime}$ | $\mathbf{V}_{\mathrm{a} 21}$ | $\mathbf{V}_{\mathrm{a} 31}$ | $\mathbf{V}_{\mathrm{a} 41}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 0 | $\mathrm{~V}_{\mathrm{dc}}$ | $-\mathrm{V}_{\mathrm{dc}}$ | $\mathrm{V}_{\mathrm{dc}}$ | 0 | 0 |
| 2 | 0 | $\mathrm{~V}_{\mathrm{dc}}$ | 0 | 0 | $\mathrm{~V}_{\mathrm{dc}}$ | $-\mathrm{V}_{\mathrm{dc}}$ |
| 3 | 0 | $-\mathrm{V}_{\mathrm{dc}}$ | 0 | 0 | $-\mathrm{V}_{\mathrm{dc}}$ | $\mathrm{V}_{\mathrm{dc}}$ |
| 4 | 0 | $-\mathrm{V}_{\mathrm{dc}}$ | $\mathrm{V}_{\mathrm{dc}}$ | $-\mathrm{V}_{\mathrm{dc}}$ | 0 | 0 |
| 5 | $\mathrm{~V}_{\mathrm{dc}}$ | 0 | $\mathrm{~V}_{\mathrm{dc}}$ | 0 | $\mathrm{~V}_{\mathrm{dc}}$ | 0 |
| 6 | $\mathrm{~V}_{\mathrm{dc}}$ | 0 | 0 | $\mathrm{~V}_{\mathrm{dc}}$ | 0 | $\mathrm{~V}_{\mathrm{dc}}$ |
| 7 | $-\mathrm{V}_{\mathrm{dc}}$ | 0 | 0 | $-\mathrm{V}_{\mathrm{dc}}$ | 0 | $-\mathrm{V}_{\mathrm{dc}}$ |
| 8 | $-\mathrm{V}_{\mathrm{dc}}$ | 0 | $-\mathrm{V}_{\mathrm{dc}}$ | 0 | $-\mathrm{V}_{\mathrm{dc}}$ | 0 |
| 9 | $\mathrm{~V}_{\mathrm{dc}}$ | $\mathrm{V}_{\mathrm{dc}}$ | 0 | $\mathrm{~V}_{\mathrm{dc}}$ | $\mathrm{V}_{\mathrm{dc}}$ | 0 |
| 10 | $\mathrm{~V}_{\mathrm{dc}}$ | $-\mathrm{V}_{\mathrm{dc}}$ | $\mathrm{V}_{\mathrm{dc}}$ | 0 | 0 | $\mathrm{~V}_{\mathrm{dc}}$ |
| 11 | $-\mathrm{V}_{\mathrm{dc}}$ | $\mathrm{V}_{\mathrm{dc}}$ | $-\mathrm{V}_{\mathrm{dc}}$ | 0 | 0 | $-\mathrm{V}_{\mathrm{dc}}$ |
| 12 | $-\mathrm{V}_{\mathrm{dc}}$ | $-\mathrm{V}_{\mathrm{dc}}$ | 0 | $-\mathrm{V}_{\mathrm{dc}}$ | $-\mathrm{V}_{\mathrm{dc}}$ | 0 |
| 13 | 0 | 0 | 0 | 0 | 0 | 0 |
| 14 | 0 | 0 | $\mathrm{~V}_{\mathrm{dc}}$ | $-\mathrm{V}_{\mathrm{dc}}$ | $\mathrm{V}_{\mathrm{dc}}$ | $-\mathrm{V}_{\mathrm{dc}}$ |
| 15 | 0 | 0 | $-\mathrm{V}_{\mathrm{dc}}$ | $\mathrm{V}_{\mathrm{dc}}$ | $-\mathrm{V}_{\mathrm{dc}}$ | $\mathrm{V}_{\mathrm{dc}}$ |

Two states 14-15 describe situations ( $V_{\text {in }}^{\prime}=0 \& V_{\text {out }}^{\prime}=0$ ) in which one module charges while the other one discharges in the same arm. The state 13 also makes similar result to those of 14-15, but modules neither charge nor discharge. These three states can be employed in the modulation technique when appropriate. Different conventional modulations can be used to engage the detailed switching states such as SVM. For example, the naturally sampled PWM is considered to show the feasibility of achieving the reference waveforms. Meanwhile, we apply a compensation offset ( $O C$ ) between the input/output carriers to get the regulated DC voltages.

## A. Evaluation of Reference Voltages

When the compensation principle is based on reactive and active powers at mains frequency, only the magnitudes and phases of fundamental internal voltages are controlled. While the input reactive power $\left(Q_{i n}\right)$ is controlled to produce the output demand, the active power drawn from the input ( $P_{i n}$ ) has to be equal to the load active power $\left(P_{o u t}\right)$ plus the converter losses ( $P_{\text {loss }}$ ).

The average voltage of capacitors is used to decide on the needed active power $P_{i n}$. Fig. 2 shows the control loop to obtain the internal reference voltage for the input $\left(V_{i n}^{\prime}{ }^{*}\right)$. Here the reference angle is regulated based on the DC capacitors voltage drops using a PI controller. At the same time, the reference magnitude is generated according to the needed reactive power at the output.

## B. Modulation establishment

Having established the reference fundamental voltages $\left(V_{i n}^{\prime}{ }^{*}\right.$ and $V_{\text {out }}^{\prime}{ }^{*}$ ), two ramp carriers are used to modulate the required internal voltages by $\mathrm{AC} / \mathrm{AC}$ converter. The principal reason to use two carriers is the employed DC balancing strategy described in the next section. Also, here we use only
three levels of Vdc, 0 , and $-V_{d c}$ for modulating both the internal input and output voltages. It can be seen from Table 2 that there exist two switching states 1 and 2 in which $V_{i n}^{\prime}=0$, while the output voltage $V_{\text {out }}^{\prime}$ is equal to $V_{d c}$. Hence, we have expanded the Table 2 into two Tables III and IV. Each of these Tables provides unique combinations of ( $V^{\prime}$ in and $V_{\text {out }}^{\prime}$ ), which are repeated in the other Table with different modulation states. Selecting one of these Tables is dependant on the DC voltage balancing. Once the suitable Table is selected, every switching instant of the modules is determined by the PWM modulating procedure based on the established internal references.


Figure 2. Derivation of the fundamental voltage of the internal input.

TABLE III. Possible three Level switching combinations generating ( $V$ 'IN AND $V_{\text {out }}^{\prime}$ ).

| No. | $\mathbf{V}^{\mathbf{i n}}$ | $\mathbf{V}_{\text {out }}^{\prime}$ | $\mathbf{V}_{\mathrm{a} 11}^{\prime}$ | $\mathbf{V}_{\mathrm{a} 21}$ | $\mathbf{V}_{\mathbf{a 3 1 1}}$ | $\mathbf{V}_{\text {a41 }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 0 | $\mathrm{~V}_{\mathrm{dc}}$ | $-\mathrm{V}_{\mathrm{dc}}$ | $\mathrm{V}_{\mathrm{dc}}$ | 0 | 0 |
| 4 | 0 | $-\mathrm{V}_{\mathrm{dc}}$ | $\mathrm{V}_{\mathrm{dc}}$ | $-\mathrm{V}_{\mathrm{dc}}$ | 0 | 0 |
| 5 | $\mathrm{~V}_{\mathrm{dc}}$ | 0 | $\mathrm{~V}_{\mathrm{dc}}$ | 0 | $\mathrm{~V}_{\mathrm{dc}}$ | 0 |
| 8 | $-\mathrm{V}_{\mathrm{dc}}$ | 0 | $-\mathrm{V}_{\mathrm{dc}}$ | 0 | $-\mathrm{V}_{\mathrm{d}}$ | 0 |
| 9 | $\mathrm{~V}_{\mathrm{dc}}$ | $\mathrm{V}_{\mathrm{dc}}$ | 0 | $\mathrm{~V}_{\mathrm{dc}}$ | $\mathrm{V}_{\mathrm{dc}}$ | 0 |
| 10 | $\mathrm{~V}_{\mathrm{dc}}$ | $-\mathrm{V}_{\mathrm{dc}}$ | $\mathrm{V}_{\mathrm{dc}}$ | 0 | 0 | $\mathrm{~V}_{\mathrm{dc}}$ |
| 11 | $-\mathrm{V}_{\mathrm{dc}}$ | $\mathrm{V}_{\mathrm{dc}}$ | $-\mathrm{V}_{\mathrm{dc}}$ | 0 | 0 | $-\mathrm{V}_{\mathrm{dc}}$ |
| 12 | $-\mathrm{V}_{\mathrm{dc}}$ | $-\mathrm{V}_{\mathrm{dc}}$ | 0 | $-\mathrm{V}_{\mathrm{dc}}$ | $-\mathrm{V}_{\mathrm{dc}}$ | 0 |
| 13 | 0 | 0 | 0 | 0 | 0 | 0 |

TABLE IV. A difFERENT SET OF SWITCHING STATES GENERATING similar ( $V^{\prime}$ IN and $V^{\prime}{ }_{\text {out }}$ ) as Table III.

| No. | V'in | V'out | Va11 | Va21 | Va31 | Va41 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 2 | 0 | $V_{d c}$ | 0 | 0 | $V_{d c}$ | $-V_{d c}$ |
| 3 | 0 | $-V_{d c}$ | 0 | 0 | $-V_{d c}$ | $V_{d c}$ |
| 6 | $V_{d c}$ | 0 | 0 | $V_{d c}$ | 0 | $V_{d c}$ |
| 7 | $-V_{d c}$ | 0 | 0 | $-V_{d c}$ | 0 | $-V_{d c}$ |
| 9 | $V_{d c}$ | $V_{d c}$ | 0 | $V_{d c}$ | $V_{d c}$ | 0 |
| 10 | $V_{d c}$ | $-V_{d c}$ | $V_{d c}$ | 0 | 0 | $V_{d c}$ |
| 11 | $-V_{d c}$ | $V_{d c}$ | $-V_{d c}$ | 0 | 0 | $-V_{d c}$ |
| 12 | $-V_{d c}$ | $-V_{d c}$ | 0 | $-V_{d c}$ | $-V_{d c}$ | 0 |
| 13 | 0 | 0 | 0 | 0 | 0 | 0 |

## III. DC-Link Balancing

The DC voltages of the modules need to be balanced. In brief, this is achieved by paralleling modules to exchange electric charges from one module to the other. In practice, this
can be managed by the proper selection of switching instants among the states $1-8$ from Table II as gathered in Table III. The selection procedure depends on a comparison between the DC-link voltage differences, which eventually forces the DC voltages closer together.

In fact, when Table III is chosen for switching modulation, then the full-bridge numbered as one is paralleled with the fullbridge numbered as either two or three. Also, selecting a switching state from Table IV will result in paralleling the fourth full-bridge with either the second or the third full-bridge. Paralleling two modules take place through the inductance $L_{i}$, forcing the two involved DC capacitors exchange electric charges in a short time.

Further, it is necessary to explain how the Tables III and IV are selected for the modulation purposes. Here it is detailed the selection procedure by the following subsections, which mainly differs in the first eight switching states listed by Table II:

## A. Internal Input voltage

When $V_{i n}^{\prime}=0$, the comparison between the voltages of the modules involved parallel arms decides which Table should be used:

- If $\left|V_{a 31}-V_{a 41}\right| \leq\left|V_{a 11}-V_{a 21}\right|$, then Table III is chosen for switching modulation.
- If $\left|V_{a 31}-V_{a 41}\right| \geq\left|V_{a 11}-V_{a 21}\right|$, then Table IV is selected for switching modulation.


## B. Internal Output Voltage

When $V_{\text {out }}^{\prime}=0$, the comparison will take place between the voltages of the upper modules and the lower ones to select the modulating Table:

- If $\left|V_{a 11}-V_{a 31}\right| \geq\left|V_{a 21}-V_{a 41}\right|$, then Table III is used for modulation purposes.
- If $\left|V_{a 11}-V_{a 31}\right| \leq\left|V_{a 21}-V_{a 41}\right|$, then Table IV is used for switching modulation.
Note that when both the internal voltages are nonzero, then Tables III and IV are the same. Also, the bigger the switching frequency, the shorter is the paralleling time of the modules. Choosing suitable values for the inductance $L_{i}$ and capacitance $C$ would help to lessen the high instantaneous variations at the output of the AC/AC converter.

The presented modulation technique involves two ramp carriers in modulating the internal voltages. The reason for having two carriers is that sometimes the two internal references are in phase with the same frequency and shape. In such cases, there would be no choice for selecting a switching state from the first eight states listed in Table II. Thus, the DC voltage balancing strategy cannot be applied, entering the whole converter in an unstable operating condition.

To remedy this issue, two carriers are applied to the PWM modulation, suggesting a phase difference between them as the
compensation offset ( $O C$ ). This offset introduces vital benefits for the $\mathrm{AC} / \mathrm{AC}$ converter. First, the $O C$ makes the switching modulation technique to engage all the listed switching states in Table II. Second, this parameter improves the overall control over the paralleling the full-bridge modules.

Note that the compensation offset $O C$ modulates the paralleling duration of the modules. DC voltage variation of a module is proportional to the squared of this time, and should carefully selected to avoid any possible oscillations due to the available inductances and capacitance in the AC/AC topology. The whole DC balancing procedure is managed by two PI controllers, one for the DC reference voltage and another for the OC modulation.

## IV. ASSESSING THE PROPOSED METHOD

An AC/AC converter (MMLC) was simulated with PSCAD that is composed of four modules based on Fig. 2. Also, two PI controllers in closed-loop form provide the improvement in the DC-link balancing conditions. The parameters involve in the process are: $L_{\text {in }}=3 \mathrm{mH}, L_{i}=1 \mu \mathrm{H}, C=3 \mathrm{mF}$, Load $\left\{L_{\text {out }}=\right.$ $1 \mathrm{mH}, R=10 \Omega\}, V_{\text {in }}=100 \mathrm{~V} \angle 0^{\circ}, V_{\text {in }}^{\prime}{ }^{*}=100 \mathrm{~V} \angle-13^{\circ}, V_{\text {out }}^{\prime}{ }^{*}$ $=100 \mathrm{~V} \angle 0^{\circ}, f_{s}=2000 \mathrm{~Hz}, V_{d c}$-reference $=141.4 \mathrm{~V}$.

Here we present selected simulation results to demonstrate the viability of the proposed modulation technique. Figures 3-4 show the DC voltages of the four full-bridges in an open-loop simulation where OC was adjusted at $3 \%$ and $25 \%$ respectively, introducing the effect of $O C$ on improving the DC-link voltage regulation from $10 \%$ to $5 \%$. When $O C=3 \%$, the worst case voltage unbalance limits to 12 V , while for $O C=$ $25 \%$ this is smaller than 6 V .

Fig. 5 depicts the resulting modulated internal input/output references together with corresponding carriers for the case of $C O=25 \%$. It can also be seen the phase shift between the two carriers that improves the DC voltage balancing of the converter.

Moreover, closed-loop control gets involved, where selected results are introduced. Assume the DC reference value is set to 141.4 V , which is equal to the peak value of the input AC source. Here the control loop operates on $\alpha=\angle\left(V_{i n}, V_{i n}^{\prime}\right)$, starting from zero initial conditions for all capacitor voltages as well as all inductor currents.

Fig. 6 shows the convergence of the control angle $\alpha$, the average active power delivered by the input source and the oscillating power of second harmonic. Also, Fig. 7 illustrates average active power along with second harmonic oscillating power of the load. Further, the convergence of the four DC-link voltages based on the closed-loop control can be observed in Fig. 8, showing a balanced situation with voltage regulation about 3\%.

Closed-loop simulation results also show that the PI controller (shown in Fig. 2) retains different parameters of the $\mathrm{AC} / \mathrm{AC}$ converter within the specified expected settings. In practice, the initial values for inductance currents as well as DC



Figure 4. DC voltages for the case $O C=25 \%$


Figure 5. Internal references along with corresponding two carriers for the case $\mathrm{OC}=25 \%$.


Figure 6. Closed-loop control over DC-link voltages (reference is 141.4 V ) with $\mathrm{OC}=25 \%$


Figure 7. Load active and oscillating power under closed-loop control.
capacitance voltages are not necessarily starting from zero; hence, the converging time is much shorter than that of the first time starting up of the converter as illustrated by Figs. 6-8.


Figure 8. Balancing the DC-link voltages under three volt deviations.

## V. CONCLUSION

This paper proposes a modulation scheme for a modular multilevel AC/AC converter. The method selects a number of switching instants among all possible states to satisfy topological constraints along with restricting the control strategy to the provision of three-level outcomes. Further, to modulate input/output references, some other switching states are selected that can regulate the DC-link voltages of the fullbridge modules. This is demonstrated by introducing a DC-link voltage balancing strategy based on using the modulating procedure as a way of paralleling the DC capacitors to exchange electric charges. Moreover, a closed-loop PI controller is used to regulate the phase shift between the input source and the converter AC input to achieve active power balance between the two AC sides. Also, another controller adjusts the compensating offset of the carriers to avoid a special practical case where both internal voltages are always nonzero. The whole power circuit as well as the modulation and control loops was simulated with PSCAD, demonstrating the effectiveness and full control over input/output AC voltages.

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