Analog VLSI Circuit Design:
Linear Voltage Regulator

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Abstract

The project outlined in this report is the design, layout, and routing of a linear voltage regulator using Cadence VLSI (very-large-scale integration) software. The design specifications for this regulator are as follows: input voltage range of 5V $\pm$ 1V, load current capabilities of 150mA, and output voltage range of 1.15V to 3.3V. Furthermore, the design of this circuit was broken into three main sub-circuits: an error amplifier, bandgap reference circuitry, and biasing circuitry for the bandgap. Together, these sub-circuits integrated to make the final design.

Research for different topologies for a voltage regulator was done and the Brokaw bandgap reference circuit by Paul Brokaw was used for the reference voltage.

The layout and routing of these sub-circuits was performed by breaking these sub-circuits into even smaller sub-circuits and routing these individually. In the end, the group was able to layout and route all of the sub-circuits. However, several DRC and LVS errors were encountered throughout the layout process. Main sources of errors were due to the bipolar junction transistors and resistors used in this design.

To the best knowledge of the group, layout and routing of the bipolar junction transistors used in this design have never been attempted at California Polytechnic State University San Luis Obispo. Therefore, it was expected that the group ran into several problems with these devices and it is outlined in the report how some of these problems were resolved.

From the final design, it was found that the voltage regulator that was created in Cadence has an output voltage of about 3.4V; 100mV more than the intended 3.3V, yielding a discrepancy of 3% from the design specifications. In regards to temperature, the design deviates about 85mV across the industrial temperature range of -40□ to 100□. Another metric that was used to test the final design is the voltage deviation when the load current is swept from 0-150mA,which was found to be 170mV.

It was found that the subcircuits created for this project performed fairly close to the intended purpose and therefore the design of the voltage regulator is seen as a success. Thus, the next step for this project will be to fix the DRC and LVS errors associated with BJTs and resistors. After that, extraction of the circuit should be done to determine the parasitic capacitance and inductance associated with this circuit. And finally, the GDSII file should be made to be sent to the chip manufacturer to tape-out the chip.

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Introduction

This paper outlines the design, routing, and layout of a linear voltage regulator using Cadence VLSI software and IBM CMHV7SF technology. This project was chosen so that the group could get a greater understanding of the integrated circuit (IC) design and fabrication process. The group was interested in designing an IC from start to finish and wanted to pursue this challenge. Cadence software was chosen to be used for this project due to its availability at California Polytechnic State University San Luis Obispo and because the group had previous experience designing in Cadence in a course titled "EE431: Computer-Aided Design of VLSI Devices." Furthermore, Cadence is one of the industry's leading EDA software.

A voltage regulator is a device used to maintain a lower constant output voltage than the voltage that is input to the device. Regulators are especially of interest in systems where only one power source is used to input power and multiple different power rails are required for the system to function. For systems such as this, different power rails are created from the main input voltage by dropping the input voltage using regulators. This allows devices that require a lower operating voltage than the power supply to operate correctly in the system as a whole.

There are two very common types of voltage regulators: switching voltage regulators and linear voltage regulators. The differences between switching and linear regulators can be seen below in **Table 1**.

Table 1: Linear vs. Switching Regulator Comparison

Regulator Type	Advantage	Disadvantage
Linear	Low complexity Small to medium size Low noise Low cost	Low to medium efficiency Only steps down (buck) voltage
Switching	High efficiency Can step up (boost) or step down (buck) voltage	High component count Medium to high output switching noise Medium to high complexity Medium to high cost Larger size than linear

Since modern ICs are very complicated, a linear voltage regulator was decided to be designed. This allowed for a realistic project goal that could be accomplished within the allotted time.

Now, a very basic explanation of how a voltage regulator functions will follow. The regulator utilizes a comparator circuit which, for this project, consists of an error amplifier where the output of the error amplifier is used to drive a control element. The control element in this project is a power MOSFET operating in the linear mode. This creates a variable resistor in series with the load which is used to adjust the output voltage to the desired voltage. A typical block diagram for a linear voltage regulator showcasing the above explanation is shown below in **Figure 1**.

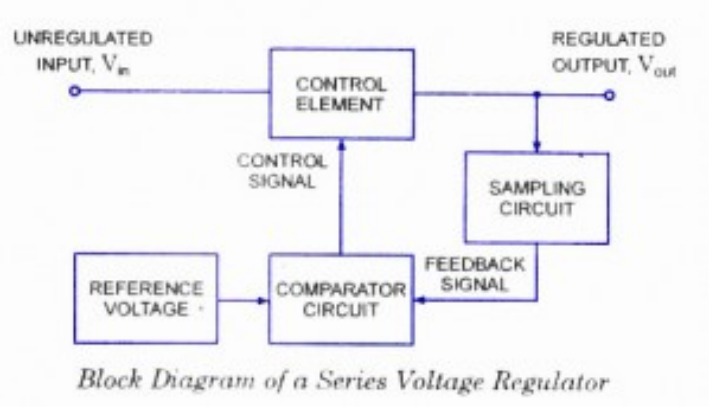


Figure 1: Linear Voltage Regulator Block Diagram
(Image obtained from HQEW.net [1])

The reference voltage in **Figure 1** is used for comparison purposes in the regulator and is the input to the positive terminal of the error amplifier. The error amplifier is needed in the linear regulator because it is used in the feedback loop of the circuit to compare the reference voltage V_{Ref} with the sampled DC output voltage V_{FB} from the voltage divider of R_A and R_B. The output of the error amplifier is then fed into the base of the series power transistor (or gate in this case since the design utilizes a power MOSFET) which allows for tuning of the output voltage to the desired value. The block diagram of a typical linear regulator showcasing the above explanation can be seen below in **Figure 2**.

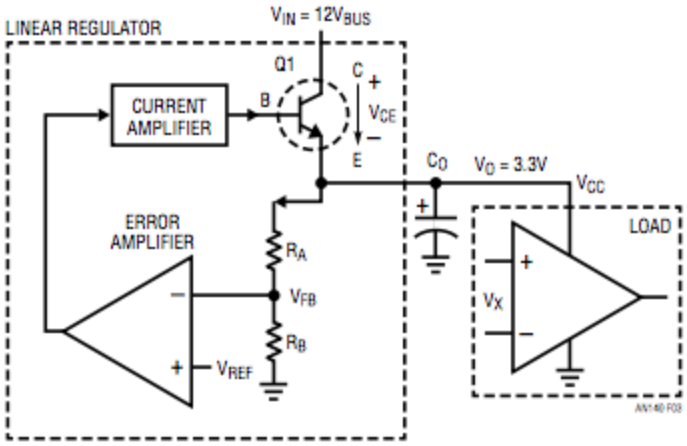


Figure 2: Typical Linear Regulator Schematic
(cds.linear.com [2])

Of note is that voltage regulators typically have two external resistors that are attached to the device which are used to set the output voltage to the desired value. These resistors are labeled R_A and R_B in **Figure 2** and are used in the feedback network which consists of the error amplifier, power MOSFET, and the two resistors. This feedback network allows the error amplifier to adjust the voltage V_{FB} to V_{REF} and thus allows the desired output voltage to be maintained. An example of a block diagram of a voltage regulator and the external resistors can be seen from the Texas Instruments LM317-N datasheet in **Figure 3**.

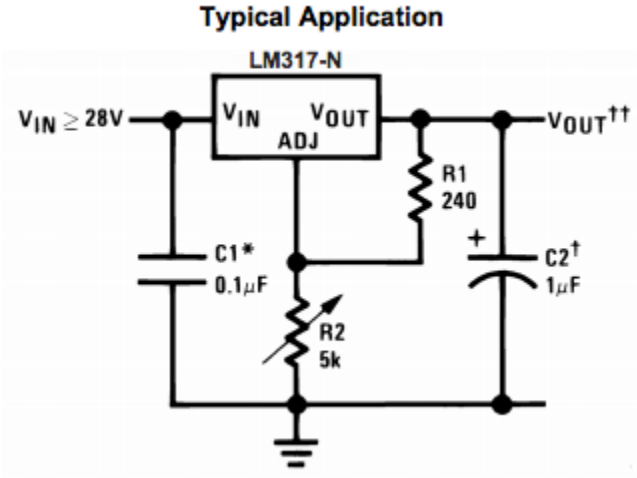


Figure 3: Texas Instrument's LM317-N Block Diagram [7].

As mentioned previously, the two external resistors that are attached to the regulator are used to set the desired output voltage. The equation that is used to set the output voltage for voltage regulators is derived below and **Figure 3** should be referenced when viewing this derivation.

$$V_{OUT} = V_{R1} + V_{R2} = V_{R1} + V_{REF} = I_{R1} * R_1 + V_{REF} \Rightarrow$$
$$I_{R1} = I_{R2} = \frac{V_{REF}}{R_2} \Rightarrow$$
$$V_{OUT} = I_{R1} * R_1 + V_{REF} = \frac{V_{REF}}{R_2} * R_1 + V_{REF} \Rightarrow$$
$$V_{OUT} = V_{REF}(1 + \frac{R_1}{R_2})$$

Design

Now that the reader has an understanding as to how a linear voltage regulator functions, how the output voltage is set using resistors, and how the reference voltage plays a role in the overall system of a linear regulator, the design and implementation of the reference voltage will be discussed. To create the reference voltage, a bandgap reference voltage circuit is utilized through the use of PTAT (proportional to absolute temperature) and CTAT (complementary to absolute temperature) circuitry. The reference voltage is typically found to be a constant 1.25V due to the bandgap of silicon and is intended to remain constant independent of temperature, power supply variation, or load variation.

The PTAT circuitry creates a voltage which increases linearly over temperature (a positive temperature coefficient) and the CTAT circuitry creates a voltage which decreases linearly over temperature (a negative temperature coefficient). The goal is that the voltages of these two circuits, when added together, create a constant voltage. This constant voltage is used as a reference for the voltage regulator to accurately maintain the desired output voltage. Therefore, it is important that the CTAT and PTAT circuitry create voltages whose temperature coefficients accurately compliment one another to ensure the reference voltage does not change with respect to temperature and is stable throughout. An example of this ideal situation of how the PTAT and CTAT is supposed to interact with each other can be seen below in **Figure 4**.

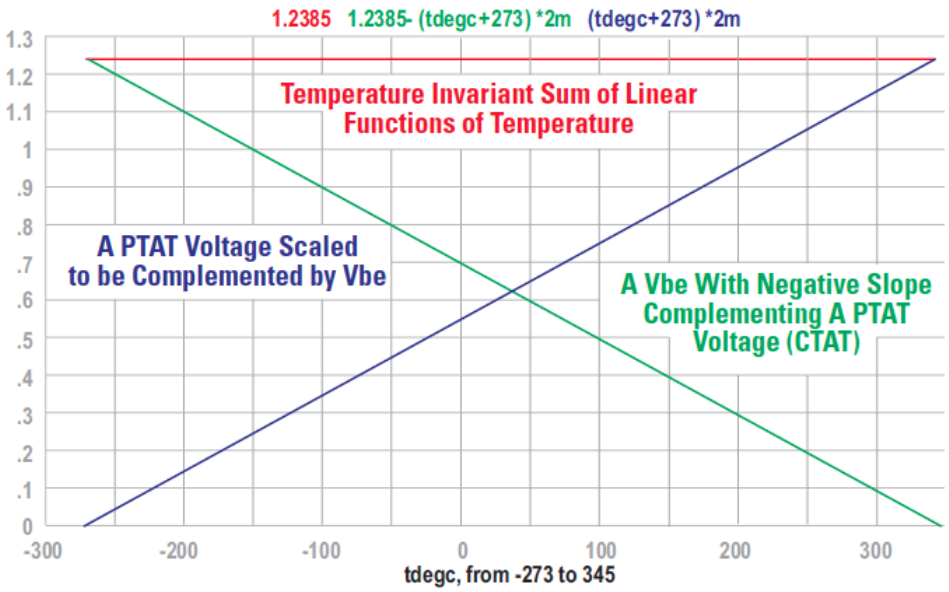


Figure 4: Reference Voltage Created Via PTAT and CTAT.
(*How to Make a Bandgap Reference Voltage in One Easy Lesson* [3])

The group decided to implement a Brokaw bandgap reference voltage circuit to create a stable reference voltage for the regulator. A view of this circuitry can be seen below in **Figure 5**.

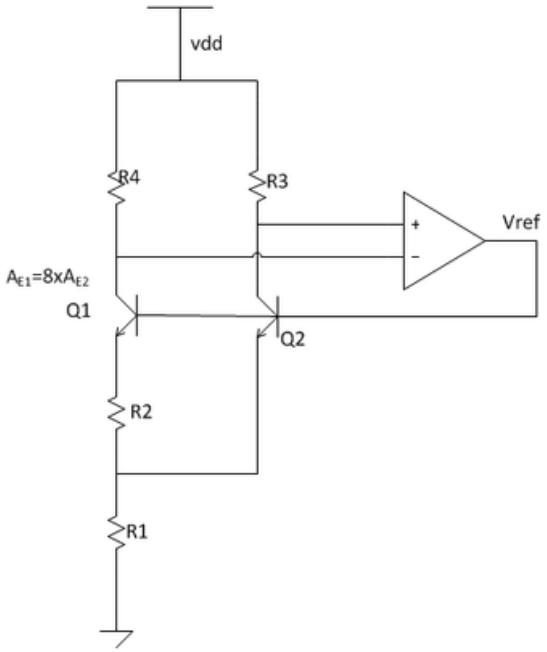


Figure 5: Brokaw Bandgap Reference Circuitry
(www.vlsi.itu.edu.tr [4])

The basic idea behind this topology is to allow for the creation of a reference voltage, as labeled V_{Ref} above, which will remain constant across temperature. The V_{BE} junction of the transistor labeled Q_2 acts as a CTAT device and the resistors labeled R_2 and R_1 act as PTAT devices.

The transistor labeled Q1 has 8X the area when compared to Q2. That is, the transistor Q1 represents eight of the Q2 transistors in parallel with the bases, collectors, and emitters tied together so that the device operates as if it were a single transistor with 8X the area as Q2. Each of these eight transistors carries ⅛ of the current that flows through Q2, so that the total current through all eight of the Q1 transistors is equal to the current through the Q2 transistor. Since each of the eight transistors carries ⅛ of the current, their V_{BE} voltages must be less when compared to the V_{BE} voltage of Q2.

Note that a BJT can be viewed as two diodes connected at the base. Thus, the base-collector junction and the base-emitter junction each create one diode. Since the diode in the base-collector junction is reverse-biased, this diode does not turn on. However, the diode in the base-emitter junction is forward biased, thus V_{BE} has a voltage drop and a current through it. From the current through a diode, the V_{BE} voltage can be found as follows.

$$I = A\, I_S(e^{\frac{q*V_{BE}}{kT}} - 1) \sim I = A\ \ I_S(e^{\frac{q*V_{BE}}{kT}}) \Rightarrow V_{BE} = \frac{kT}{q} ln(\frac{I}{A})$$

Now, recognizing that the voltage across R_2 is V_{BE1}-V_{BE2}, the voltage across R_2 can be found to be:

$$V_{R2} = \Delta V_{BE} = V_{BE1} - V_{BE2} = \frac{kT}{q} ln[(\frac{I_{c1}}{I_{c2}})/(\frac{A_2}{A_1})]$$

Assuming that the currents through both Q1 and Q2 are the same and noting that A1=8A2, this equation can be reduced to the following:

$$V_{R2} = \Delta V_{BE} = V_{BE1} - V_{BE2} = \frac{kT}{q} ln(8)$$

As can clearly be seen from this equation, the voltage across the resistor labeled R_2 is proportional to temperature. Since the voltage across the resistor R_2 is a PTAT, the current that flows through R_2 must also be a PTAT. In fact, the current through resistor R_1 is also a PTAT since the current that flows through R_1 will rise as temperature increases [5]. Therefore, the voltage across R_1 also acts as a PTAT voltage. When the resistor value for R_1 is chosen such that it will have a temperature coefficient that is exactly opposite the CTAT voltage produced by the V_{BE} voltage of the transistor, then the reference voltage equal to $V_{REF} = V_{R2} + V_{BE2}$ should

remain constant at a voltage around 1.25V. That is, the summation of these two voltages creates a stable voltage that should not deviate.

To correctly set up the Brokaw Bandgap circuit in **Figure 5**, it is important to set up the voltages at the input of the op-amp correctly. The positive terminal of the op-amp should be larger than the negative terminal of the op-amp, else the op-amp will not function correctly and act as a latch. This will cause the output of the op-amp to hit the voltage rails.

In the end, the group decided to alter the design slightly by adding a current mirror instead of using the op amp circuitry mentioned above. This allowed the collector currents of the transistors labeled Q1 (consisting of 8 transistors in parallel) to be equal to the current in Q2, which is the intended goal of the op amp.

With that said, the design aspect of this project began by designing the Brokaw bandgap reference circuitry. However, in order to design a reference voltage the behavior of the components being used to create this reference voltage must be known. Therefore, the bipolar junction transistors were characterized and their collector current vs. beta plots were generated. The only NPN and PNP PCELL bipolar junction transistors available from the IBM technology library are labeled as VNPN and VPNP, respectively. Therefore, data was collected with respect to the VNPN BJT and the schematic used to collect this data can be seen in **Figure 6**.

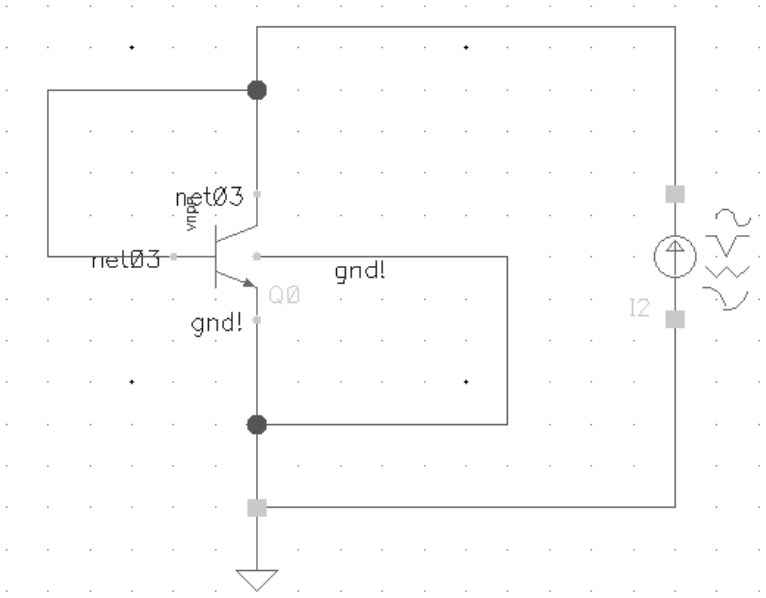


Figure 6: Schematic Used to Characterize VNPN BJT.

The current source was then swept from 1uA to 750uA for a 5V supply and various measurements were taken as shown in **Table 2**.

Table 2: Experimental Data Used to Characterize VNPN BJT.

Ie (uA)	Ic (uA)	Ib (uA)	Beta (DC)	VBE (V)	Beta (AC)
100	96.4200	3.576	26.9631	0.8222	18.25
80	77.4000	2.598	29.7921	0.8114	20.58
60	58.2500	1.746	33.3620	0.7984	24.39
40	38.9600	1.025	38.0098	0.7819	29.56
20	19.5600	0.4398	44.4748	0.7568	37.88
10	9.7990	0.2011	48.7270	0.7346	44.41
5	4.9040	0.09586	51.1579	0.7141	48.75
1	0.9814	0.01863	52.6785	0.6693	52.82
0.1	0.0980	0.001969	49.7867	0.6074	52.1
0.01	0.0098	0.000233	41.9099	0.5461	46.98
0.001	0.0010	0.00003294	29.3139	0.4849	36.78
0.0001	0.0001	0.000005765	16.1249	0.4233	23.13

From this data, the collector current versus the beta of the VNPN transistor was plotted and is shown in **Figure 7**.

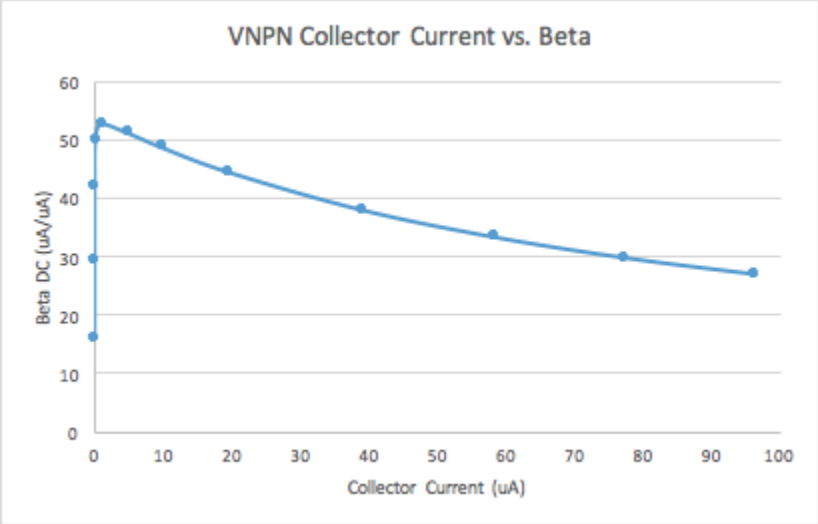


Figure 7: Characterization of VNPN Bipolar Junction Transistor.

Next, the VPNP BJT was characterized. The schematic used to characterize this transistor is shown in **Figure 8**.

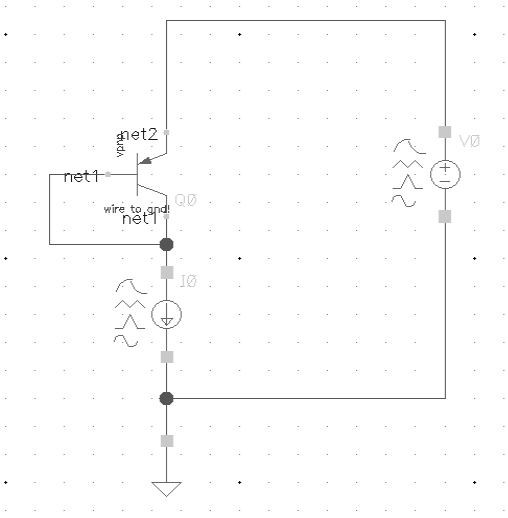


Figure 8: Schematic Used to Characterize VPNP BJT.

As was performed with the VNPN, the current source was then swept from 1uA to 750uA for a 5V supply and various measurements were taken using the VPNP BJT as shown in **Table 3**.

Table 3: Experimental Data Used to Characterize VPNP BJT.

Ie (uA)	Ic (uA)	Ib (uA)	Beta (DC)	|VBE| (V)	Beta (AC)
100	98.40000	1.60000	61.50000	0.6702	48.08
80	78.79000	1.21100	65.06193	0.6626	52.87
60	59.14000	0.85730	68.98402	0.6533	58.67
40	39.46000	0.54000	73.07407	0.6408	65.78
20	19.74000	0.25780	76.57099	0.6207	74.3
10	9.87100	0.12870	76.69775	0.6016	78.41
5	4.93400	0.06614	74.59933	0.5831	79.19
1	0.98470	0.01530	64.35948	0.5408	73.4
0.1	0.09776	0.00224	43.66235	0.4809	55.51
0.01	0.00960	0.00040	24.10495	0.4207	34.16
0.001	0.00092	0.00008	11.28687	0.3599	17.28
0.0001	0.00008	0.00002	4.71347	0.2974	7.52

From this data, the collector current versus the beta of the VPNP transistor was able to be plotted. This can be seen below in **Figure 9**.

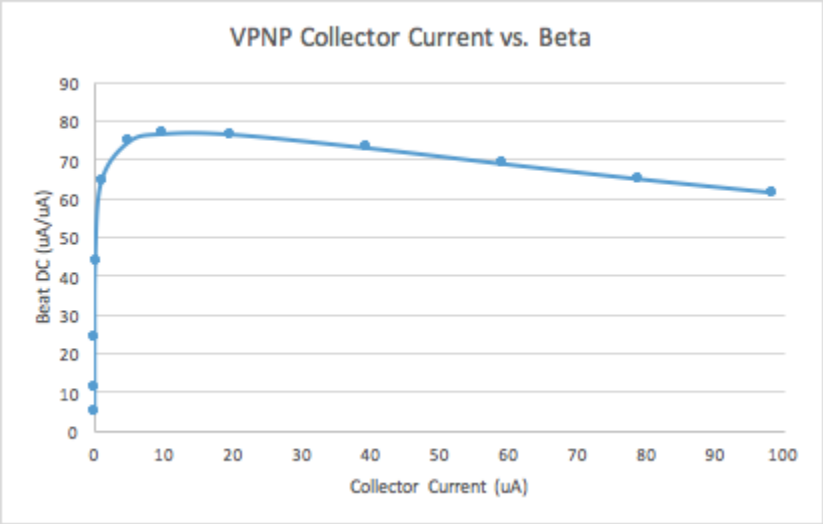


Figure 9: Characterization of VPNP Bipolar Junction Transistor.

This information was found to be valuable since it allowed for the understanding of when the bipolar junction transistors were in a stable region of operation. That is, these plots allowed for the group to understand when beta could be assumed approximately constant. Furthermore, this information allowed the group to be able to quantify how much current can be achieved through a single BJT.

Now that the bipolar junction transistors have been characterized, the MOSFET transistors were characterized. That is, the width and length ratios were adjusted and the current density calculated. The MOSFETs used in this project are the PFETX and the NFETX PCELLs in the CMHV7SF library in Cadence. The schematic used when characterizing the PFETX can be seen below in **Figure 10**.

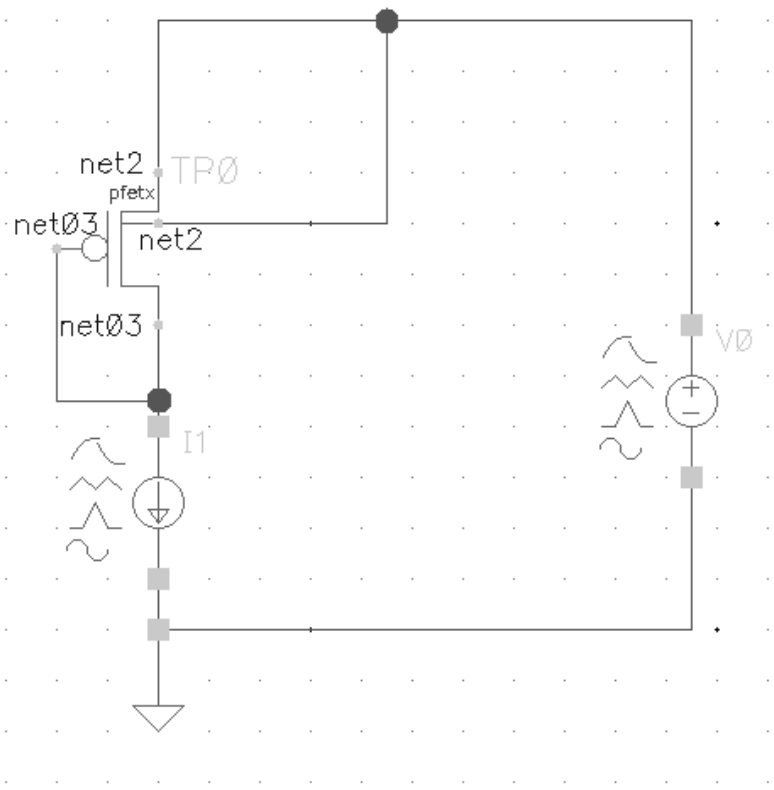


Figure 10: Schematic Used to Characterize PFETX MOSFET.

Various measurements were taken for W/L ratios of W/L=20 and W/L=10. The results obtained from characterizing the PFETX MOSFET can be seen in **Table 3**.

Table 4 : Experimental Data Used to Characterize PFETX MOSFET.

W/L	R_{OUT} (kΩ)	I_{MAX} (μA)	|VT| (V)	V_{SG} (V)	ΔV_{SG} (V)	J (uA/um)
10	307	21	0.420	0.716	0.300	5.83
20	48	53.5	0.420	0.718	0.300	14.86

Most of the above information was calculated through the use of the calculator tool in Cadence. The current I_{MAX} was found by sweeping the current from 1uA to 750uA and finding the voltage at 5V - ($|V_T| + \Delta V_{SG}$). An overdrive voltage of ΔV_{SG} = 300mV was desired for this design since this allowed for approximately 300mV of noise to be present without disrupting the system performance. From these measurements and calculations, current densities were obtained. For W/L=10, a current density of 14.86 uA/um was obtained and for W/L=10, a current density of 5.83 uA/um was obtained. From this information, it is clear that a higher current density is able to be obtained when W/L=20. Therefore, all transistors used in this project were chosen based on these findings.

Now that the bipolar junction transistors and MOSFETs being used in this design have been characterized, the design of the Brokaw bandgap reference is able to be completed. Based on the discussion in the introduction section of this paper, it is assumed that the reader has an overall understanding of how the brokaw bandgap reference voltage is intended to function. Therefore, the Brokaw bandgap circuit was next modeled in Cadence using BJT PCells, as shown in **Figure 11**.

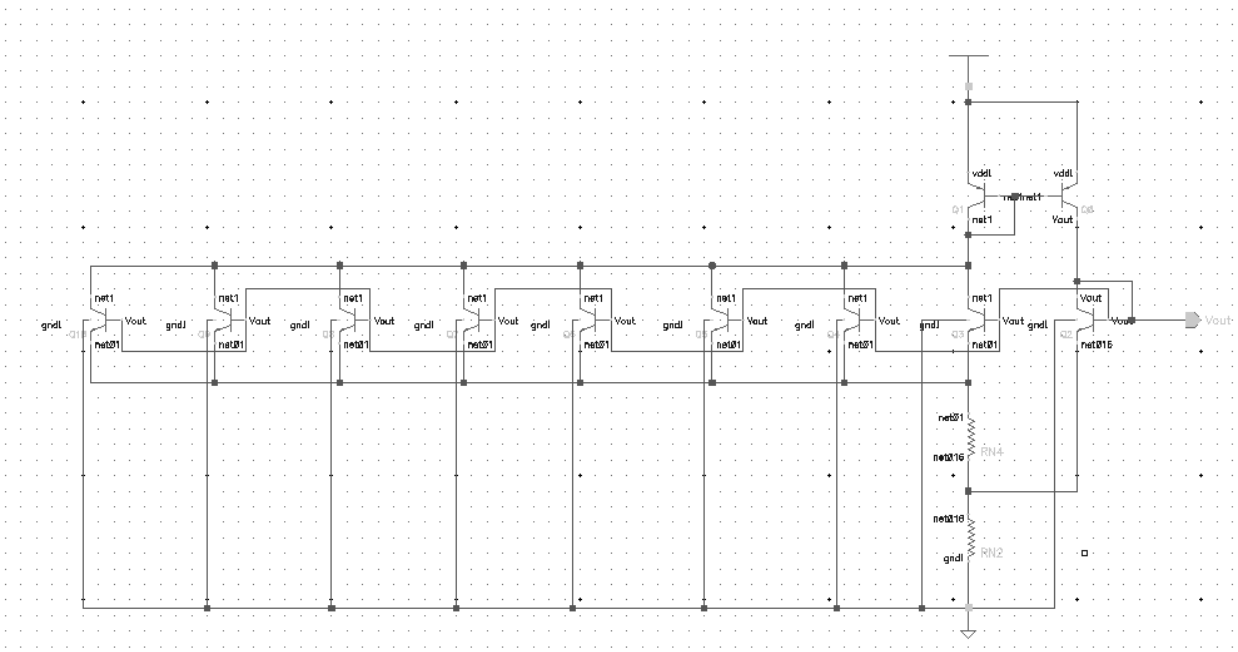


Figure 11: Brokaw Bandgap Circuit using Cadence PCells

The use of PCells expedited the process when compared to having to draw the BJTs using layers. Unfortunately, the process used in this class, CMHV7SF, provides no control over the size and doping concentration of the BJTs. Thus, 8 BJTs were used in parallel to represent the transistor Q1 having 8X the area of Q2.

Furthermore, the resistor value that set up the PTAT voltage in Cadence had to be adjusted. After adjusting this resistor using an iterative approach, the Brokaw Circuit was able to output a voltage that was close to being constant across the desired temperature range, as shown in **Figure 12.**

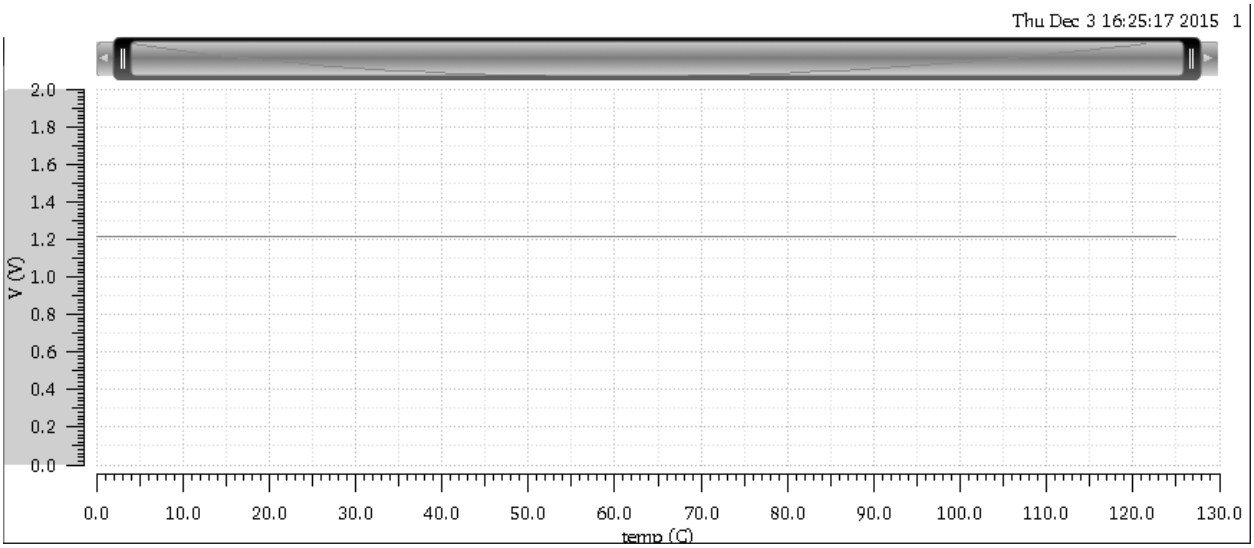


Figure 12: Reference Voltage Output of the Brokaw Bandgap

As can be seen from the above plot, the reference voltage appears to be approximately constant over the temperature range of 0□ to 125□. However, when zoomed in the voltage variation across temperature appears to be more of a bathtub shape, as can be seen below in **Figure 11**.

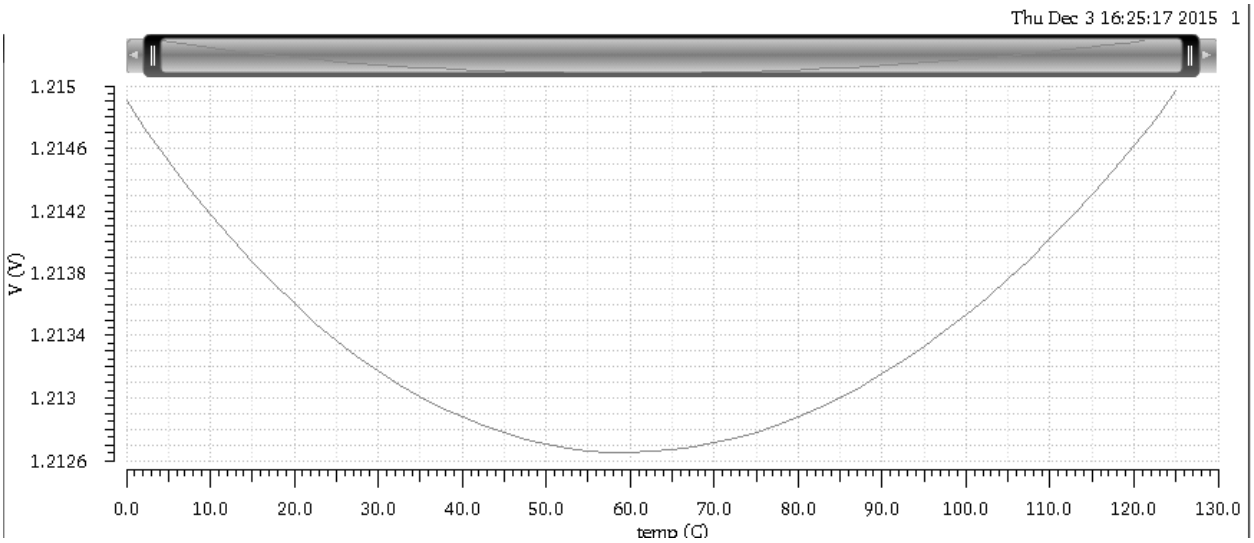


Figure 13: Zoomed in Reference Voltage Output of the Brokaw Bandgap

As shown, the reference voltage deviates approximately 2.4mV at most over the swept temperature range. Although this value is not close to 100 ppm as some of the top performing current bandgap voltages available on the market today, the group is very satisfied with this result. Of note is that the output voltage is in the range of 1.215V to 1.2126V. This is as expected due to the fact that bandgap voltage references commonly have an output voltage around 1.25V since this value is close to the theoretical bandgap energy of silicon (~1.22 eV) [5].

This design was found to simulate well in Cadence but was determined to have a fundamental flaw. The current mirror utilizes two VPNP bipolar transistors. After researching the CMHV7SF technology more thoroughly, it was found that the collector terminal of the VPNP bipolar transistor is tied to the substrate. Therefore, it was found that this transistor is intended to be used in bandgap circuits only and not used otherwise. It was found interesting that these results were able to be achieved in simulation with the collector not tied to the substrate since the device inherently had this property.

Therefore, since the VPNP bipolar transistor is the only pnp transistor available in the CMHV7SF technology, the current mirror was determined to be unable to be implemented using bipolar technology. Thus, MOSFETs were utilized for the current mirror.

Various types of current mirror options were explored in order to get the most accurate current mirror and reference voltage. The design was modified using various types of current mirrors and various multiplicities of transistors in order to allow the desired amount of current to flow in the current mirrors. First, a simple PMOS current mirror was simulated and this schematic can be seen below in **Figure 14**.

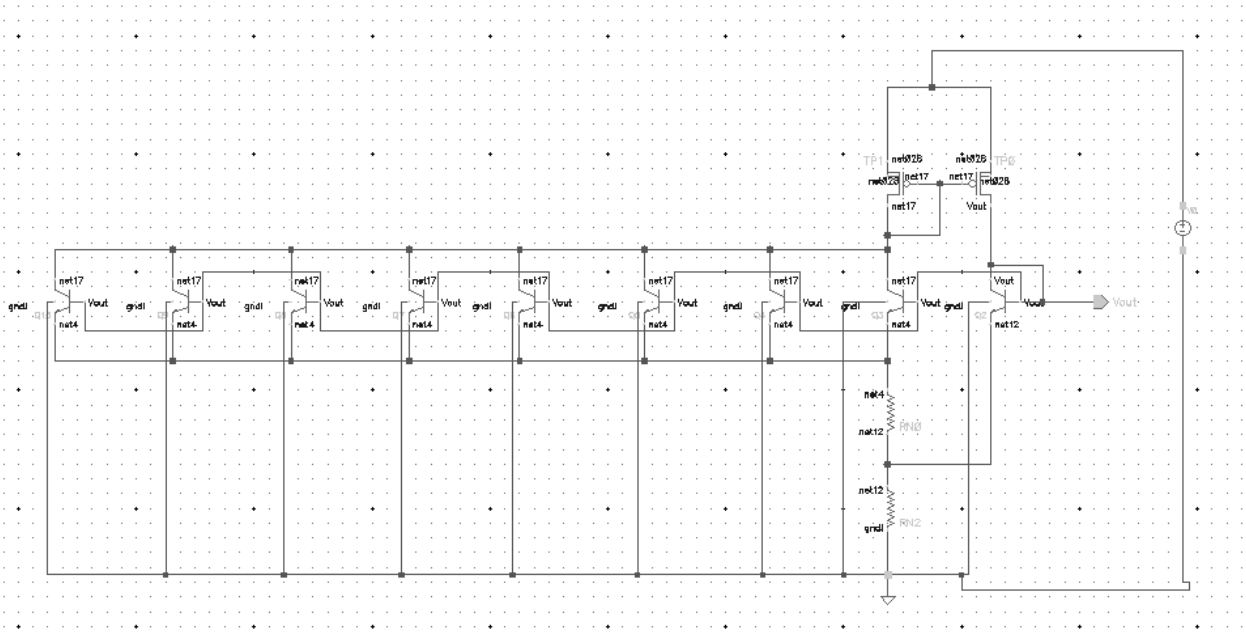


Figure 14: Bandgap Reference with Simple PMOS Current Mirror.

Zooming in on the current mirror allows for a better understanding of how the terminals are connected as shown in **Figure 15**.

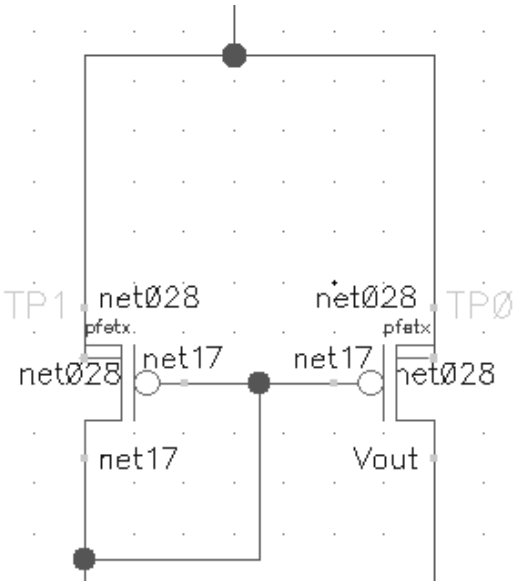


Figure 15: Simple PMOS Current Mirror.

From the above schematic, the output plots of the currents through the current mirror can be seen in **Figure 16**.

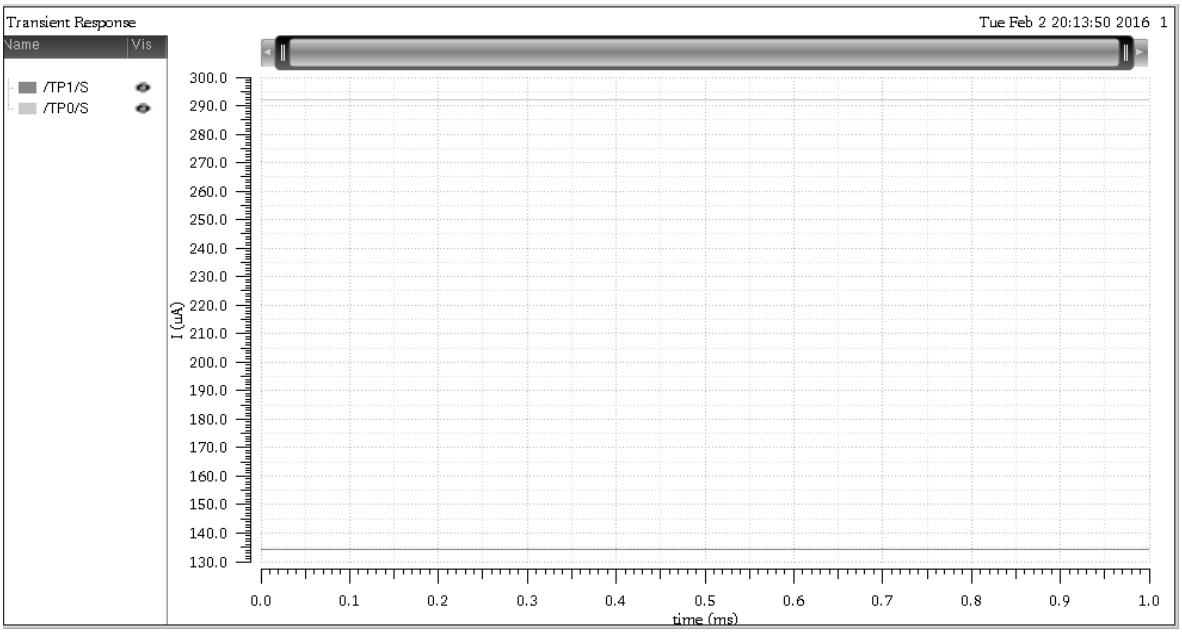


Figure 16: Currents in the Simple PMOS Current Mirror.

As can be seen, the current I1=135uA is not mirrored well in the second transistor as I2=290uA. This was determined to be due to channel-length modulation. Therefore, the multiplicities of the transistors were increased while the length was increased. This allowed for the same desired current to flow through the devices while decreasing the effects of channel-length modulation.

The simulated output transient response using higher multiplicity and length transistors at T=25□ can be seen in **Figure 17**.

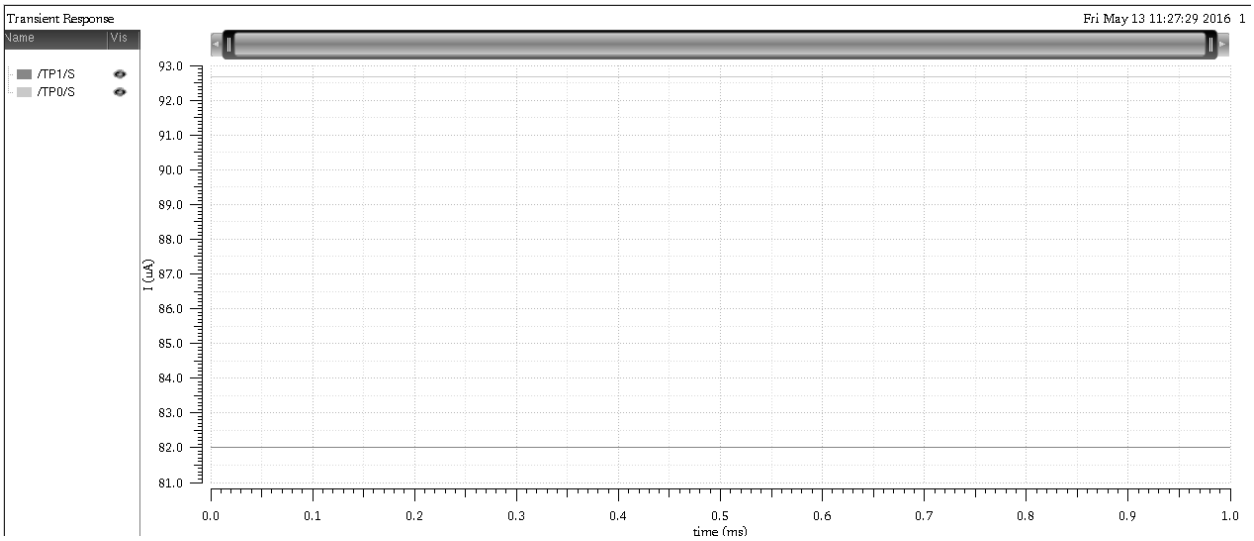


Figure 17: Currents in the Simple PMOS Current Mirror with M=3.

As shown in **Figure 17**, the currents are approximately equal to I1=82uA and I2=92.7uA. These are fairly good values. However, several transistors are required in order to obtain these results due to the higher multiplicities. Based on these observations, more types of current mirrors were researched in order to design a better performing current mirror for the bandgap reference circuitry with smaller in size and fewer transistors. Therefore, a cascoded PMOS current mirror was created. The schematic for this design can be seen in **Figure 18**.

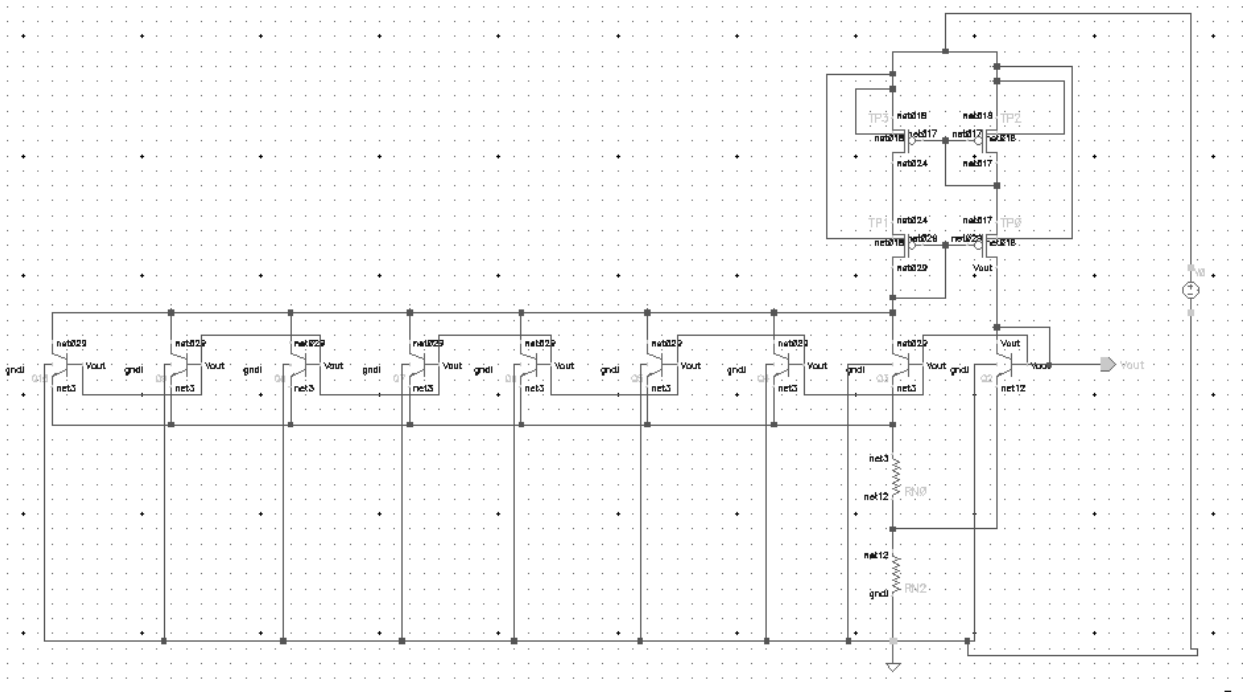


Figure 18: Bandgap Reference with Cascaded PMOS Current Mirror.

Observing the current mirror allows for a better understanding of how the terminals are connected as shown in **Figure 19**.

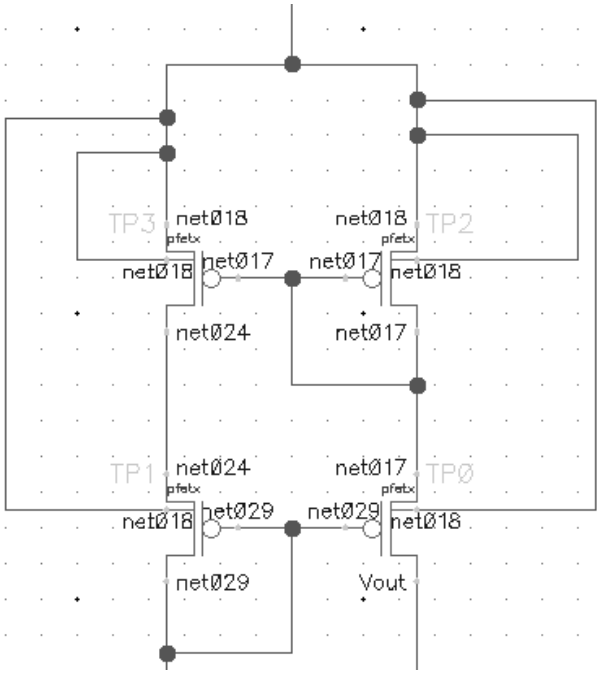


Figure 19: Cascoded PMOS Current Mirror.

From the above schematic in **Figure 19**, the currents through the current mirror were observed and can be seen below in **Figure 20**.

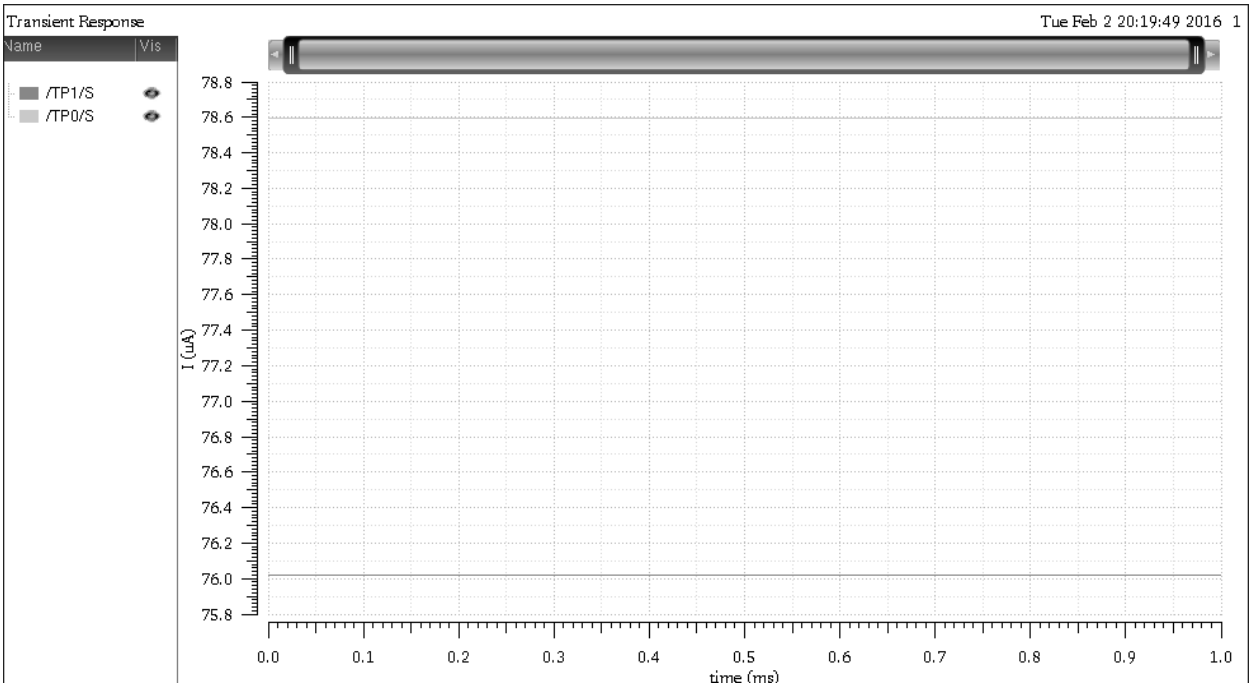


Figure 20: Currents in the Cascoded PMOS Current Mirror.

As shown in **Figure 20**, these two currents are quite close to one another. The current is mirrored quite well with the two currents equaling 78.6uA and 76uA, leaving a small discrepancy of 2.6uA; which corresponds to about 3% error. This design was found to be an accurate enough current mirror for the regulator design. However, this current mirror was not implemented since it required too much voltage to operate.

That is, the total V_{DS} voltage is approximately twice that of the simple PMOS current mirror, which only required one V_{DS} drop of supply voltage and the cascoded current mirror requires two V_{DS} voltage drops. This is important since the power rail may have noise which could reduce the voltage on the supply and cause the current mirror to drop out of the desired region of operation. If the current mirror were to fall out of operation, so would the entire regulator.

Therefore, for a robust design the linear voltage regulator should be able to handle as much voltage variation on the power rail as possible. This is accomplished with the current mirrors requiring as little V_{DS} voltage as possible so that in the event that the supply voltage increases or decreases, the current mirrors and thus the circuit will still operate as intended. Therefore, another current mirror was explored. This current mirror will be called the Prodanov current mirror since it was discussed in a paper co-authored by Professor Vladimir Prodanov [6]. The Prodanov current mirror circuitry can be seen in **Figure 21**.

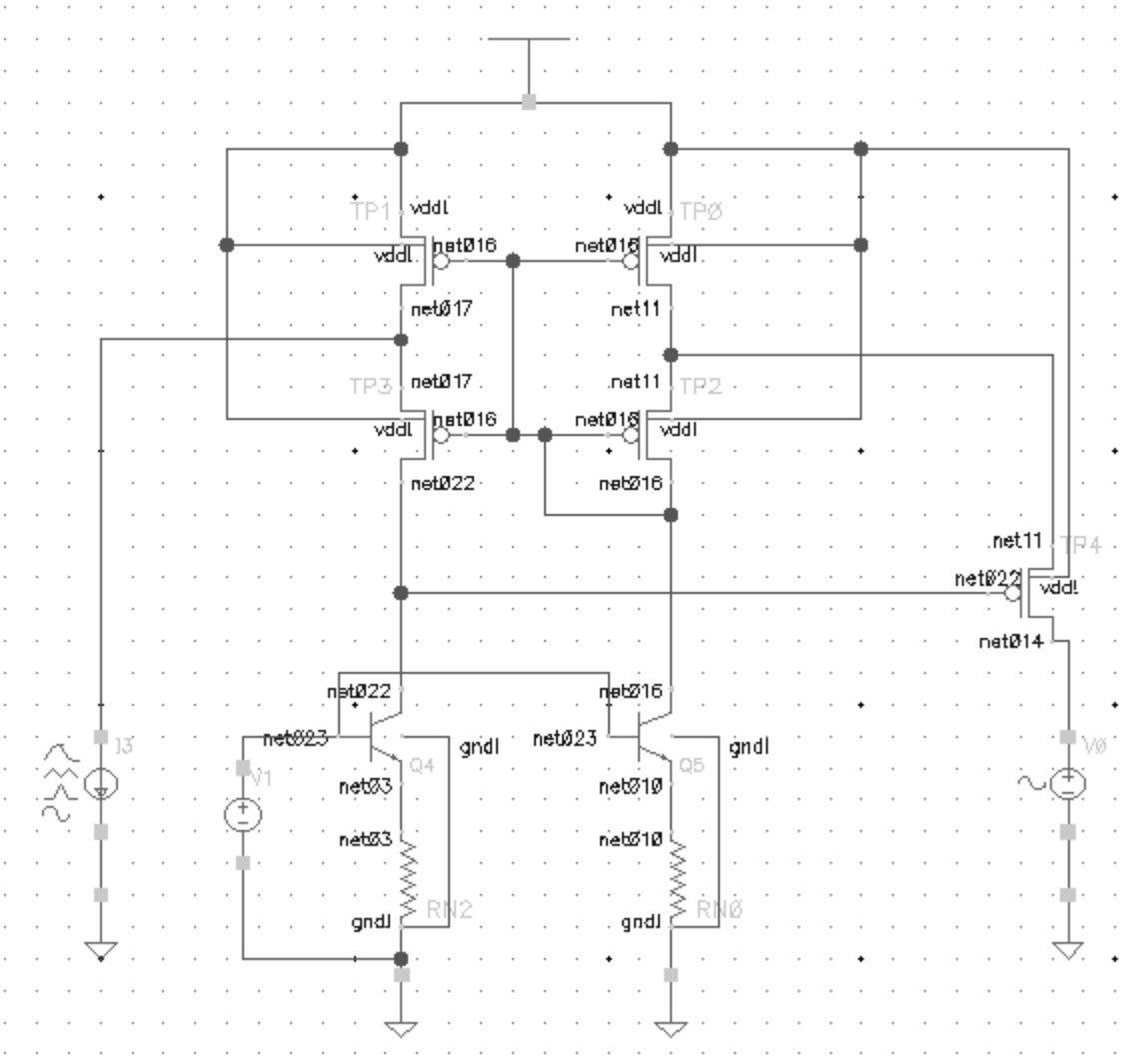


Figure 21: Prodanov Current Mirror Schematic.

This schematic operates by providing mirrored current from the node consisting of the drain of transistor TP1 and the source of transistor TP3. This current is mirrored through the source of transistor TP4. Using the above schematic, the voltage source V0 was swept while a current of 60uA was held constant by the current source I3; the current value was generically chosen. The current through the current mirror can be observed as V0 is swept in **Figure 21**.

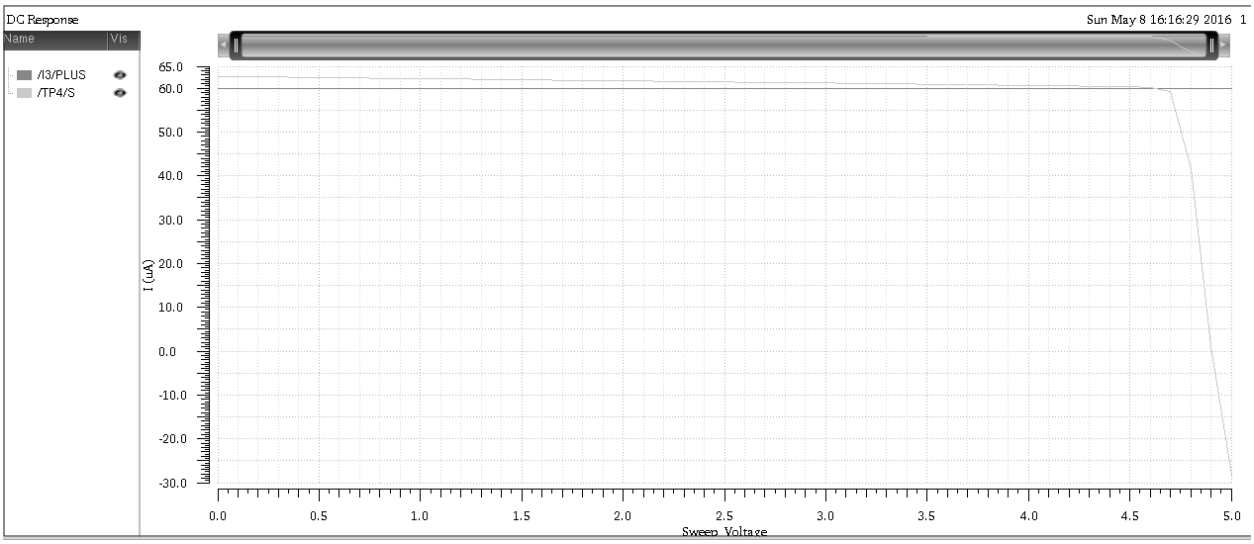


Figure 22: Prodanov Current Mirror Simulation.

As can be seen in **Figure 22**, the currents are mirrored very closely. That is, the currents being mirrored are approximately 62uA to 60uA; again, with a discrepancy of 3% between the two currents. This topology was found to be accurate enough for the reference voltage current mirror and to allow for a low enough supply voltage so that this current mirror can operate in a system where a lot of supply noise may occur.

Once the design of the current mirror was complete, the design of the reference voltage could be finished. Thus, the schematic used in **Figure 11** was referenced when designing the reference voltage with the simple PMOS current mirror replaced with the Prodanov current mirror. Therefore, the bandgap reference with the Prodanov current mirror can be seen in **Figure 23**.

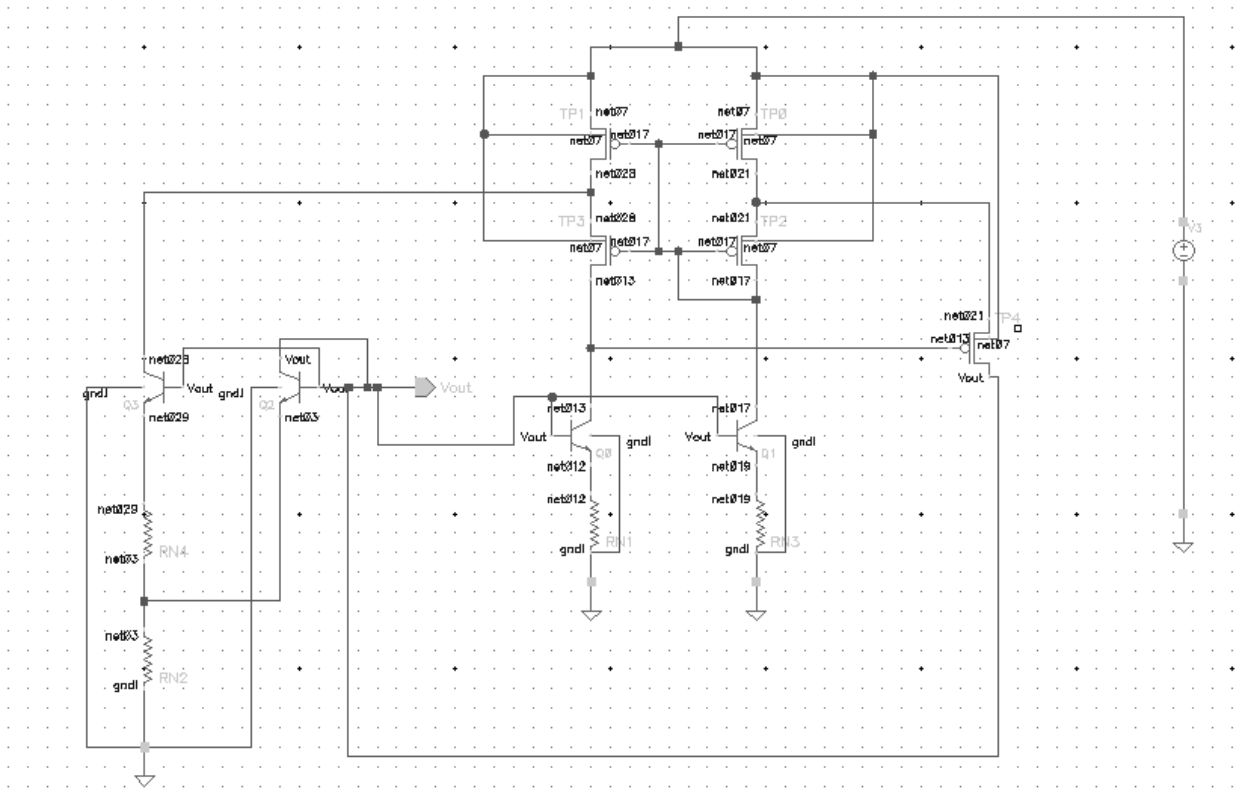


Figure 23: Bandgap Reference Circuitry with Prodanov Current Mirror.

Of note is that the eight bipolar junction transistors that were in parallel in the original bandgap reference in **Figure 11** are now replaced with a single bipolar transistor in the schematic with a multiplicity of 32. Thus, the transistor labeled Q3 in **Figure 23** has a multiplicity of 32 and represents 32 transistors with all their bases connected, collectors connected, and emitters connected. Similarly, a transistor with a multiplicity of 32 represents a single transistor with a width equal to thirty-two times the original width and the same length.

In addition, Q2 was designed to have a multiplicity equal to 4. These multiplicities were chosen since they allowed for the transistor labeled Q2 to be able to handle the desired current of approximately 100uA. Since Q3 has 8x the area of Q2 in our design, Q3 thus was chosen to have a multiplicity of 32. Once the Prodanov current mirror had been connected to the bandgap reference, the currents were observed through the two branches of the current mirror as shown in **Figure 24**.

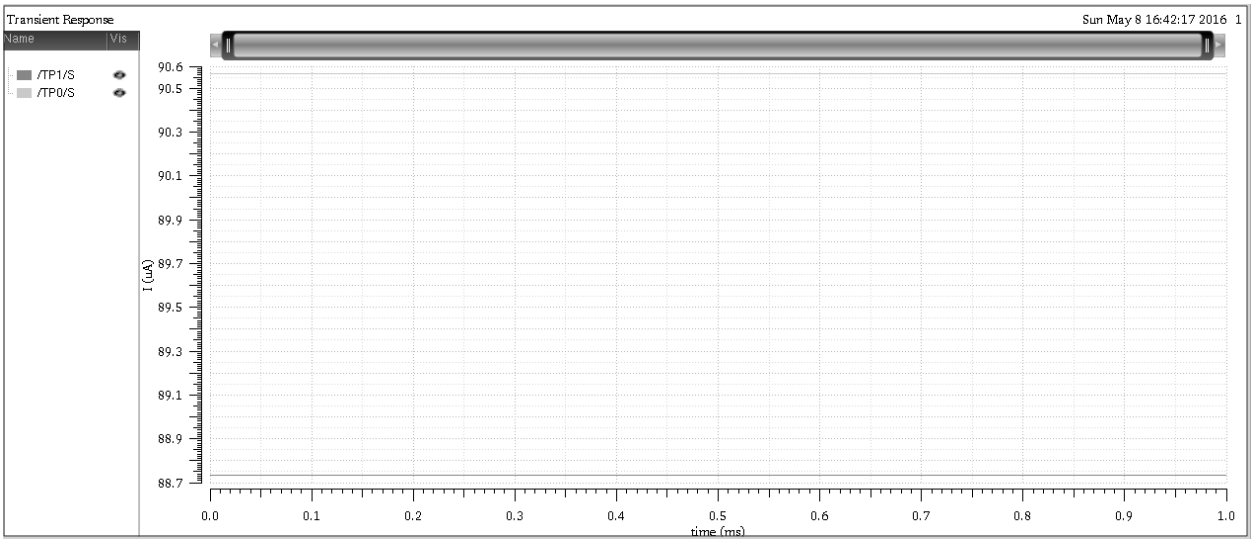


Figure 24: Currents in the Prodanov Current Mirror.

As seen in **Figure 24**, the currents in the two branches of the current mirror are 88.7uA and 90.6uA; yielding a discrepancy of 2% between the two currents. These are ideal values since the currents are very close to one another. Next, the PTAT resistor labeled RN2 in **Figure 23** was iteratively adjusted until the temperature coefficient of the output voltage was minimized over the temperature range of -40□ to 100□. This temperature range was chosen since this is the industrial temperature range typically used for integrated circuits. The optimized output voltage across temperature simulated plot of the bandgap reference using the Prodanov current mirror can be seen below in **Figure 25**.

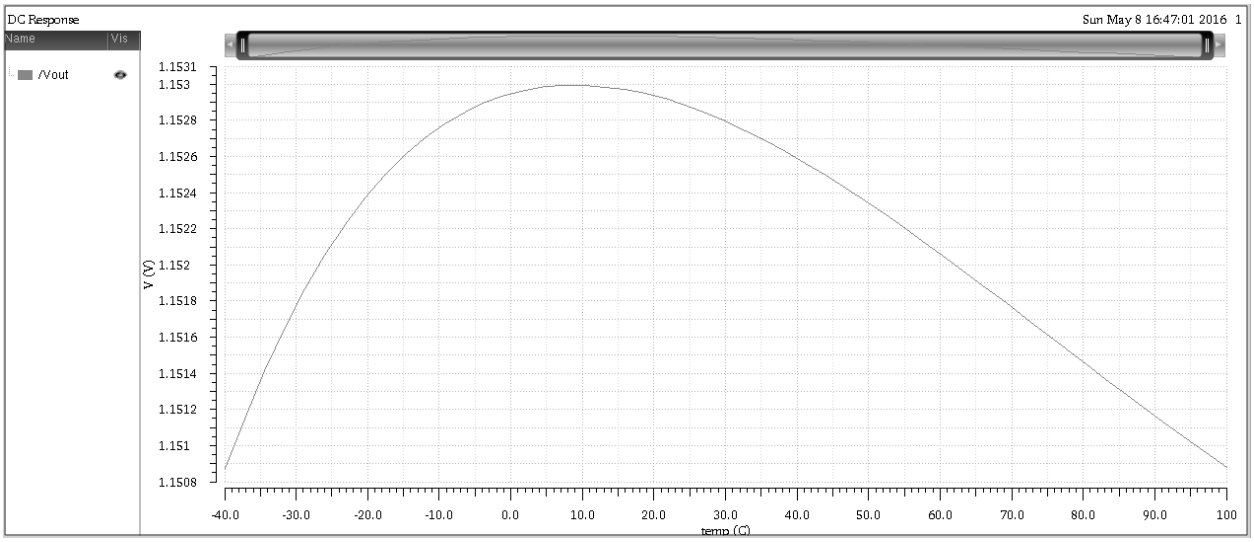


Figure 25: Optimized Output Voltage of Bandgap Reference Across Temperature.

As seen in **Figure 25**, the output voltage of the bandgap reference deviates approximately 2.2mV over the temperature range of -40□ to 100□. This is a very desirable result since the reference voltage has shown the ability to maintain an approximately constant voltage over the intended operating temperature range of the IC. In addition, the transient response of the bandgap reference was plotted at 25□. This plot is shown in **Figure 26**.

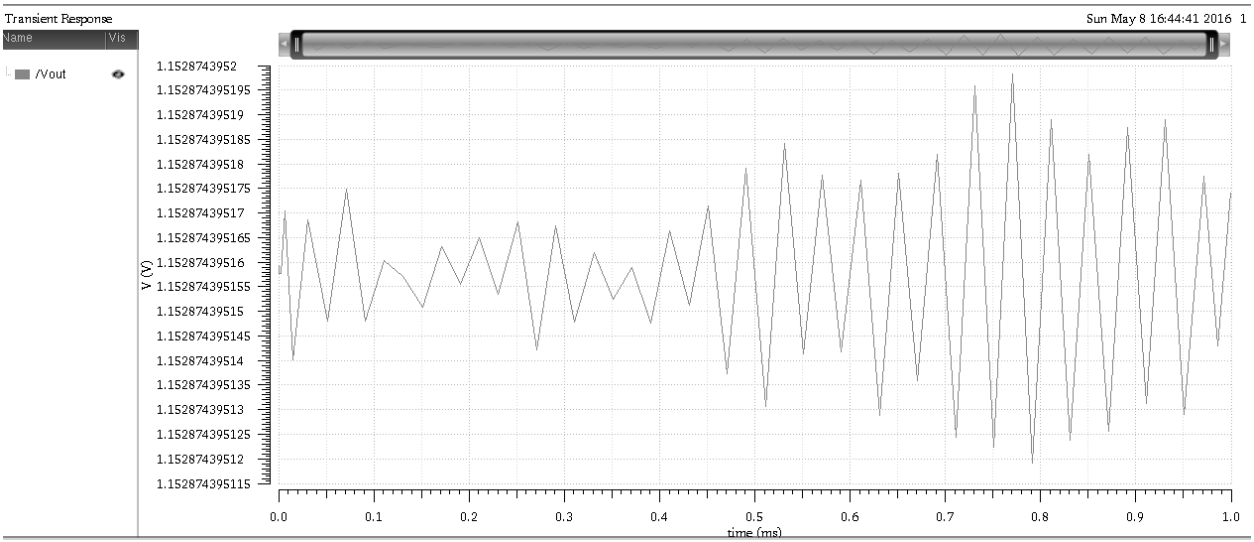


Figure 26: Transient Response of Bandgap Reference at 25℃.

As can be seen, the transient response shows the output voltage deviating by approximately 10nV maximum over the 1ms plot shown. This is a very small deviation, which allows for an accurate reference.

Now that the design of the bandgap reference had been finalized, the error amplifier was designed. The error amplifier is a transconductance amplifier since the amplifier takes an input voltage and outputs current. The amplifier is designed to use the approximately 1.15V reference voltage designed previously as the input to the positive terminal of the op amp. The negative terminal of the op amp is then used in a resistive feedback network in order to gauge the output voltage. The output current of the error amplifier is then used to adjust the amount of current flowing through the resistive feedback network and the load, which sets the output voltage of the entire linear voltage regulator. The error amplifier schematic can be seen below in **Figure 27**.

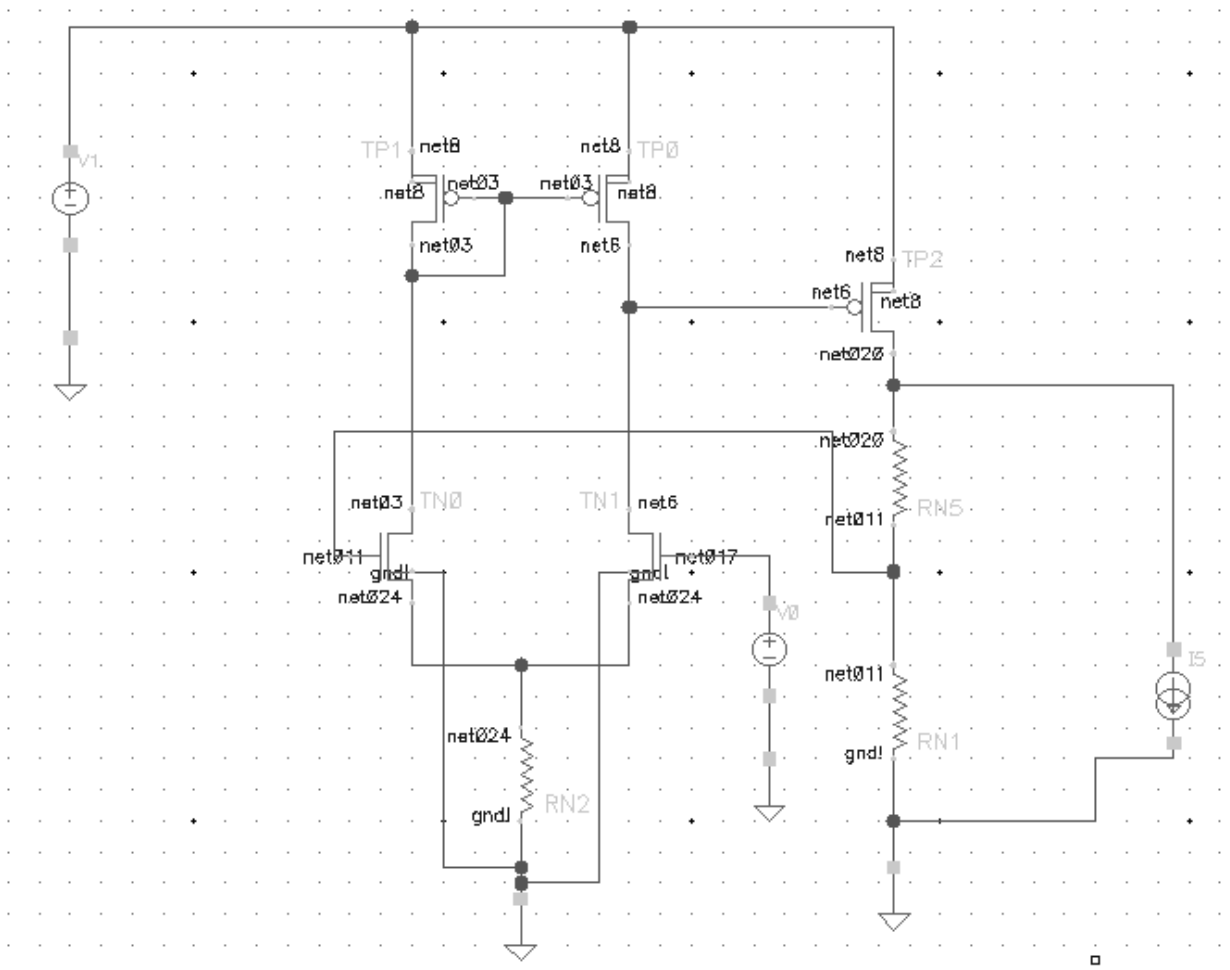


Figure 27: Error Amplifier Schematic.

As shown, the positive terminal of the op amp, labeled net017 in **Figure 27** above, is attached to a 1.15V source which simulates the bandgap reference being attached at that node. The negative terminal of the op amp, labeled net011 above, is attached between two resistors. These are the two resistors which are attached externally to the voltage regulator device and are used when setting the output voltage. For this simulation, an output voltage of approximately 3.23V was achieved through this resistor ratio. The calculation used to determine this value can be seen below.

$$V_{OUT} = V_{REF}(1 + \frac{R_1}{R_2}) = (1.152V)(1 + \frac{18.0087k\Omega}{19.0047k\Omega}) = 3.2256V$$

Furthermore, the transistor labeled TP2 is a power transistor which has a multiplicity of 80 and is the transistor responsible for adjusting the output voltage by allowing more or less current to flow through the resistive branch. This current changes the voltage at the node labeled net011 to match the reference voltage. Of note is that this transistor is required to have a high multiplicity

in order for currents in the mA range to be output of the device. That is, the load current output specification of this device is 150mA of current which is the reason for the power transistor having a multiplicity of 80.

Next, the voltage nodes net017 (positive terminal of amplifier) and net011 (negative terminals of amplifier) were plotted together. This transient response is shown in **Figure 28**.

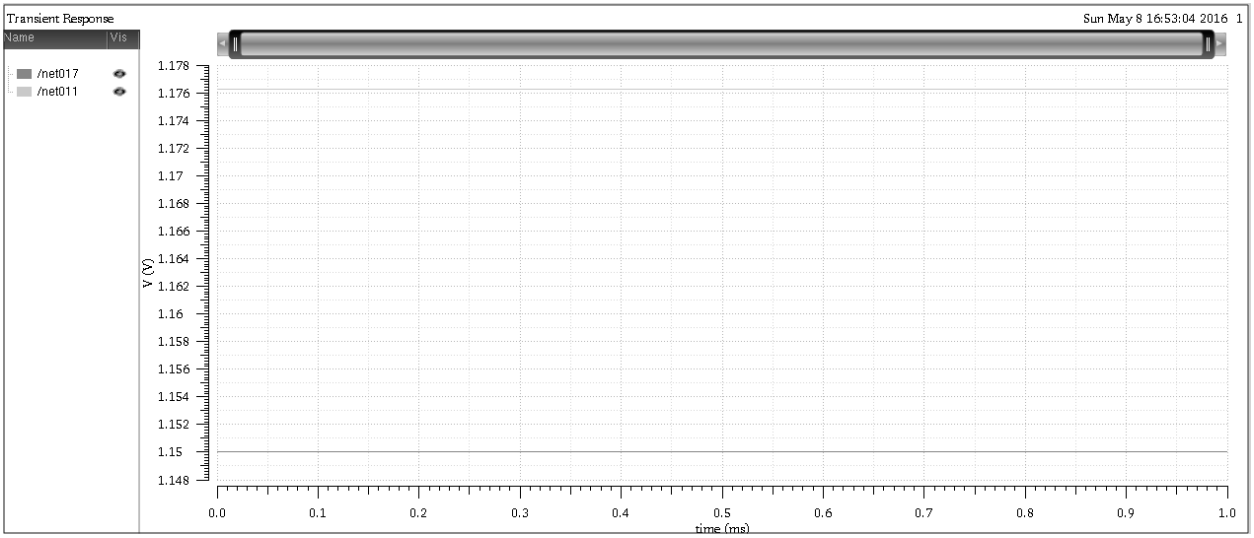


Figure 28: Simulated Transient Response of V+ and V- nodes of op amp.

As shown in **Figure 28**, the positive terminal of the error amplifier is approximately 1.176V and is intended to be the same voltage as the negative terminal of the op amp which is 1.15V. This causes a discrepancy of approximately 26mV or 2% under these testing conditions.

Moving forward, the transient response was observed for an input voltage of 5V, temperature of 25℃, and for a load current of 75 uA. This simulated output can be seen below in **Figure 29**.

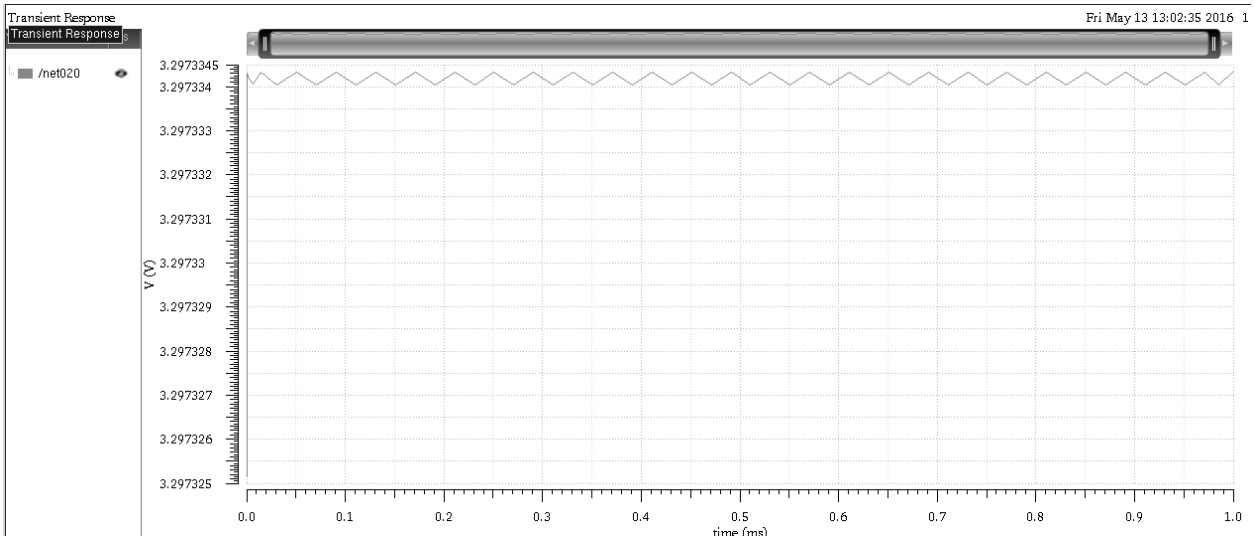


Figure 29: Output Voltage of Regulator from Error Amplifier Circuit.

As seen in **Figure 29**, the output voltage of the regulator, simulated using the error amplifier circuitry, deviates by approximately 0.5uV over time under these conditions. Next, the current was swept from 0 to 150uA and the output voltage was observed. This plot is shown in **Figure 30**.

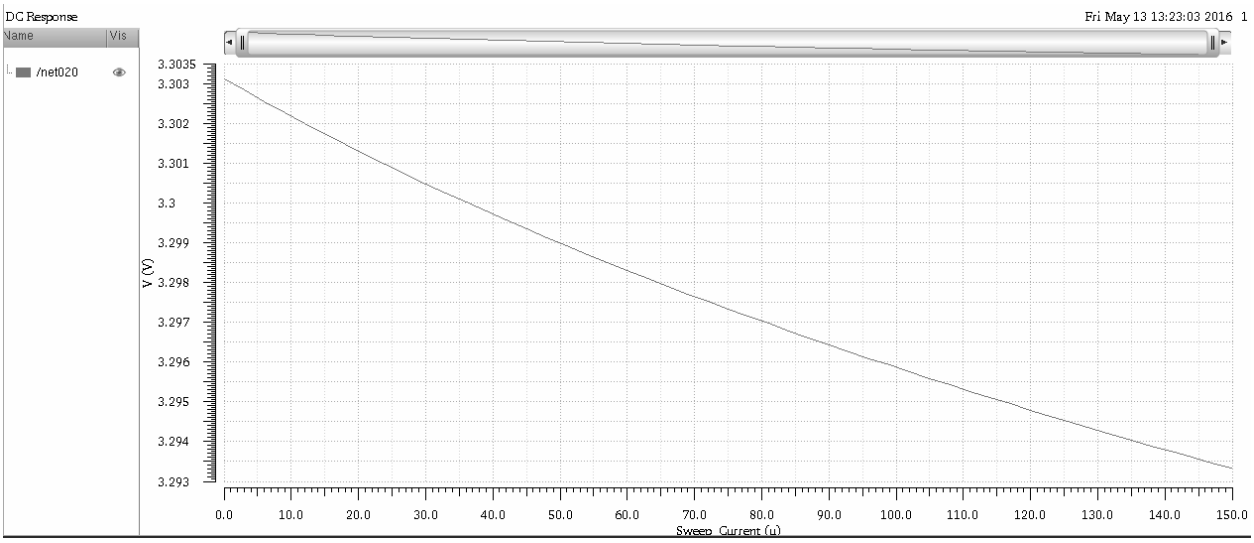


Figure 30: Simulated Output Voltage of Error Amplifier Circuit as Load Swept.

As shown, the output voltage deviates by approximately 10mV over the load current range of 0uA to 150uA. Although these results are not perfect, these results are considered good since the output voltage is approximately able to be maintained constant over this current range.

Next, the positive and negative terminal (simulated with a 1.15V source) of the op amp were simulated across the 150uA load range and can be seen in **Figure 31**.

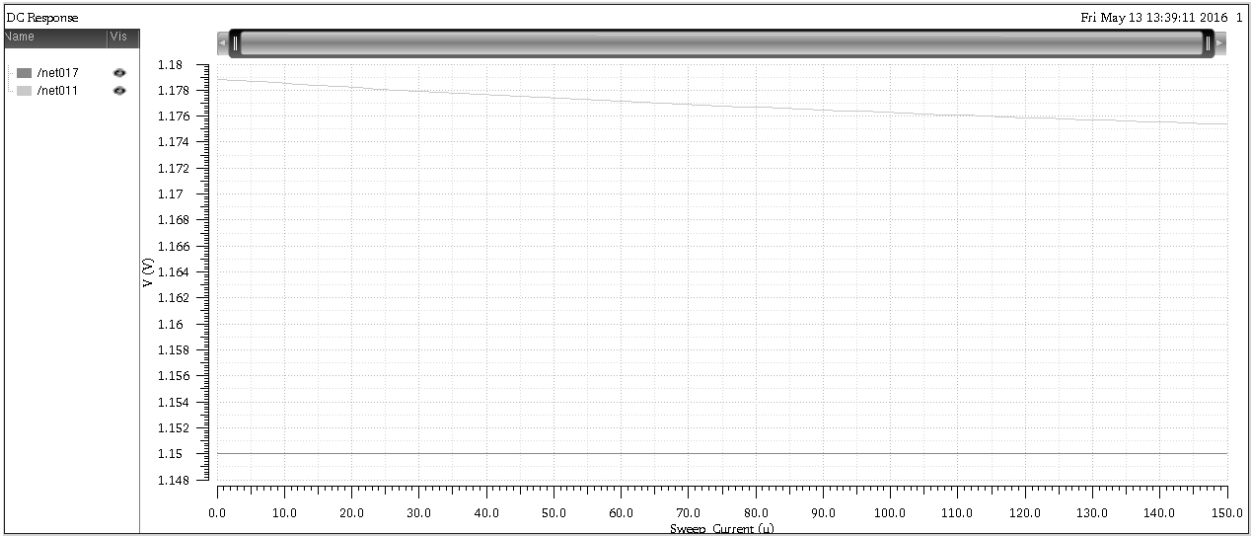


Figure 31: Positive and Negative Terminals of Error Amplifier as Load Swept.

As shown, the discrepancy of the voltage between the positive and negative terminal of the error amplifier decreases as the load current increases. The deviation between the two amplifier terminals is approximately 29mV under no load condition and approximately 25mV under full load condition of 150mA.

Next, the entire schematic was put together and simulated. The schematic of the final design can be seen below in **Figure 32** and additionally in **Appendix A** in a larger view for the reader's convenience.

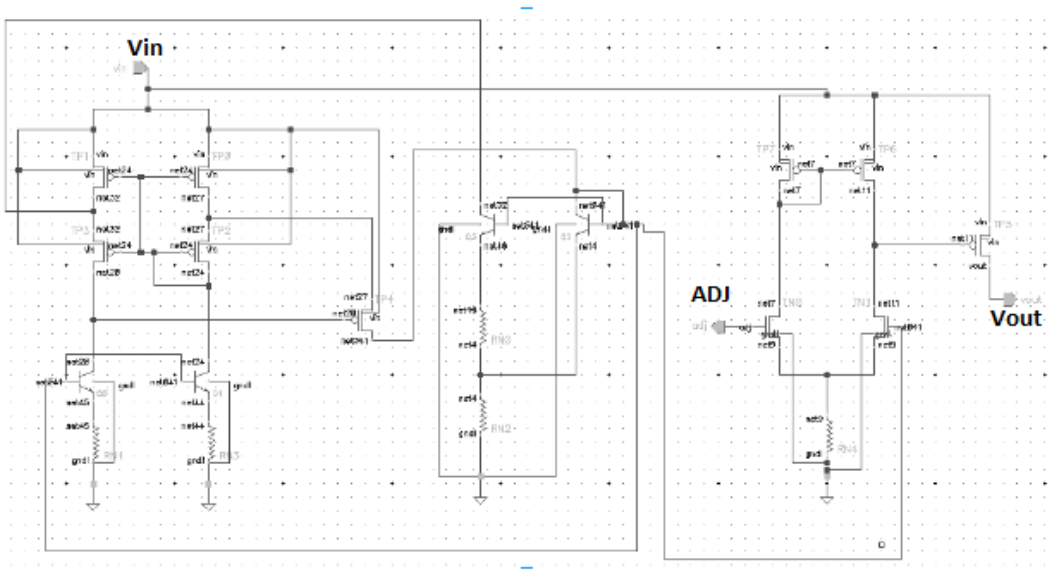


Figure 32: Final Schematic of Regulator Design

As shown in **Figure 32**, the regulator has three pins: ADJ, Vin, and Vout. Next, the schematic was simulated and the results observed. Therefore, the schematic above was altered by adding resistors in order to simulate the output voltage. This altered schematic can be seen below in **Figure 33** and is shown in **Appendix B** in a larger view for convenience of the reader.

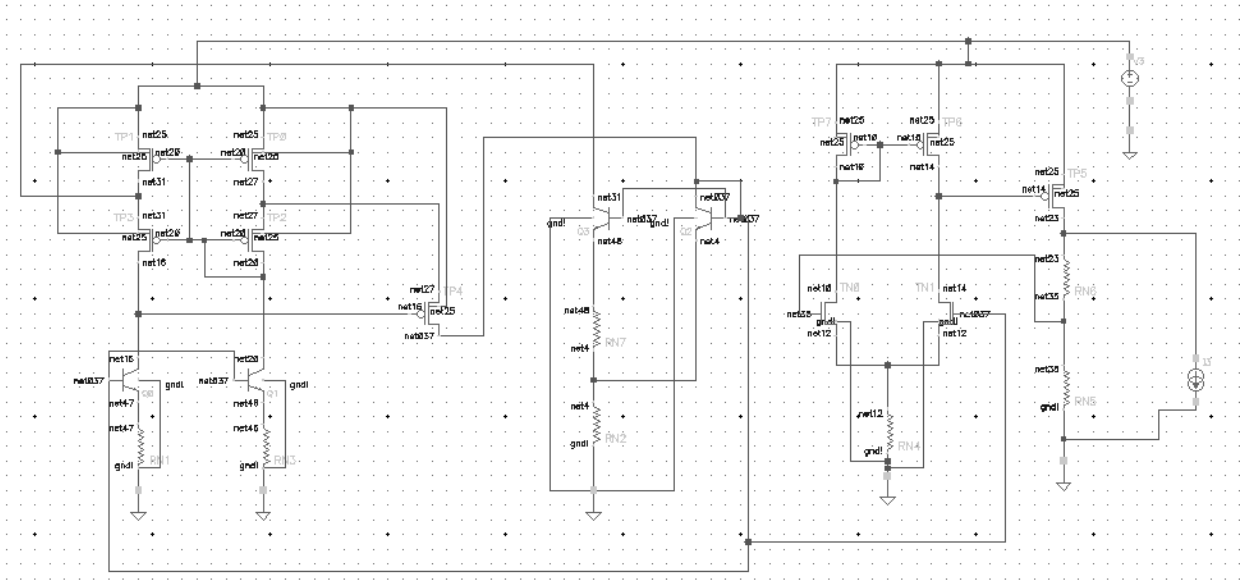


Figure 33: Final Schematic of Regulator Design Used for Simulating.

From this schematic, several simulations were performed. The resistor ratio on the output was chosen to allow for an output voltage of 3.3V. The calculation used to determine this output voltage can be seen below.

$$V_{out} = V_{ref}(1 + \frac{R1}{R2}) = 1.152V(1 + \frac{18.6567k}{10.0047k}) = 3.30024V$$

The first simulation performed was for the transient response of the output voltage with a load current of 75mA. This can be seen below in **Figure 34**.

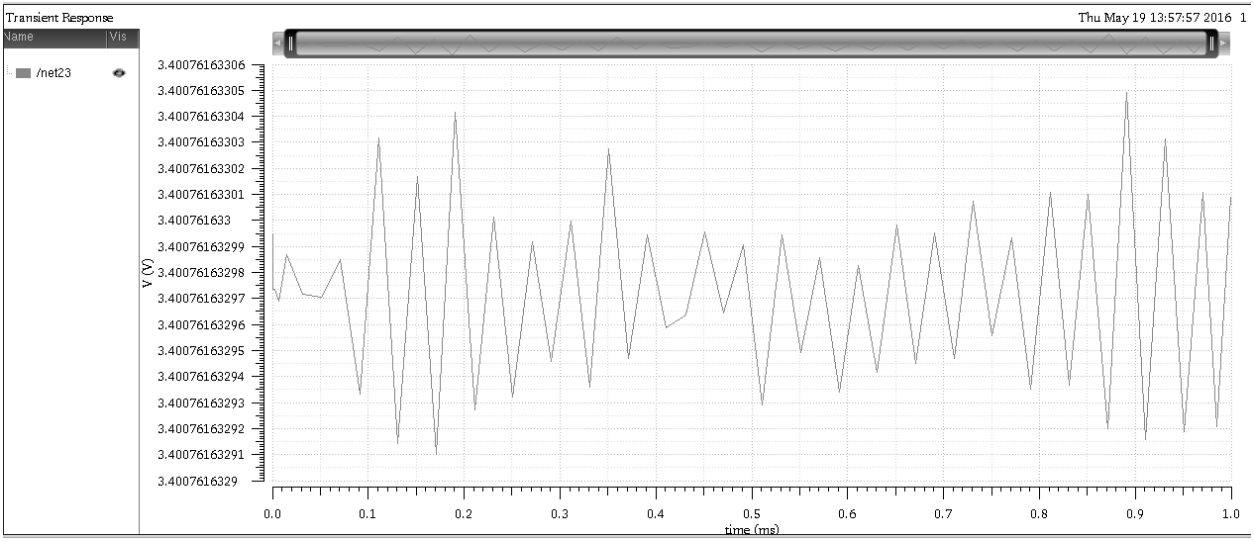


Figure 34: Output Voltage Transient Response.

As shown, the output voltage averages approximately 3.4V, which is 100mV from the intended value of 3.3V. Although the output voltage is 100mV from the desired value, it appears to be very constant at 3.4V as it deviates in the nV range as time varies. Next, the output voltage across temperature for a load of 75mA was simulated. This can be seen in **Figure 35** below.

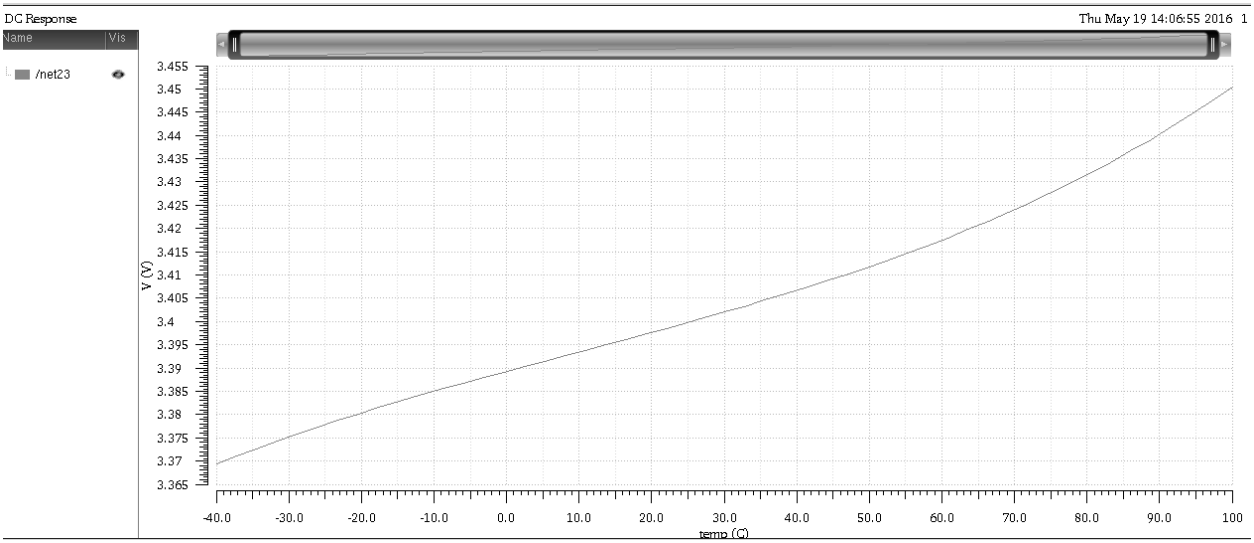


Figure 35: Output Voltage Across Temperature for a Load of 75mA and Temperature 25℃.

As can be seen, the output voltage deviates approximately 85 mV across -40□ to 100□ under these conditions. Next, the output voltage was observed as the load current was swept from 0mA to 150mA, which is the desired current range for this regulator. This can be seen below in **Figure 36**.

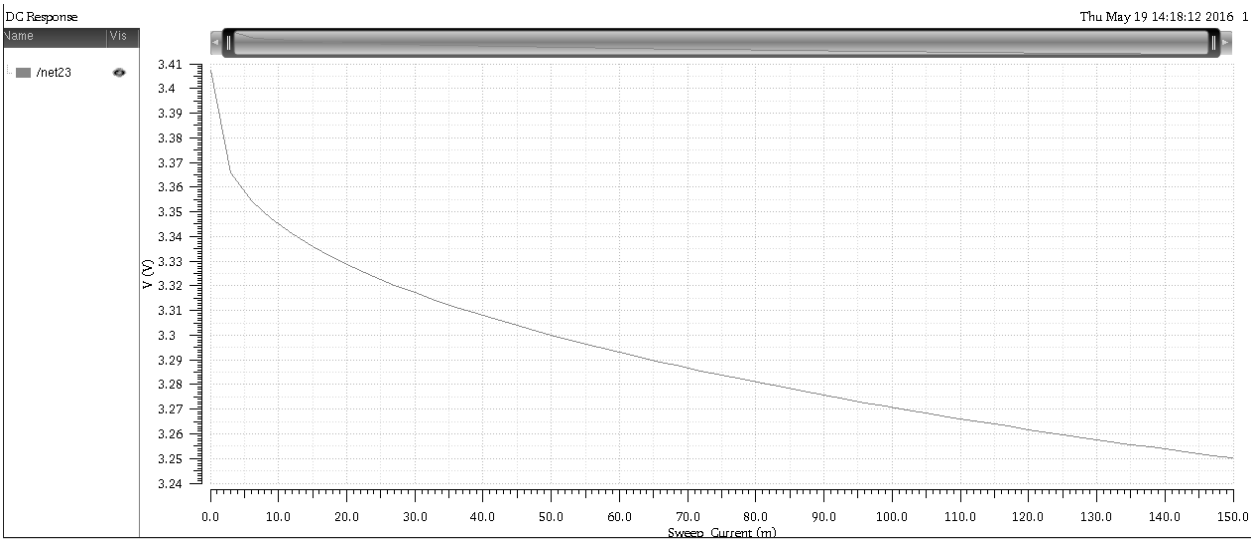


Figure 36: Output Voltage Across Load Current Sweep of 150mA.

As shown, the output voltage deviates approximately 170mV over the desired current range. This is an undesirable result and leaves room for improvement of the project. In addition, the currents in the current mirror were observed. The transient response of the current mirror for a load current of 75mA and temperature of 25□ can be seen in **Figure 37**.

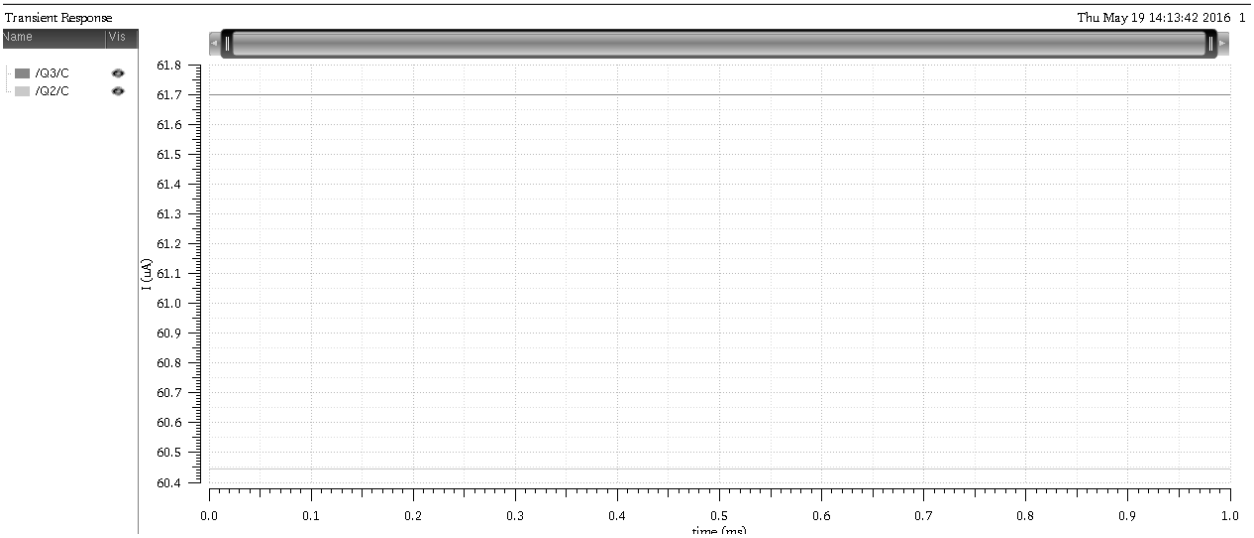


Figure 37: Current Mirror at 75mA Load Current and T=25℃.

As shown, the currents in the current mirror are approximately 61.7uA and 60.45uA, with a deviation of about 2% which is considered to be good values. Next, the currents in the current mirror were observed over temperature. This can be seen below in **Figure 38**.

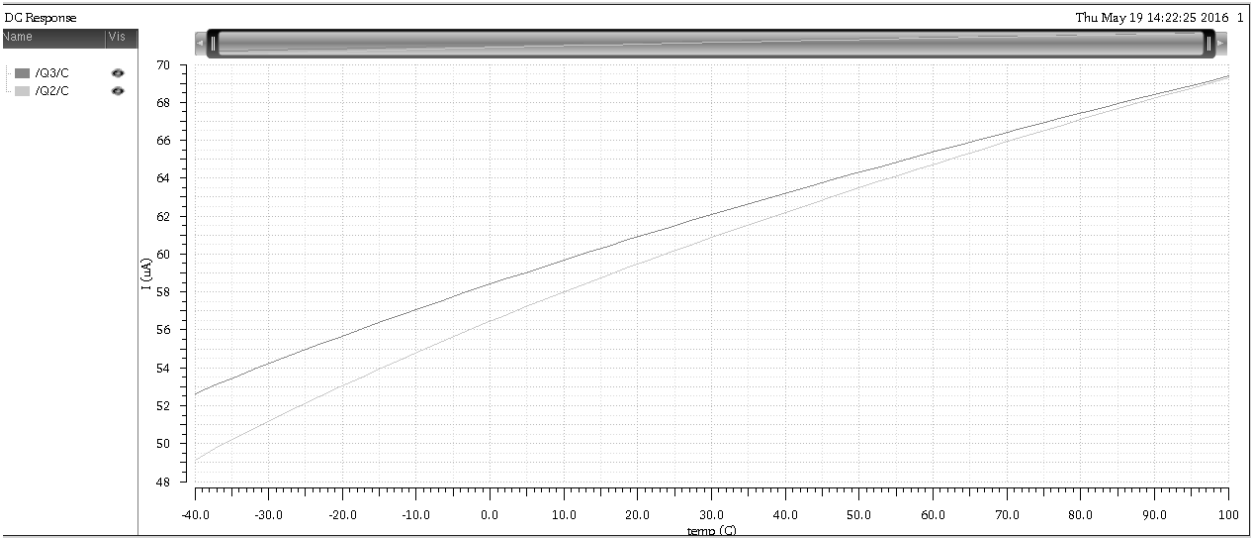


Figure 38: Current Mirror Temperature Sweep.

As can be seen from **Figure 38**, the currents in the current mirror follow each other fairly well across the temperature sweep. Of note is that the max deviation of approximately 3.5uA occurs at -40□ and the least deviation occurs at 125□ where the currents appear to be approximately equal in value. Next, the currents in the current mirror were simulated as the load current was varied from 0mA to 150mA. This can be seen below in **Figure 39**.

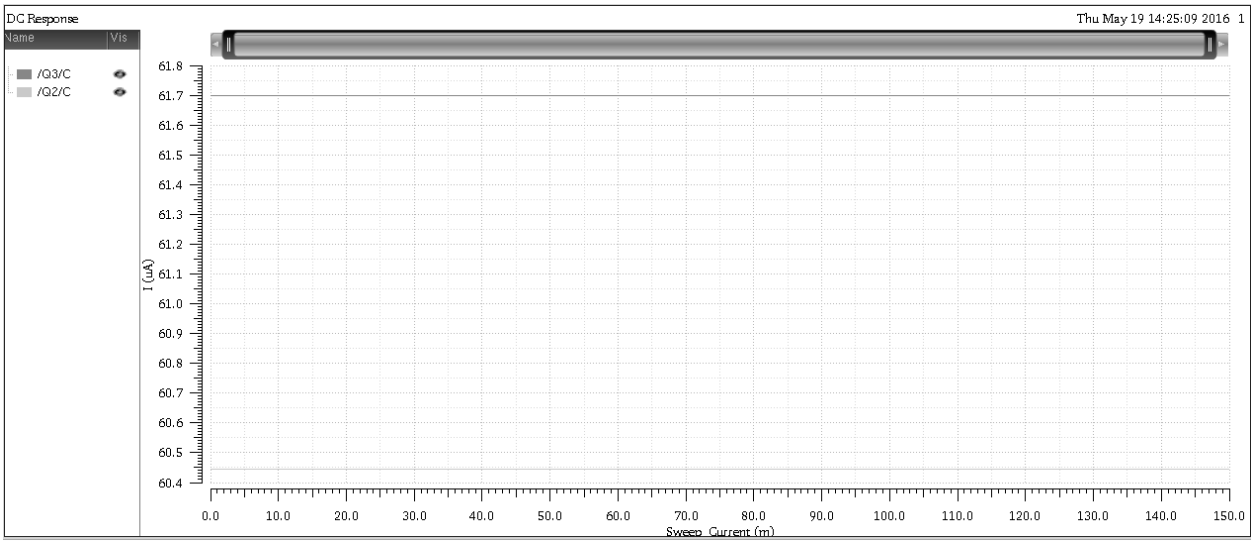


Figure 39: Current Mirror Performance Across Load Current Sweep.

These results are the same as was observed in **Figure 37**. That is, currents in the current mirror are simulated to maintain the same currents of 61.7uA and 60.45uA across the transient response of 1ms and across the load being swept from 0 to 150mA under these conditions. Next, the terminals of the error amplifier were analyzed. The error amplifier transient response was simulated and can be seen below in **Figure 40**.

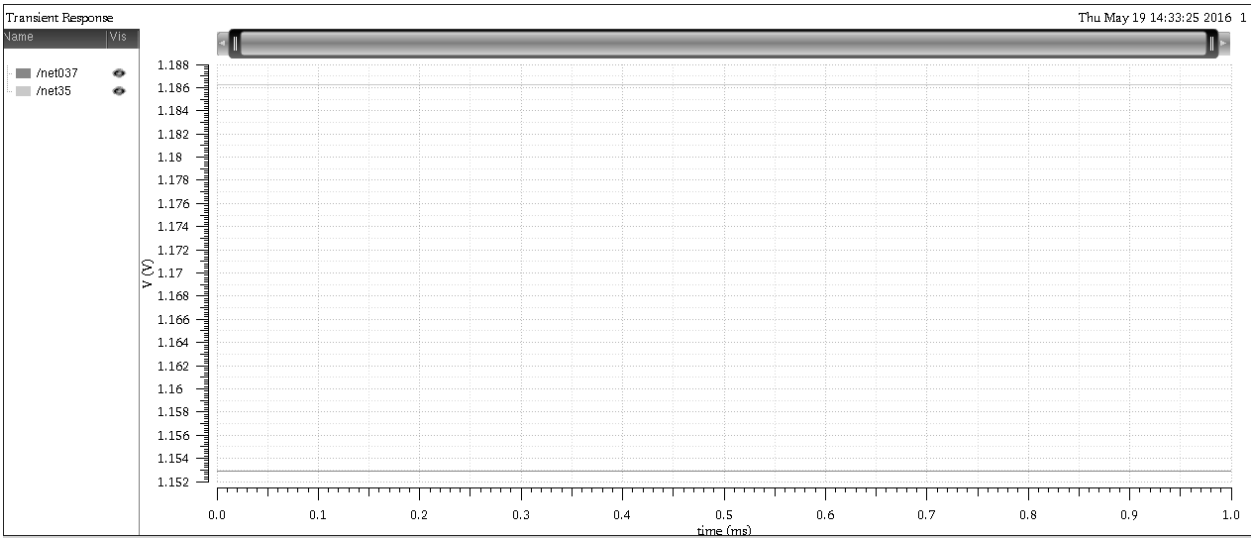


Figure 40: Transient Response of Error Amplifier Terminals

As shown in **Figure 40**, the negative and positive terminals of the error amplifier have a discrepancy of approximately 33 mV over the 1ms transient response. Next, the terminals of the error amplifier were simulated across temperature as shown in **Figure 41**.

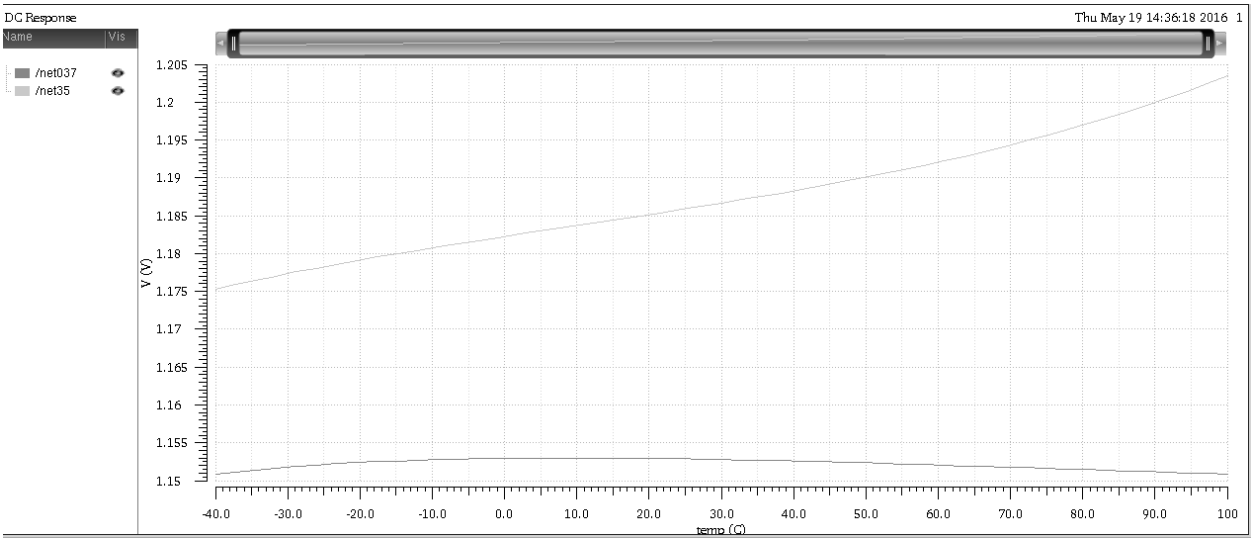


Figure 41: Temperature Sweep of Error Amplifier Terminals

As shown, the voltages at the terminals deviate approximately 25mV at -40□ and approximately 55mV at 100□. Next, the performance of the error amplifier was analyzed as the load was swept as seen in **Figure 42**.

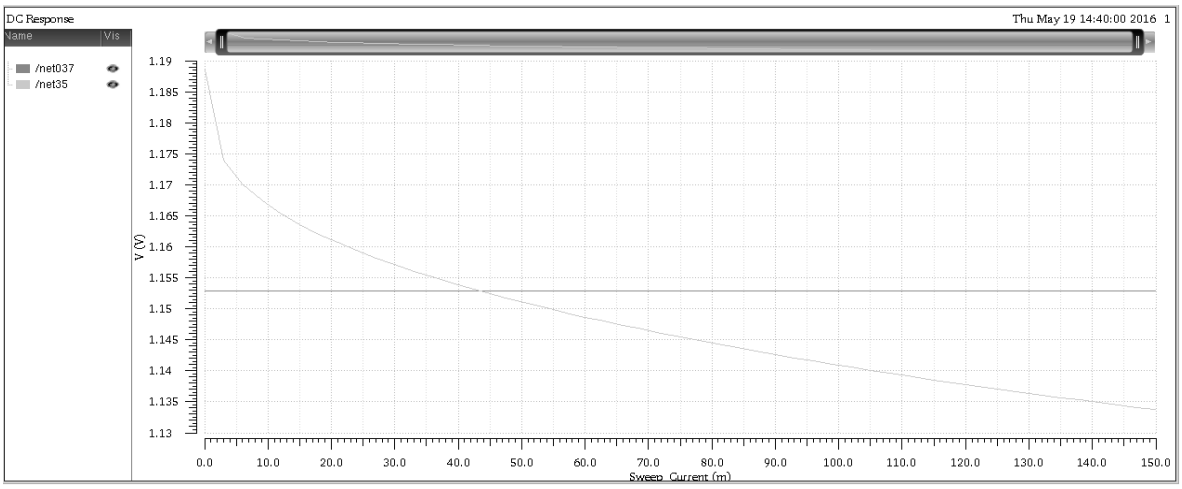


Figure 42: Load Current Sweep of Error Amplifier Terminals

As can be seen the positive terminal of the amplifier, which is connected to the bandgap reference, appears to be stable over the load sweep at approximately 1.153V. The voltage observed at the positive terminal of the amplifier deviates approximately 37 mV at -40□ and approximately 19 mV at 100□, with the best results obtained at a current of approximately 43 mA.

Next, the input voltage supply was swept from 0V to 5V and the output voltage observed. This can be seen below in **Figure 43**.

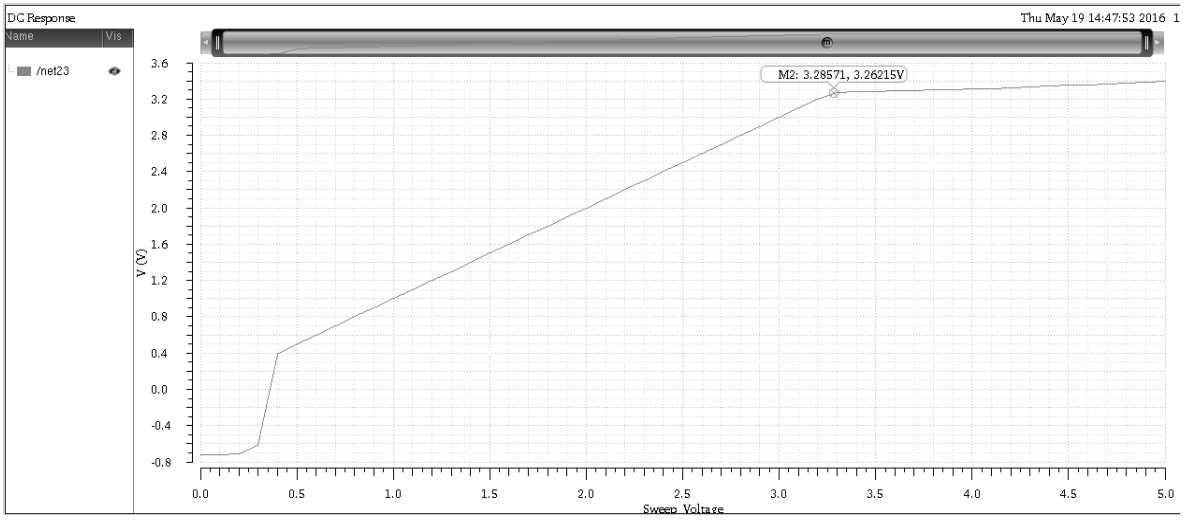


Figure 43: Output Voltage over 5V Supply Voltage Sweep

As seen in **Figure 43**, the output voltage maintains fairly constant until the supply voltage reaches approximately 3.285V, at which point the output voltage begins to drop rapidly. Next, the region where the input voltage was swept from 3.28V to 5V was observed so that the deviation could be better understood. This plot can be seen in **Figure 44**.

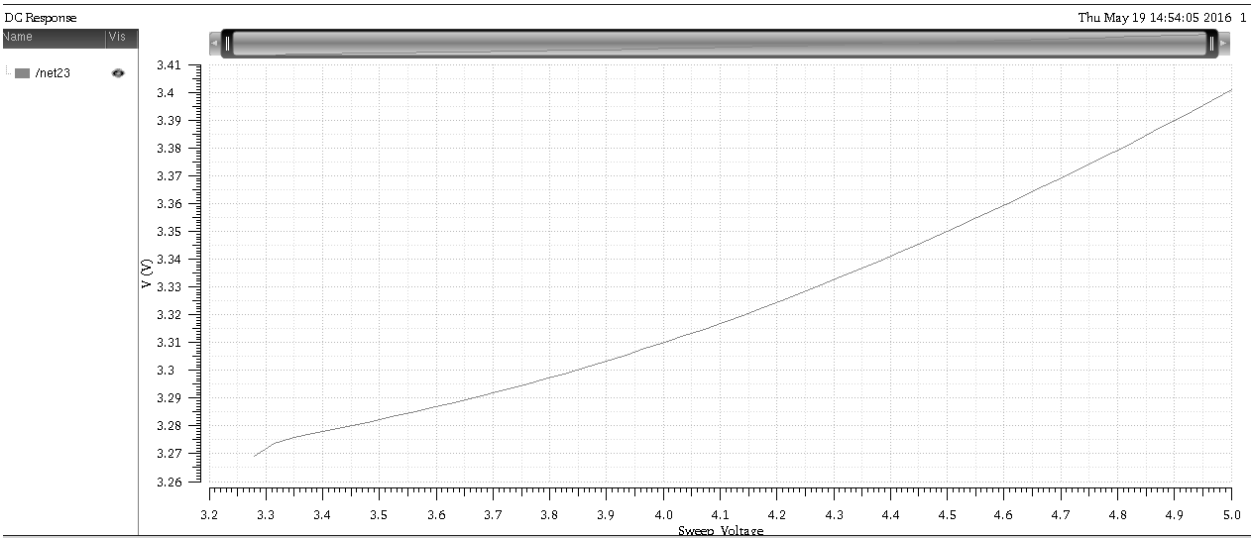


Figure 44: Output Voltage over 5V to 3.28V Supply Voltage Sweep.

As seen, the output voltage deviates approximately 130mV over the supply voltage sweep range of 3.28V to 5V. These are not very desirable results and has room for improvement.

Lastly, the performance of the bandgap reference voltage was analyzed. The bandgap voltage transient response can be seen below in **Figure 45**.

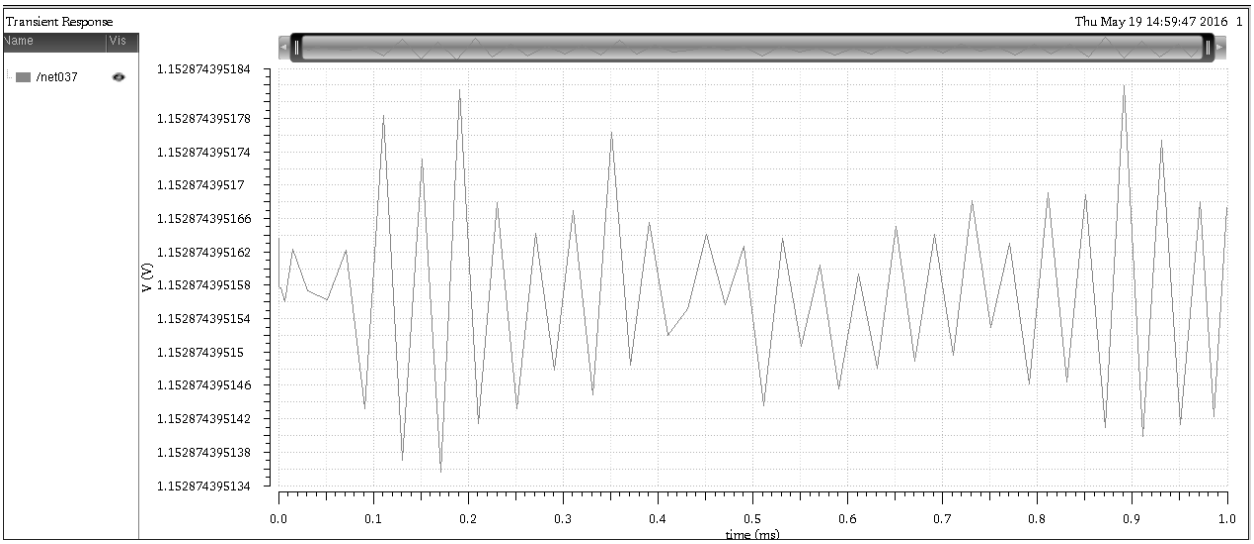


Figure 45: Bandgap Voltage Transient Response

As can be seen, the bandgap voltage varies in the pV range across the 1ms transient response, which is a desirable result. Next, the bandgap voltage was observed as the temperature was swept. This simulation can be seen below in **Figure 46**.

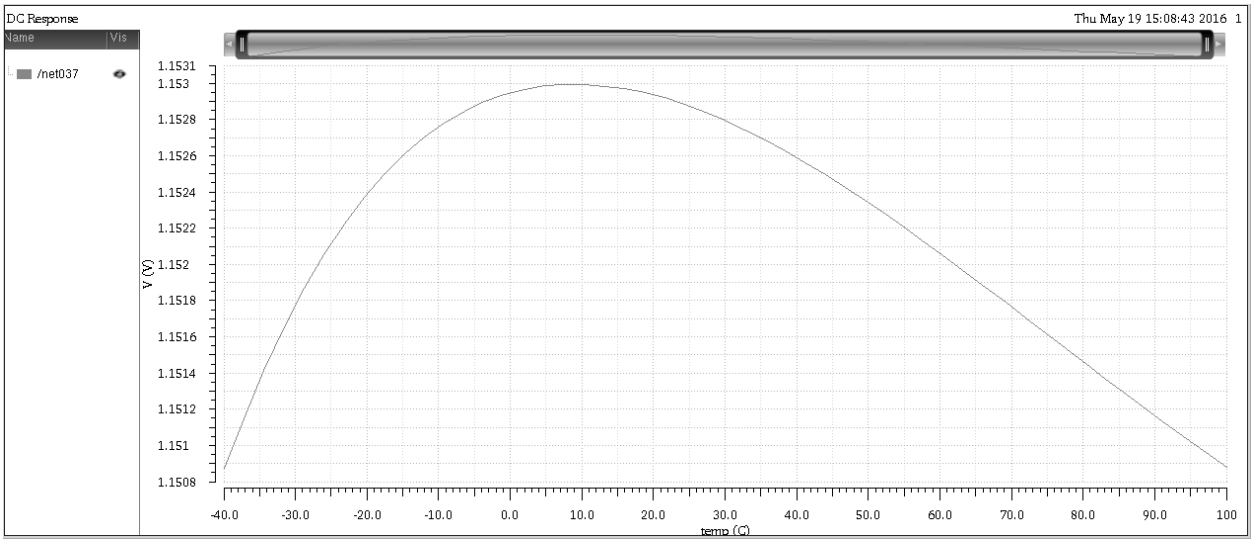


Figure 46: Bandgap Voltage Across Temperature Sweep.

As can be seen the bandgap voltage deviates by approximately 2.2mV over temperature, as desired. Next, the bandgap voltage was simulated as the load current was swept. This simulation can be seen in **Figure 47** below.

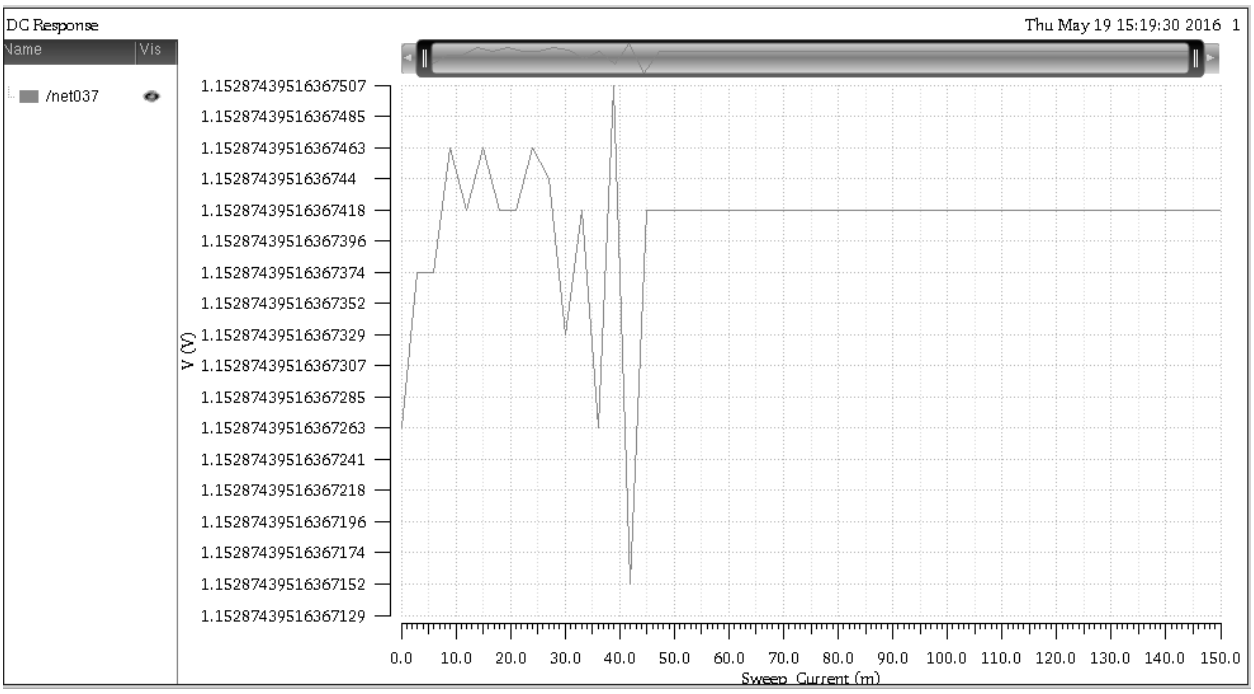


Figure 47: Bandgap Voltage Across Load Current Sweep

As shown, the output voltage deviates in the fV range over the current sweep of 0mA to 150mA, which is a great result.

Layout & Routing

Layout was performed in sections of the overall project. The group decided to begin layout with the power transistor. Therefore, layout and routing of 10 VPNP pfet Pcells was performed using Cadence Layout XL. The intention of this was to layout and route 10 transistors and then to create a symbol for this combination of transistors. This symbol would then be cascaded eight times so that the power transistor, consisting of eighty transistors in parallel, could be emulated. The schematic of ten transistors in parallel can be seen below in **Figure 48** and the corresponding layout can be seen in **Figure 49**.

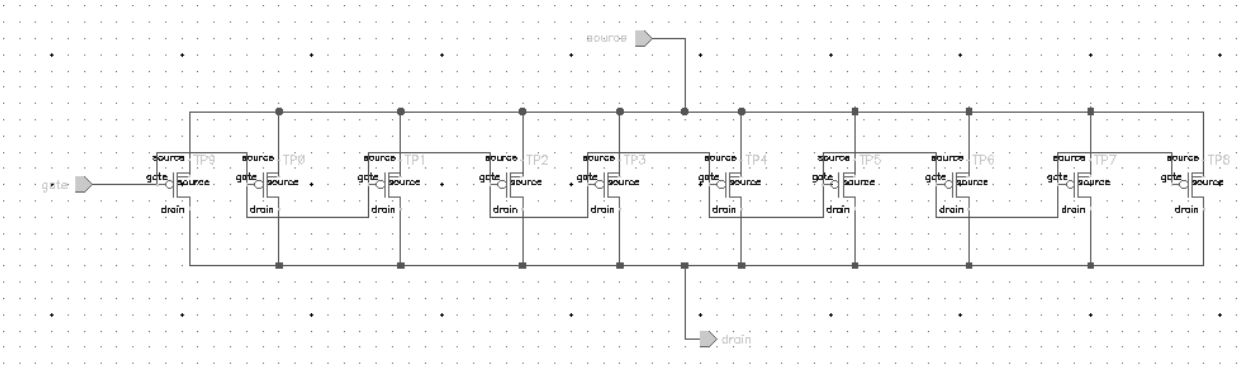


Figure 48: Ten Transistor Schematic for Power Transistor.

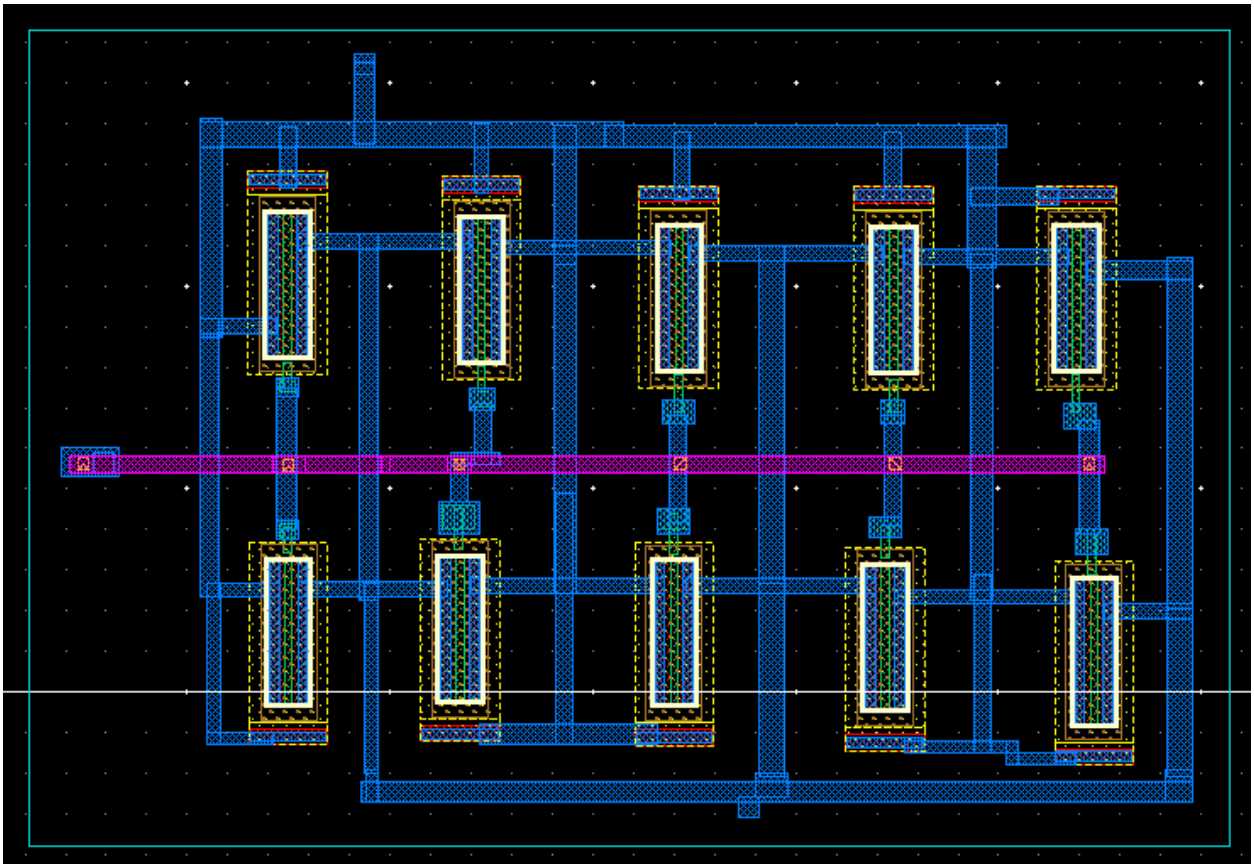


Figure 49: Ten Transistor Layout for Power Transistor.

Metal layer 1 is represented in blue above and metal layer 2 is represented in purple above. As shown in **Figure 49**, the drains and sources of the mosfets are connected using metal layer 1. Contacts were added to the polysilicon of the gates and then gate connections were made using metal layer 1, metal layer 2, and vias. Metal layer 2 and vias were utilized to avoid unwanted overlap of metal layer 1. Furthermore, this layout was able to pass both DRC and LVS.
Next, layout of the rest of the error amplifier circuitry was performed. First, the schematic was created which consisted of the error amplifier circuitry except for the power transistor. This schematic can be seen below in **Figure 50**.

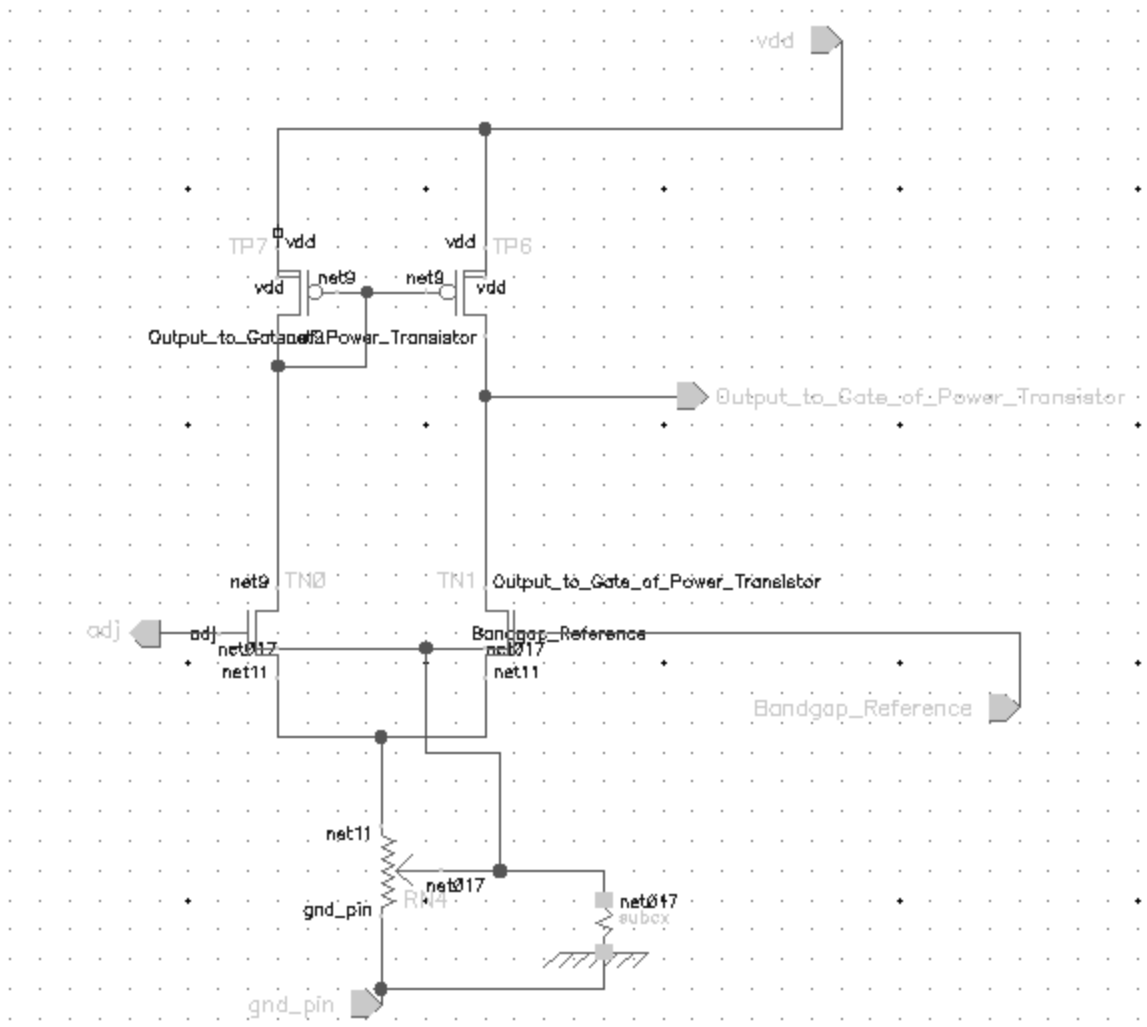


Figure 50: Error Amplifier Schematic Without Power Transistor.

Using the same methodology as mentioned above, this schematic was dropped into Layout XL where layout and routing was performed. The layout of the schematic in **Figure 50** can be seen below in **Figure 51**.

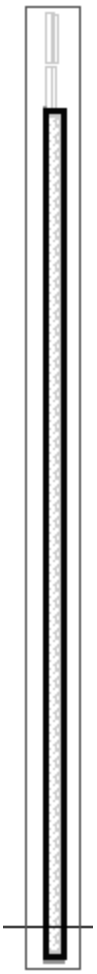


Figure 51: Error Amplifier Layout Without the Power Transistor

The resistor used in the error amplifier circuitry is quite large in comparison to the mosfets, as can be seen in **Figure 51**. With that said, a zoomed in view of the mosfets on top of the resistor in **Figure 51** can be seen in **Figure 52**.

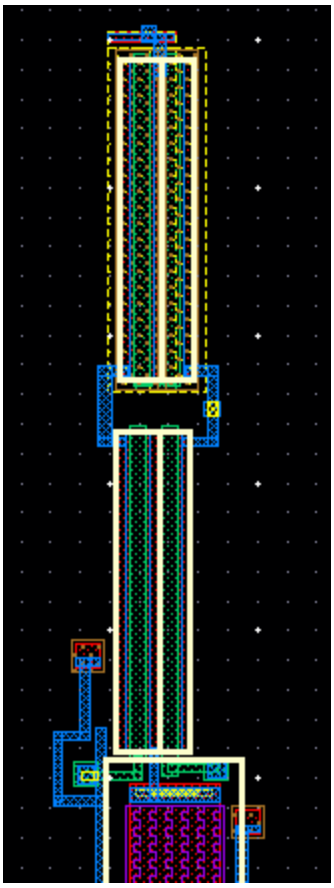


Figure 52: Layout of Mosfets Used in Error Amplifier (Excluding Power Transistor)

Furthermore, the connections at the bottom of the resistor can be seen in **Figure 53**.

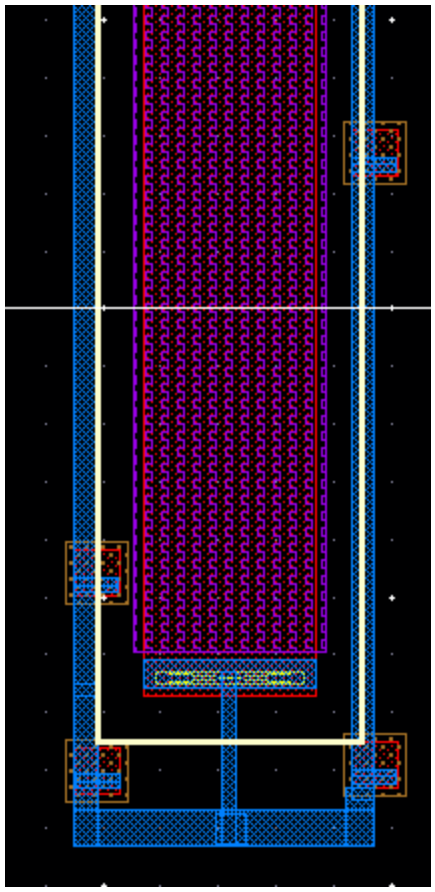


Figure 53: Layout Bottom Connection of Resistor Used in Error Amplifier.

It is believed that Pcells called SUBCX had to be utilized in order to connect the substrate of the resistor to the most negative potential, which is ground in this case. Therefore, multiple SUBCX Pcell components were dropped into layout in an attempt to connect the substrate of the resistor to ground. In the end, this schematic passed DRC but was not able to pass LVS. The reason for this was due to an error which stated that the substrate of the resistor was unbounded. Therefore, the group is unsure if these Pcells being added to the layout had much of an effect in the end since it appears that their intended goal of grounding the substrate was not accomplished.

Next, layout of all five of the mosfets that are utilized in the current mirror circuitry was accomplished. This began with creating the schematic for these transistors, which can be seen below in **Figure 54**.

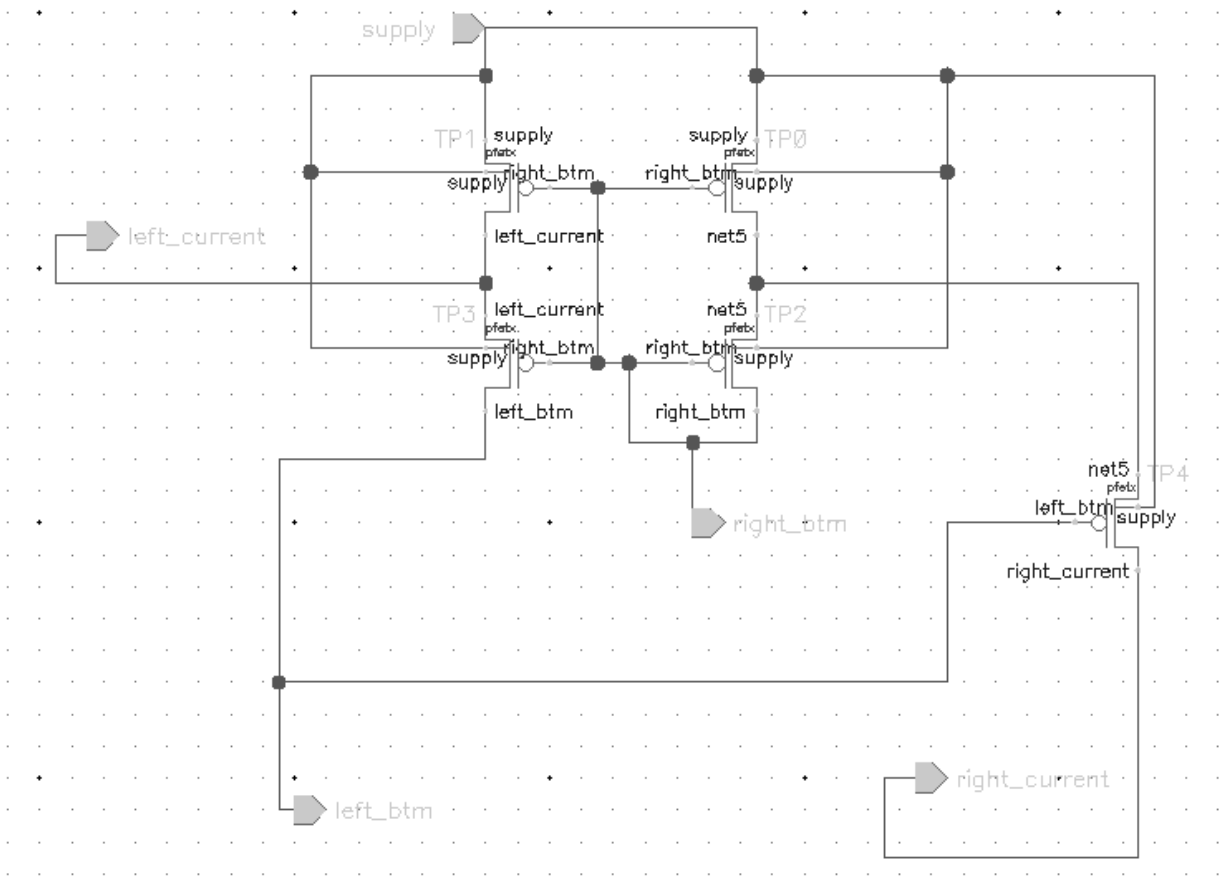


Figure 54: Error Amplifier Circuitry Without the Resistor.

From this schematic, as performed previously, Layout XL was entered and then layout and routing of the transistors in **Figure 54** was performed. This layout can be seen below in **Figure 55**.

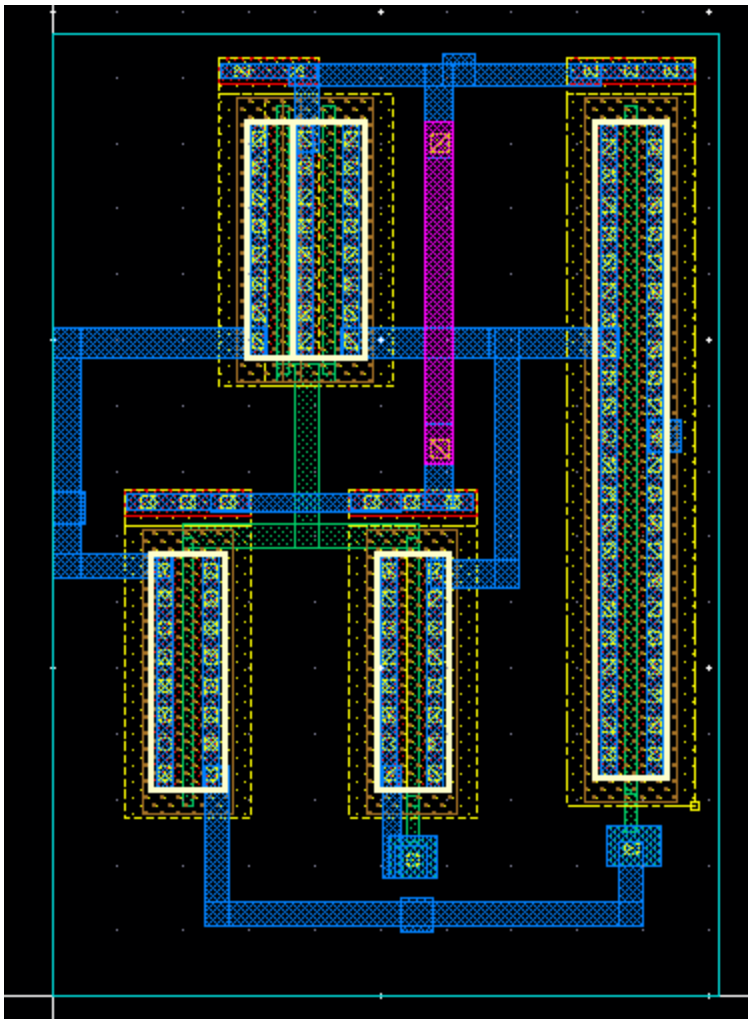


Figure 55: Layout of Current Mirror Without Bottom BJTs and Resistors.

Of note is that the source terminals of the pfet transistors were able to be overlapped, as can be seen in **Figure 55**. However, this was found to be difficult when using the nfet transistors since one of the source terminals, when overlapped with another nfet source terminal, would be automatically changed in the layout to a drain terminal. Although it would not affect the behavior of the circuit to have the drain terminal act as a source terminal since these transistors are symmetric devices, the group decided to route the nfet transistors without overlapping the sources. This was performed in an attempt to avoid LVS errors since the drain would be connected to the source, and not the source connected to source.

Next, layout and routing of the BJTs in the bandgap circuitry was performed using the same method as described earlier. The BJTs were designed to consist of 4 transistors in parallel on the diode connected side and 32 transistors in parallel on the other side. Of note is that to connect the transistors in parallel, the bases were tied together, the collectors tied together, and the emitters tied together. An example of this schematic can be seen in **Figure 56**.

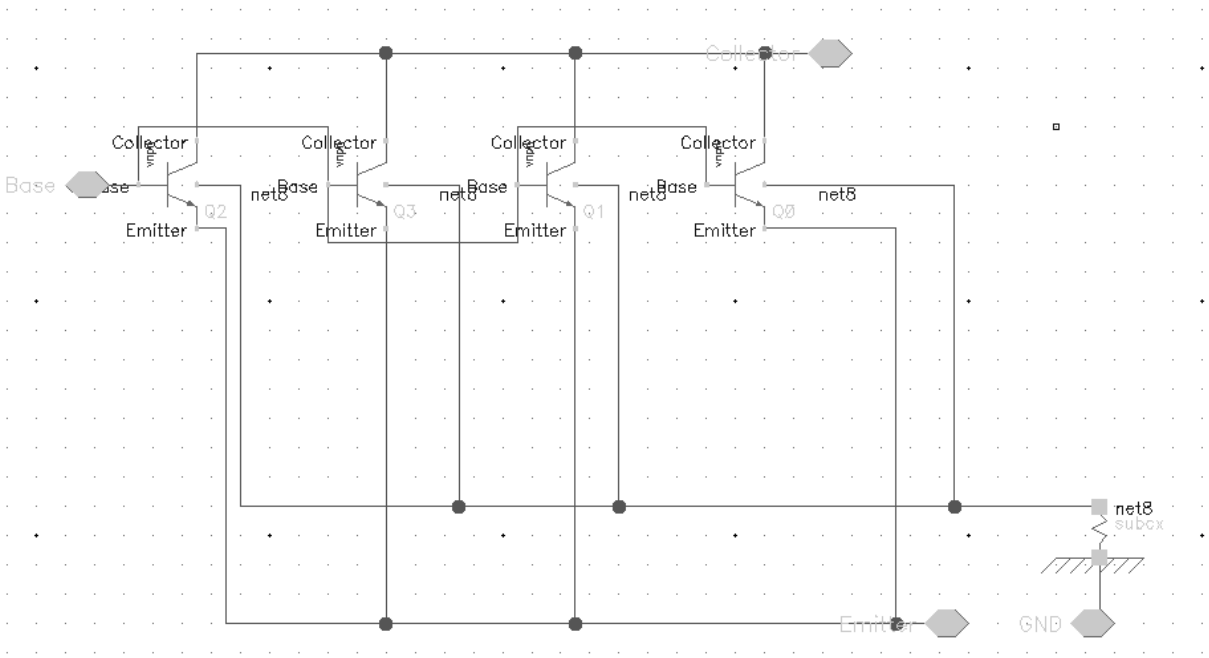


Figure 56: Four BJTs in Parallel

The layout of the four transistors can be seen in **Figure 57**.

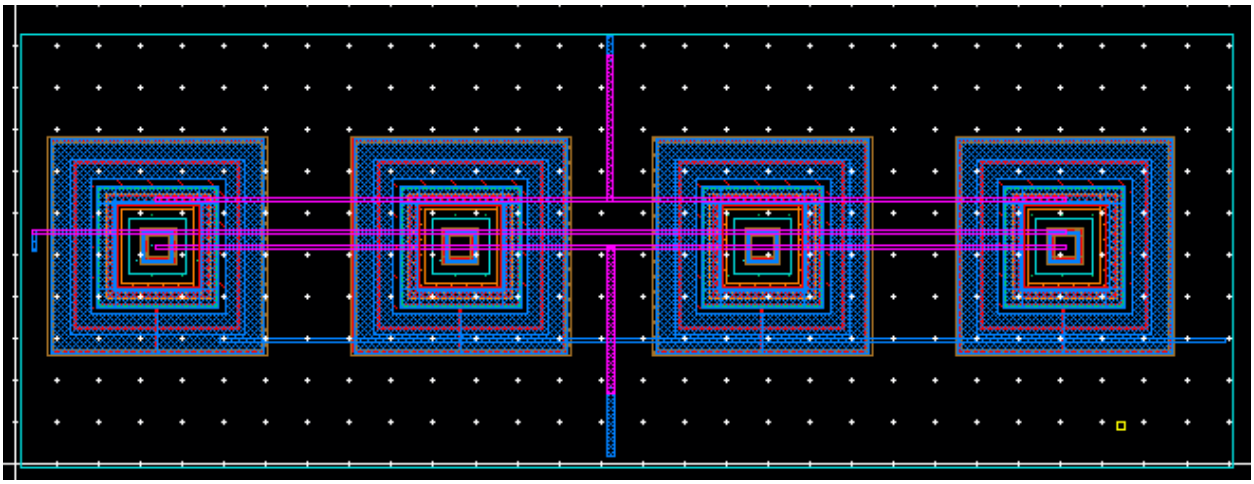


Figure 57: Layout of Four BJTs in Parallel

From **Figure 57**, it is seen that the layout for a BJT is much different than that of a MOSFET. The way the BJT is represented in layout is with concentric squares. The emitter is the smallest and in the middle, the collector is around that, and the base around that. The substrate of the device is the outer ring. In order to connect the correct terminals together, for example the base of one transistor to the base of another transistor, a metal 2 layer had to be used. To connect metal 1 and metal 2 together, a V1 (via) connector had to be used and placed where the two metals overlapped, as seen in **Figure 58.**

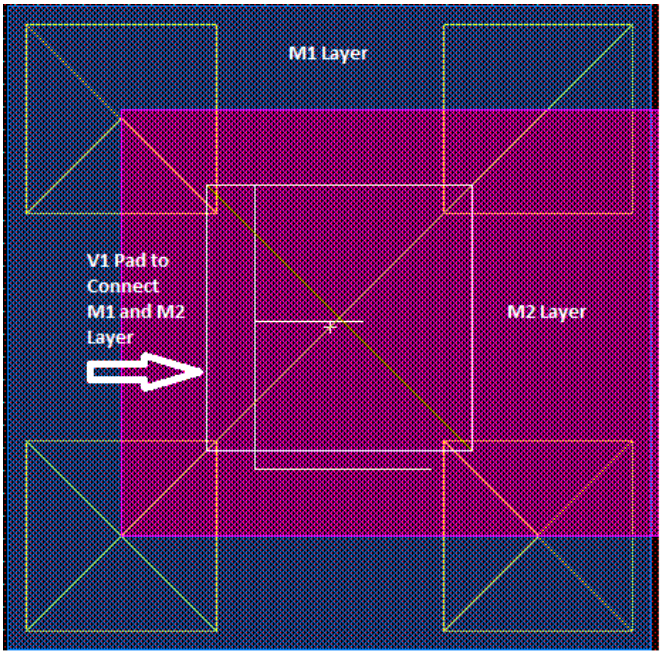


Figure 58: Connecting M1 and M2 Layer with a Via

Upon completion of laying out the four BJTs, layout and routing of the biasing circuitry for the Prodanov current mirror was performed in Cadence. The schematic of this circuit can been seen in **Figure 59**, below.

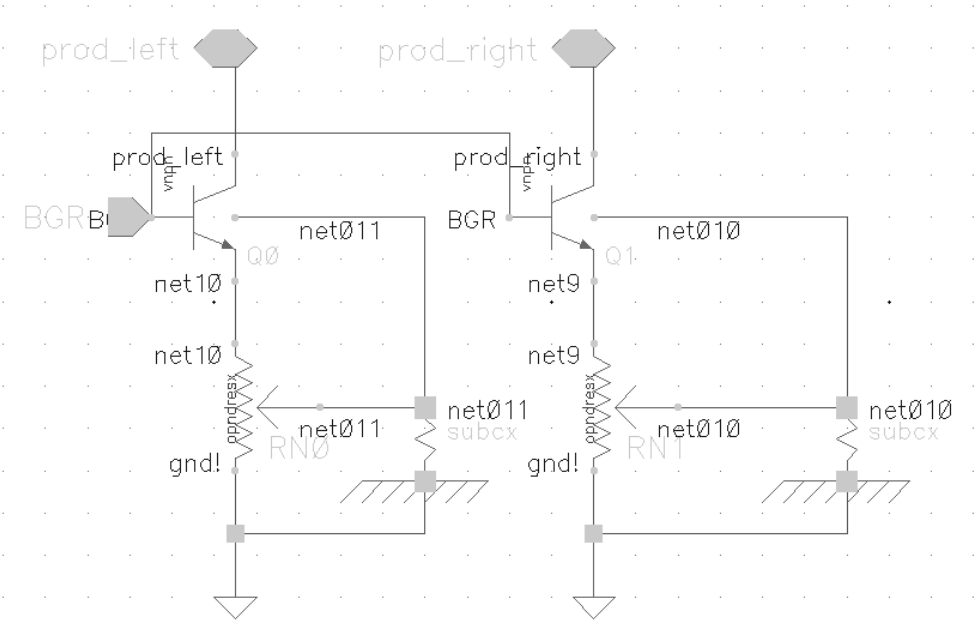


Figure 59: Biasing Circuitry of Prodanov Current Mirror

The difficult part of this section of the system was the resistors that were used for this process. As can be seen in the schematic above, the resistors have a substrate pin, and it was discovered that the substrate terminal of the resistor has to be connected to ground through a Subcx block. The layout of this biasing circuitry can be seen in **Figure 60.**

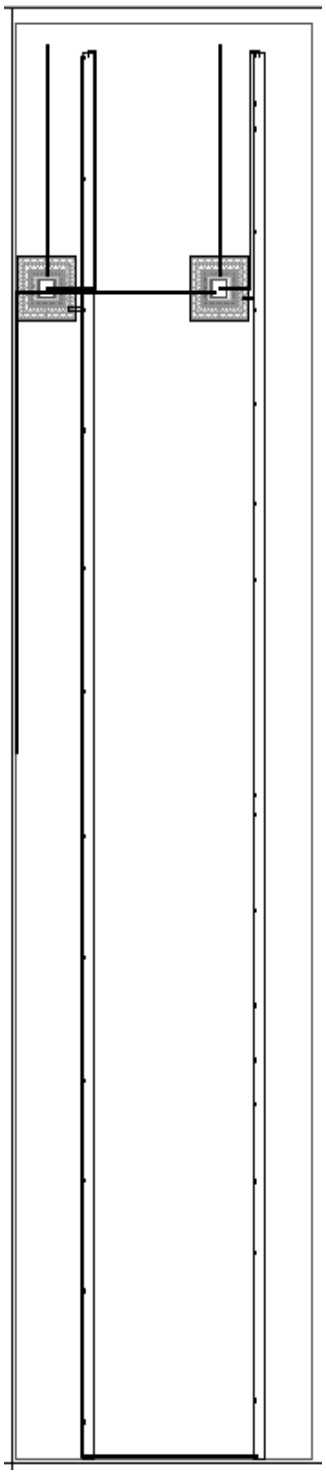


Figure 60: Layout of Biasing Circuitry with Two BJTs and Two Resistors

However, the layout of the biasing circuit does not have an explicit part of the resistor that is labeled as the substrate. Thus, it was later discovered that Subcx blocks should be placed along the edges of the resistor component in the layout window. Subcx blocks should be placed between the RX and boundary of the resistor and have a strip of layer M1 to connect the Subcx to ground; as seen in **Figure 61.**

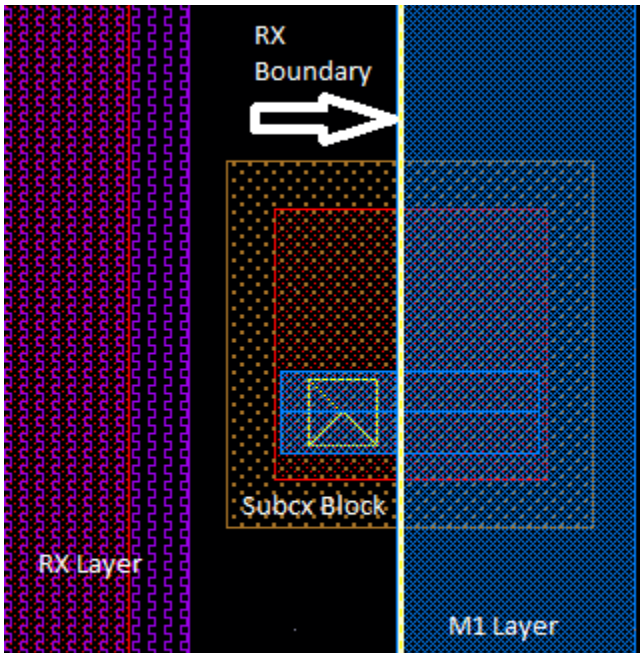


Figure 61: Subcx Block Along Resistor with M1 Layer

As mentioned previously, the addition of the Subcx Pcells tied from the substrate of the resistor to ground was intended to fix an LVS error stating that the resistor had an unbound substrate. However, this LVS error was unable to be corrected for by adding the Subcx blocks and therefore it is not understood if these blocks were truly needed.

DRC

Although the design of the system is complete, it does not necessarily mean the circuit or system will be able to be fabricated on the chip. When doing analog chip design, there are a series of checks the designer should do to ensure the design can be fabricated on the chip; this is commonly known as Design Rule Check (DRC). DRC is unique to each specific semiconductor manufacturing process, thus there are no rules that will work for all processes. Completing DRC enables the designer to verify if their design in layout satisfies the requirements for the semiconductor manufacturing process used to fabricate the chip.

With this in mind, the group found it easier and more helpful to run DRC for each sub block of the circuit. Also, since members did not have a lot of experience with Cadence, it was helpful to run DRC after every change made. That way if a new error occurred, the group was able to isolate the problem to fix it. Another helpful tip the group found while going through DRC is in the Error Layer Window (ELW). The right arrow in this window, circled in red in **Figure 62**, will redirect or zoom into the component under question in the layout view. This was found to be very helpful to the group when there were multiple BJT's or MOSFETs in the layout. Without this feature, DRC debugging would have required more time to fix the errors.

Figure 62: Tools to Isolate and Fix DRC Errors

Of note is that the lines starting with # in the ELW represent warnings and can be ignored. While going through DRC, the group came across some issues that were new to them. However, through extensive research on the internet and help from Cadence design help forums, most of the issues were resolved. Nonetheless, there was one error that the group could not resolve and that was the DRC error associated with using BJT's. From the DRC window, it was inferred that each BJT creates [4] data audit errors. An example of this can be seen in the DRC window shown in **Figure 63**.

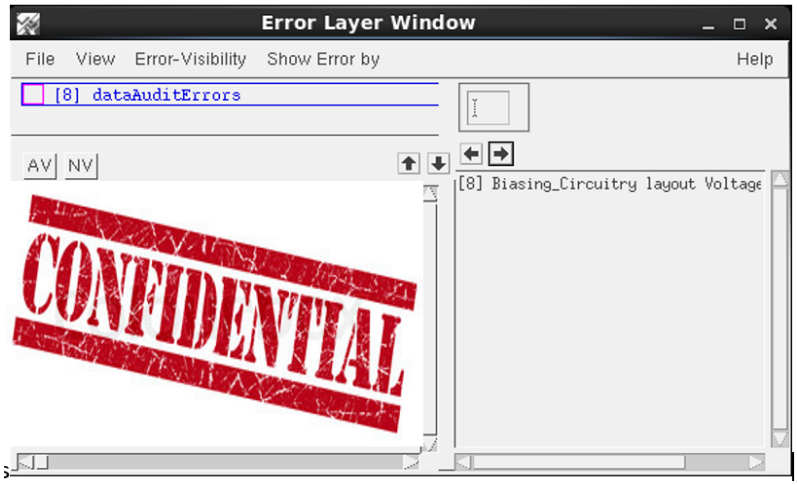


Figure 63: dataAuditErrors When Using BJTs

An additional DRC error was encountered when performing the layout of the error amplifier. That is, upon laying out the pfet devices a DRC error occurred which stated "GR268: RX(in BP) to RX(not BP) (in same NW) space<=XX.00um."

This DRC error was corrected by clicking SHIFT+Q on the pfet transistors and then going to the "Parameters" tab and clicking on "Well ring." A screenshot of the window which appears after SHIFT+Q has been clicked on the highlighted pfet can be seen in **Figure 64** below with the Parameters tab clicked and NWell box checked.

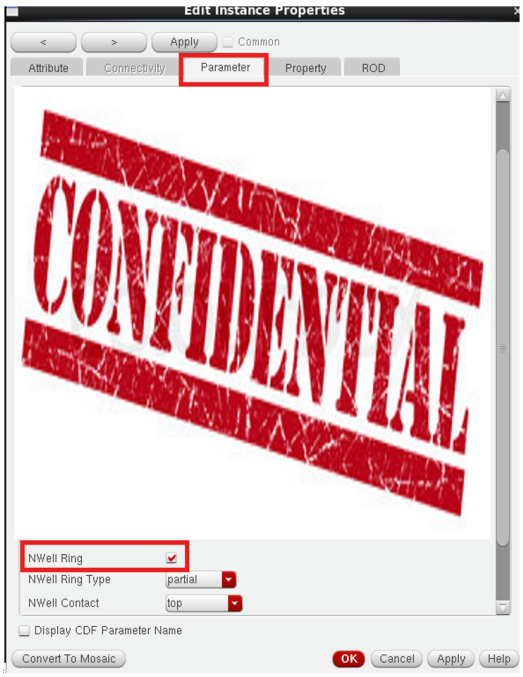


Figure 64: Edit Instances Properties Window

This allowed for NWell rings to be added to the transistors. A picture of a transistor in layout with the NWell rings and without the Nwell rings can be seen below in **Figure 65**.

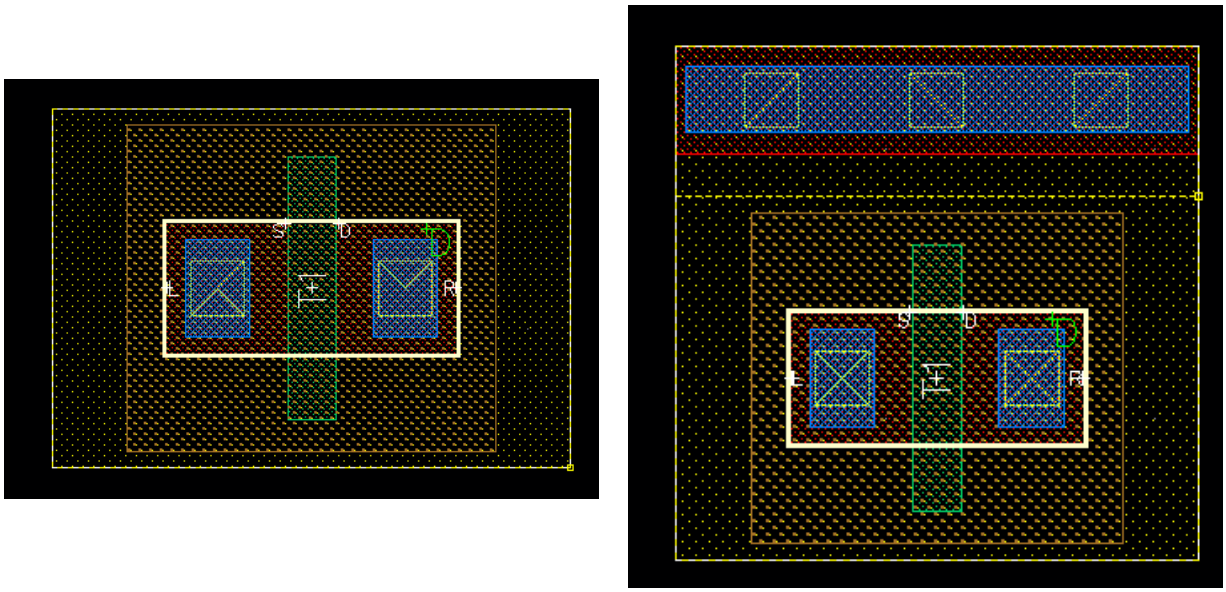


Figure 65: PFET Without NWell Ring (Left) & PFET With NWell Ring (Right)

In summary, several DRC errors were encountered throughout this project and all of them were able to be corrected except for the BJT "Audit Data Errors." The group does not currently understand the reason as to why this error is occuring.

LVS

After completing DRC, the design still needs to go through another design check known as Layout Versus Schematic (LVS). Going through LVS ensures that the layout of the chip truly matches the design as shown in the schematic view.

The Nets Mismatch Tool allows the designer to zoom into the layout and see which connection in layout does not match. However, while going through LVS, the group found that the software was not very helpful in pin pointing what was different between the schematic and layout. That is, difficulties were encountered as the tool is not very descriptive of what exactly is mismatched at the zoomed in location. An example of the Nets Mismatch Tool after performing LVS can be seen below in **Figure 66**.

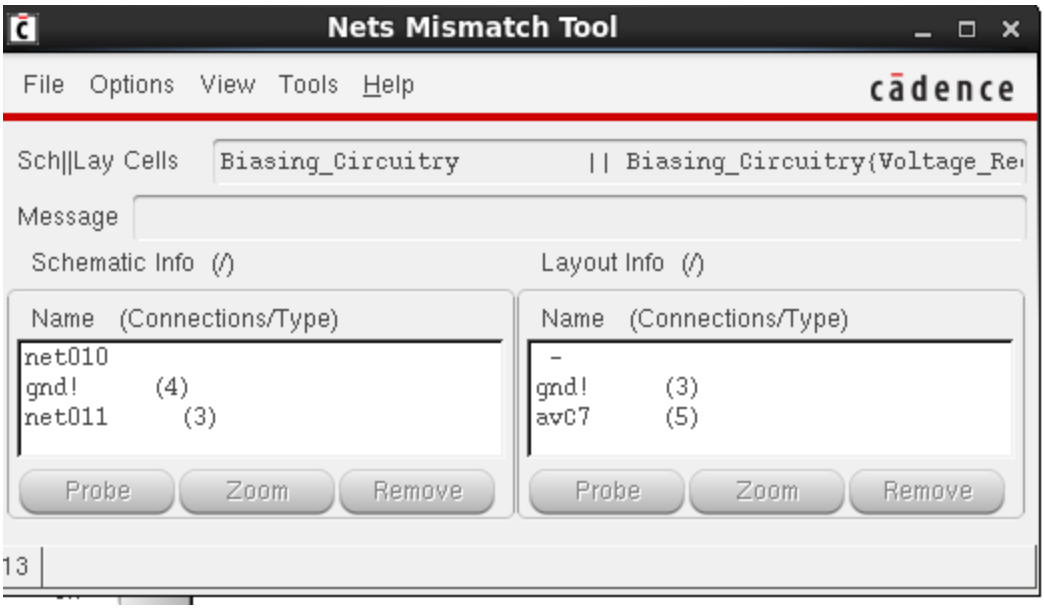


Figure 66: Nets Mismatch Tool to Fix LVS Errors

Utilization of the Nets Mismatch Tool is performed by clicking the "zoom" button seen in **Figure 66**. However, if the "zoom" button on the left of the window is pressed, the software will not zoom to the net that is mismatched in the schematic window automatically. Instead, the user has to make sure that the schematic window is the current working window before pressing the button; caution, the "zoom" button does not always work.

One issue that the group came across when running LVS with BJT's in the design is that the emitter of the VNPN needs to be connected to a subcx block before it is attached to ground. Otherwise, the software will produce an error and the chip cannot be fabricated. To do this, a subcx block needs to be added to the schematic and layout; this can be found under "Create Instance" => Library: "cmhv7sf" => cell: "subcx". In the schematic, the subcx block should be connected to the emitter of the VNPN Pcell and to ground, as shown in **Figure 67** (boxed in red).

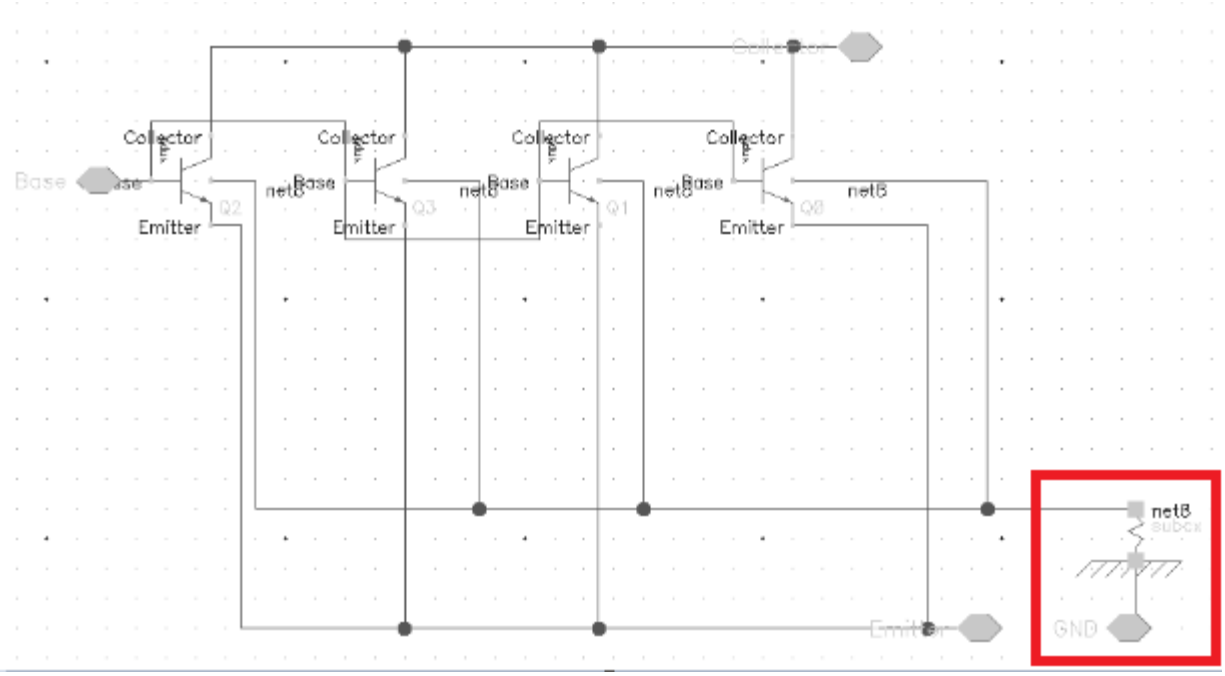


Figure 67: Layout of Four BJTs in Parallel with Subcx Component

The connection of the subcx block in the layout view is shown in **Figure 68.**

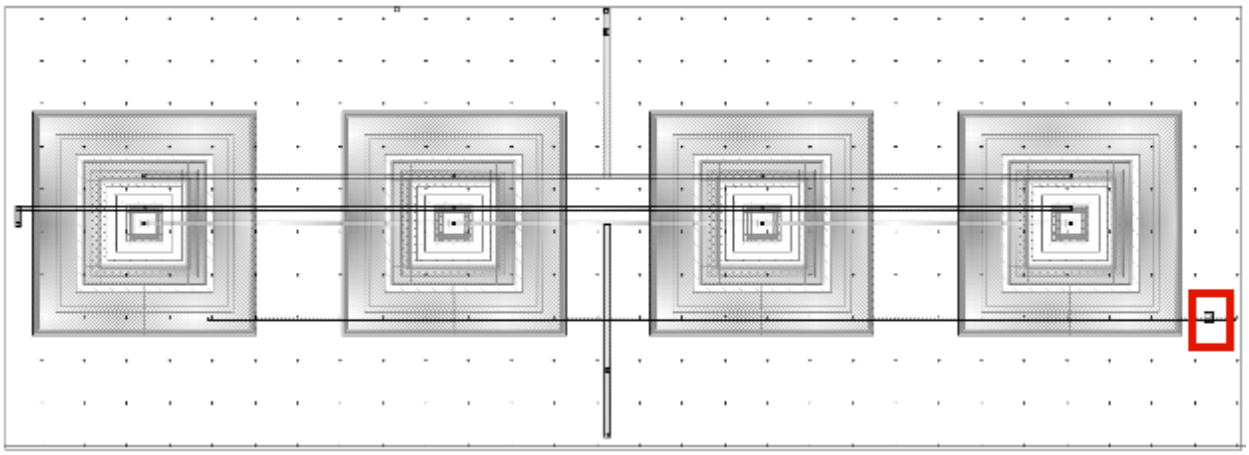


Figure 68: Layout of Four BJTs in Parallel with Subcx Block

The subcx block in layout should be attached to the outer ring of the VNPN, since this was found to be connected to the substrate of the transistor.

Furthermore, the group had difficulty connecting the substrate of the resistor component "opndresx" to ground. It was assumed that the area immediately outside the boundary of the layout of the resistor was the substrate of the resistor. Moreover, it was assumed that subcx blocks should be added along the length of the resistor so as to make connections with the substrate and then connected to ground. However, an LVS error stating "Device 'subc(RES)' on

layout is unbound to any schematic device" was encountered and unable to be resolved by this approach. The log file with the abovementioned error is shown in **Figure 69**.

```
*ERROR* Device 'subc(RES)' on Layout is unbound to any Schematic device.
*ERROR* UnBound devices found.
Info: All devices must be bound or filtered for comparison to be run.
Exiting nvn.
```

Figure 69: LVS Log File for Error Amplifier Layout

Next Steps

The next steps of this design would be to fix the DRC and LVS errors that are mentioned in the LVS and DRC sections. This includes being able to connect the substrate of the opndresx resistors to ground and finding how to get rid of the data audit errors of the BJTs. Once these errors have been fixed, the next step would be to connect the sub-circuits and then add I/O pads. By adding the I/O pads, the chip will be allowed to be probed and connections made to the device once it has been fabricated.

After adding the IO pads, extraction would be performed on the design. Extraction allows the designer to see if there are any capacitive and/or inductive effects between components which will make the circuit perform non-ideally. Once extraction is done, the GSDII file can finally be created and sent to the fabrication site for fabrication of the chip. Once the chip is returned, the chip will be tested.

In addition, the design could be further optimized. It was found that the output voltage deviates approximately 170mV over the current range sweep of 0mA to 150mA. It was also found that the output voltage deviates approximately 130mV over the supply voltage sweep range of 3.28V to 5V. These are two possible areas of the design that could be optimized. In addition, more optimal layouts and routing of the devices in this design could be performed.

Conclusion

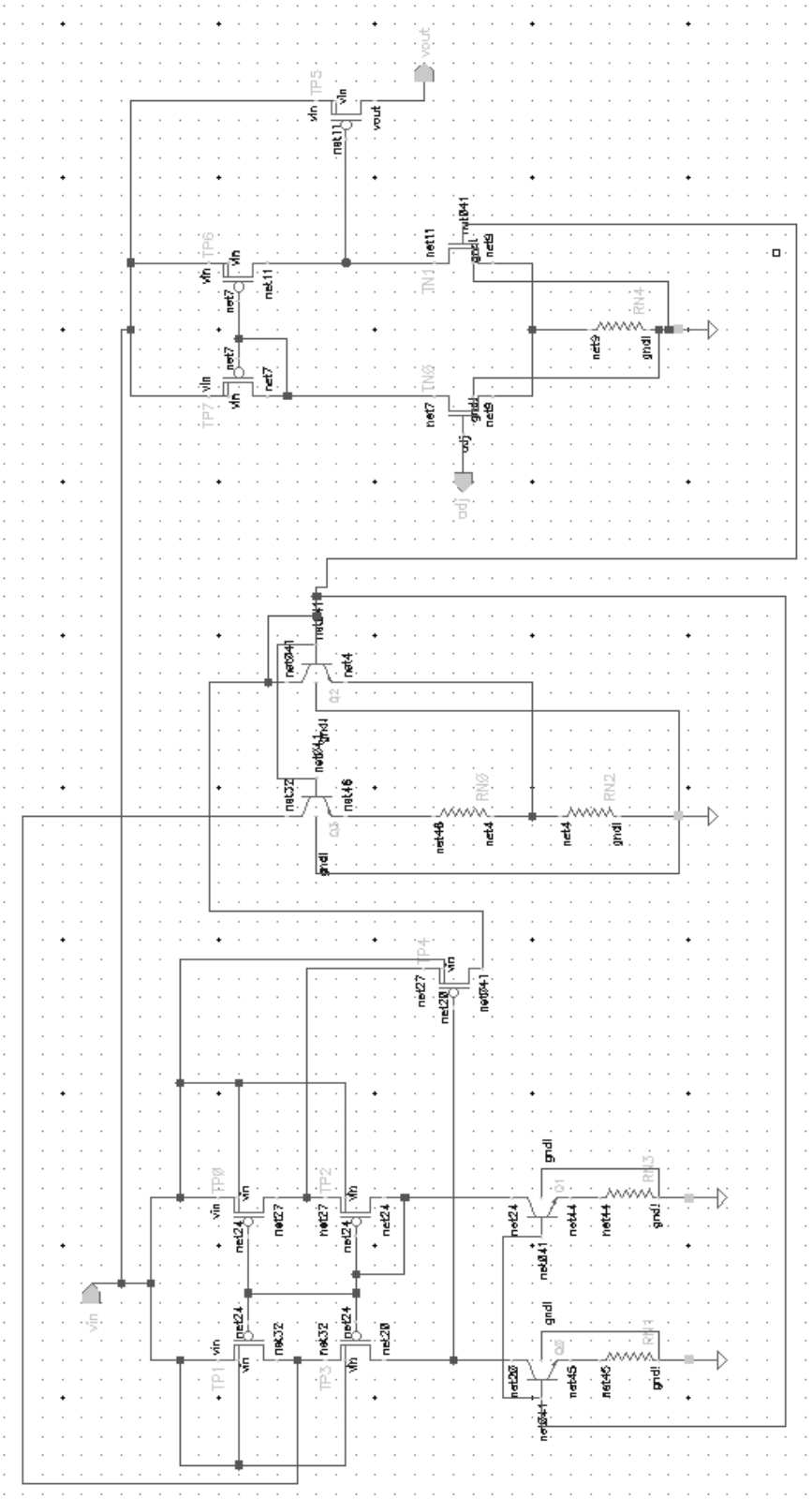
This project allowed the group to design a linear voltage regulator through the use of Cadence VLSI software. The specifications designed for were as follows: input voltage range of 5V +/- 1V, load current capabilities of 150mA, and output voltage range of 1.15V to 3.3V. The design aspect consisted of the design of a bandgap reference voltage circuit, current mirror, error amplifier, and power transistor.

The layout was broken into sub-circuits of the final design and layout of these sub-circuits was performed individually using Layout XL. Several DRC and LVS errors were encountered

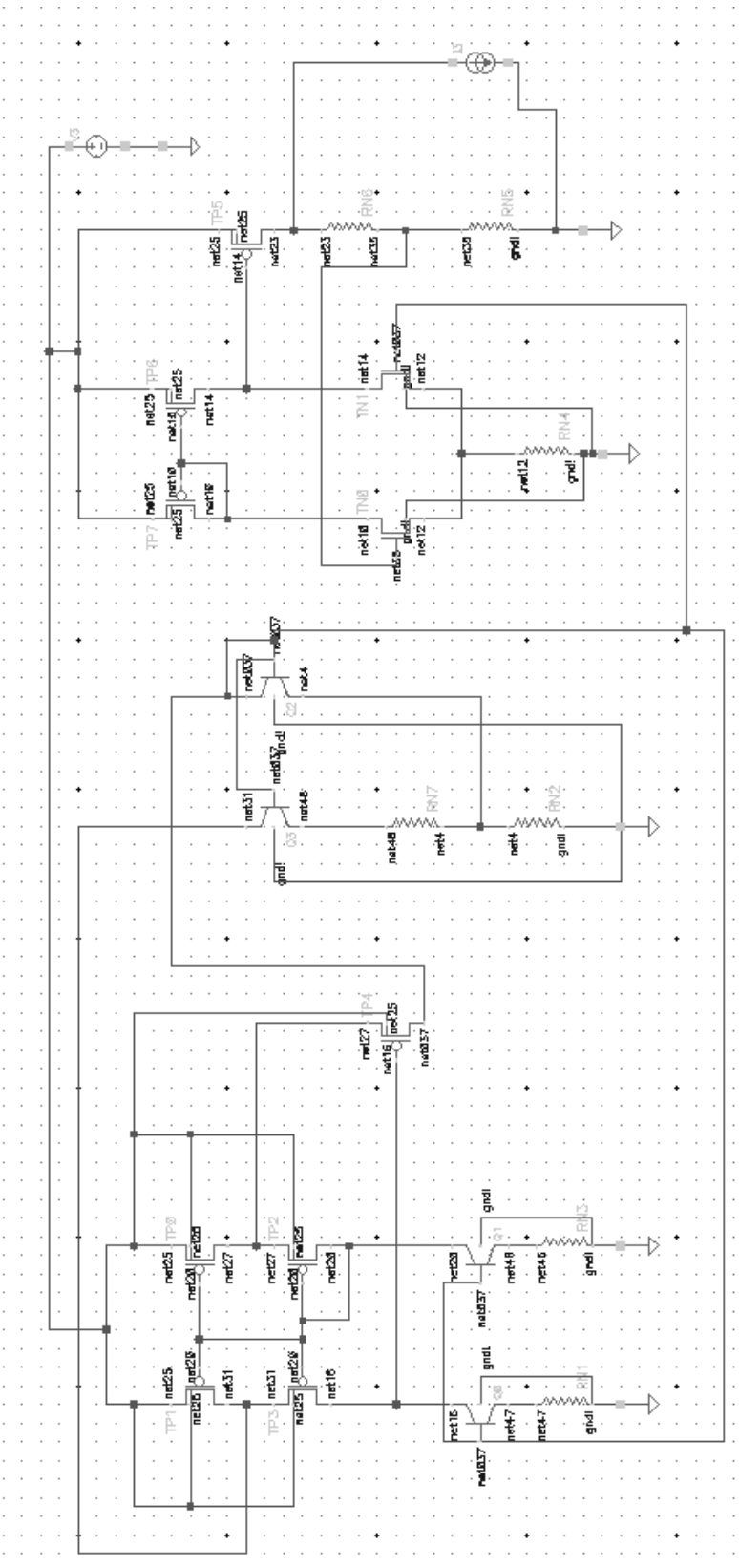
throughout the layout process. Main sources of errors were due to the bipolar junction transistors and resistors used in this design.

As a result of this project the group gained experience with analog VLSI circuit design, placement, routing, and layout. The group also gained further insight as to how mosfets, bipolar junction transistors, and resistors are fabricated on chip. In summary, this project was found to be challenging and rewarding. The group found this to be a very valuable experience and group members feel more confident with analog circuit design, Cadence VLSI software, and the semiconductor device fabrication process as a result of this project.

Appendix



Appendix A: Final Voltage Regulator Schematic Design



Appendix B: Final Schematic of Regulator Design Used for Simulating

References

[1] 2015. [Online]. Available: http://circuit-diagram.hqew.net/Discrete-Transistor-Voltage-Regulators_9685.html . [Accessed: 14- Oct- 2015].

[2]2015. [Online]. Available: http://cds.linear.com/docs/en/application-note/AN140fa.pdf. [Accessed: 14- Oct- 2015].

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