
**Algorithms and Data
Structures for External
Memory**

Algorithms and Data Structures for External Memory

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Abstract

Data sets in large applications are often too massive to fit completely inside the computer’s internal memory. The resulting input/output communication (or I/O) between fast internal memory and slower external memory (such as disks) can be a major performance bottleneck. In this manuscript, we survey the state of the art in the design and analysis of algorithms and data structures for *external memory* (or *EM* for short), where the goal is to exploit locality and parallelism in order to reduce the I/O costs. We consider a variety of EM paradigms for solving batched and online problems efficiently in external memory.

For the batched problem of sorting and related problems like permuting and fast Fourier transform, the key paradigms include distribution and merging. The paradigm of disk striping offers an elegant way to use multiple disks in parallel. For sorting, however, disk striping can be nonoptimal with respect to I/O, so to gain further improvements we discuss distribution and merging techniques for using the disks independently. We also consider useful techniques for batched EM problems involving matrices, geometric data, and graphs.

In the online domain, canonical EM applications include dictionary lookup and range searching. The two important classes of indexed data structures are based upon extendible hashing and B-trees. The paradigms of filtering and bootstrapping provide convenient means in online data structures to make effective use of the data accessed from disk. We also re-examine some of the above EM problems in slightly different settings, such as when the data items are moving, when the data items are variable-length such as character strings, when the data structure is compressed to save space, or when the allocated amount of internal memory can change dynamically.

Programming tools and environments are available for simplifying the EM programming task. We report on some experiments in the domain of spatial databases using the TPIE system (Transparent Parallel I/O programming Environment). The newly developed EM algorithms and data structures that incorporate the paradigms we discuss are significantly faster than other methods used in practice.

Preface

I first became fascinated about the tradeoffs between computing and memory usage while a graduate student at Stanford University. Over the following years, this theme has influenced much of what I have done professionally, not only in the field of external memory algorithms, which this manuscript is about, but also on other topics such as data compression, data mining, databases, prefetching/caching, and random sampling.

The reality of the computer world is that no matter how fast computers are and no matter how much data storage they provide, there will always be a desire and need to push the envelope. The solution is not to wait for the next generation of computers, but rather to examine the fundamental constraints in order to understand the limits of what is possible and to translate that understanding into effective solutions.

In this manuscript you will consider a scenario that arises often in large computing applications, namely, that the relevant data sets are simply too massive to fit completely inside the computer's internal memory and must instead reside on disk. The resulting input/output communication (or I/O) between fast internal memory and slower external memory (such as disks) can be a major performance

bottleneck. This manuscript provides a detailed overview of the design and analysis of algorithms and data structures for *external memory* (or simply *EM*), where the goal is to exploit locality and parallelism in order to reduce the I/O costs. Along the way, you will learn a variety of EM paradigms for solving batched and online problems efficiently.

For the batched problem of sorting and related problems like permuting and fast Fourier transform, the two fundamental paradigms are distribution and merging. The paradigm of disk striping offers an elegant way to use multiple disks in parallel. For sorting, however, disk striping can be nonoptimal with respect to I/O, so to gain further improvements we discuss distribution and merging techniques for using the disks independently, including an elegant duality property that yields state-of-the-art algorithms. You will encounter other useful techniques for batched EM problems involving matrices (such as matrix multiplication and transposition), geometric data (such as finding intersections and constructing convex hulls) and graphs (such as list ranking, connected components, topological sorting, and shortest paths).

In the online domain, which involves constructing data structures to answer queries, we discuss two canonical EM search applications: dictionary lookup and range searching. Two important paradigms for developing indexed data structures for these problems are hashing (including extendible hashing) and tree-based search (including B-trees). The paradigms of filtering and bootstrapping provide convenient means in online data structures to make effective use of the data accessed from disk. You will also be exposed to some of the above EM problems in slightly different settings, such as when the data items are moving, when the data items are variable-length (e.g., strings of text), when the data structure is compressed to save space, and when the allocated amount of internal memory can change dynamically.

Programming tools and environments are available for simplifying the EM programming task. You will see some experimental results in the domain of spatial databases using the TPIE system, which stands for Transparent Parallel I/O programming Environment. The newly developed EM algorithms and data structures that incorporate the paradigms discussed in this manuscript are significantly faster than other methods used in practice.

I would like to thank my colleagues for several helpful comments, especially Pankaj Agarwal, Lars Arge, Ricardo Baeza-Yates, Adam Buchsbaum, Jeffrey Chase, Michael Goodrich, Wing-Kai Hon, David Hutchinson, Gonzalo Navarro, Vasilis Samoladas, Peter Sanders, Rahul Shah, Amin Vahdat, and Norbert Zeh. I also thank the referees and editors for their help and suggestions, as well as the many wonderful staff members I've had the privilege to work with. Figure 1.1 is a modified version of a figure by Darren Vengroff, and Figures 2.1 and 5.2 come from [118, 342]. Figures 5.4–5.8, 8.2–8.3, 10.1, 12.1, 12.2, 12.4, and 14.1 are modified versions of figures in [202, 47, 147, 210, 41, 50, 158], respectively.

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West Lafayette, Indiana
March 2008

— J. S. V.

Contents

1	Introduction	1
1.1	Overview	4
2	Parallel Disk Model (PDM)	9
2.1	PDM and Problem Parameters	11
2.2	Practical Modeling Considerations	14
2.3	Related Models, Hierarchical Memory, and Cache-Oblivious Algorithms	16
3	Fundamental I/O Operations and Bounds	21
4	Exploiting Locality and Load Balancing	25
4.1	Locality Issues with a Single Disk	26
4.2	Disk Striping and Parallelism with Multiple Disks	27
5	External Sorting and Related Problems	29
5.1	Sorting by Distribution	31
5.2	Sorting by Merging	38
5.3	Prefetching, Caching, and Applications to Sorting	42
5.4	A General Simulation for Parallel Disks	52
5.5	Handling Duplicates: Bundle Sorting	53
5.6	Permuting	54
5.7	Fast Fourier Transform and Permutation Networks	54

xiv *Contents*

6 Lower Bounds on I/O	57
6.1 Permuting	57
6.2 Lower Bounds for Sorting and Other Problems	61
7 Matrix and Grid Computations	65
7.1 Matrix Operations	65
7.2 Matrix Transposition	66
8 Batched Problems in Computational Geometry	69
8.1 Distribution Sweep	71
8.2 Other Batched Geometric Problems	76
9 Batched Problems on Graphs	77
9.1 Sparsification	80
9.2 Special Cases	81
9.3 Sequential Simulation of Parallel Algorithms	81
10 External Hashing for Online Dictionary Search	83
10.1 Extendible Hashing	84
10.2 Directoryless Methods	87
10.3 Additional Perspectives	87
11 Multiway Tree Data Structures	89
11.1 B-trees and Variants	89
11.2 Weight-Balanced B-trees	92
11.3 Parent Pointers and Level-Balanced B-trees	93
11.4 Buffer Trees	95
12 Spatial Data Structures and Range Search	99
12.1 Linear-Space Spatial Structures	102
12.2 R-trees	103

12.3 Bootstrapping for 2-D Diagonal Corner and Stabbing Queries	107
12.4 Bootstrapping for Three-Sided Orthogonal 2-D Range Search	110
12.5 General Orthogonal 2-D Range Search	112
12.6 Other Types of Range Search	114
12.7 Lower Bounds for Orthogonal Range Search	116
13 Dynamic and Kinetic Data Structures	119
13.1 Dynamic Methods for Decomposable Search Problems	119
13.2 Continuously Moving Items	121
14 String Processing	123
14.1 Inverted Files	123
14.2 String B-Trees	124
14.3 Suffix Trees and Suffix Arrays	127
14.4 Sorting Strings	127
15 Compressed Data Structures	129
15.1 Data Representations and Compression Models	130
15.2 External Memory Compressed Data Structures	133
16 Dynamic Memory Allocation	139
17 External Memory Programming Environments	141
Conclusions	145
Notations and Acronyms	147
References	151

1

Introduction

The world is drowning in data! In recent years, we have been deluged by a torrent of data from a variety of increasingly data-intensive applications, including databases, scientific computations, graphics, entertainment, multimedia, sensors, web applications, and email. NASA's Earth Observing System project, the core part of the Earth Science Enterprise (formerly Mission to Planet Earth), produces petabytes (10^{15} bytes) of raster data per year [148]. A petabyte corresponds roughly to the amount of information in one billion graphically formatted books. The online databases of satellite images used by Microsoft TerraServer (part of MSN Virtual Earth) [325] and Google Earth [180] are multiple terabytes (10^{12} bytes) in size. Wal-Mart's sales data warehouse contains over a half petabyte (500 terabytes) of data. A major challenge is to develop mechanisms for processing the data, or else much of the data will be useless.

For reasons of economy, general-purpose computer systems usually contain a hierarchy of memory levels, each level with its own cost and performance characteristics. At the lowest level, CPU registers and caches are built with the fastest but most expensive memory. For internal main memory, dynamic random access memory (DRAM) is

2 Introduction

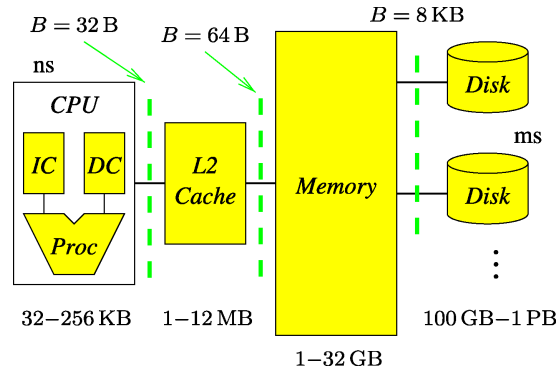


Fig. 1.1 The memory hierarchy of a typical uniprocessor system, including registers, instruction cache, data cache (level 1 cache), level 2 cache, internal memory, and disks. Some systems have in addition a level 3 cache, not shown here. Memory access latency ranges from less than one nanosecond (ns, 10^{-9} seconds) for registers and level 1 cache to several milliseconds (ms, 10^{-3} seconds) for disks. Typical memory sizes for each level of the hierarchy are shown at the bottom. Each value of B listed at the top of the figure denotes a typical block transfer size between two adjacent levels of the hierarchy. All sizes are given in units of bytes (B), kilobytes (KB, 10^3 B), megabytes (MB, 10^6 B), gigabytes (GB, 10^9 B), and petabytes (PB, 10^{15} B). (In the PDM model defined in Chapter 2, we measure the block size B in units of items rather than in units of bytes.) In this figure, 8 KB is the indicated physical block transfer size between internal memory and the disks. However, in batched applications we often use a substantially larger logical block transfer size.

typical. At a higher level, inexpensive but slower magnetic disks are used for external mass storage, and even slower but larger-capacity devices such as tapes and optical disks are used for archival storage. These devices can be attached via a network fabric (e.g., Fibre Channel or iSCSI) to provide substantial external storage capacity. Figure 1.1 depicts a typical memory hierarchy and its characteristics.

Most modern programming languages are based upon a programming model in which memory consists of one uniform address space. The notion of virtual memory allows the address space to be far larger than what can fit in the internal memory of the computer. Programmers have a natural tendency to assume that all memory references require the same access time. In many cases, such an assumption is reasonable (or at least does not do harm), especially when the data sets are not large. The utility and elegance of this programming model are to a large extent why it has flourished, contributing to the productivity of the software industry.

However, not all memory references are created equal. Large address spaces span multiple levels of the memory hierarchy, and accessing the data in the lowest levels of memory is orders of magnitude faster than accessing the data at the higher levels. For example, loading a register can take a fraction of a nanosecond (10^{-9} seconds), and accessing internal memory takes several nanoseconds, but the latency of accessing data on a disk is multiple milliseconds (10^{-3} seconds), which is about one million times slower! In applications that process massive amounts of data, the *Input/Output* communication (or simply *I/O*) between levels of memory is often the bottleneck.

Many computer programs exhibit some degree of *locality* in their pattern of memory references: Certain data are referenced repeatedly for a while, and then the program shifts attention to other sets of data. Modern operating systems take advantage of such access patterns by tracking the program's so-called "working set" — a vague notion that roughly corresponds to the recently referenced data items [139]. If the working set is small, it can be cached in high-speed memory so that access to it is fast. Caching and prefetching heuristics have been developed to reduce the number of occurrences of a "fault," in which the referenced data item is not in the cache and must be retrieved by an I/O from a higher level of memory. For example, in a page fault, an I/O is needed to retrieve a disk page from disk and bring it into internal memory.

Caching and prefetching methods are typically designed to be general-purpose, and thus they cannot be expected to take full advantage of the locality present in every computation. Some computations themselves are inherently nonlocal, and even with omniscient cache management decisions they are doomed to perform large amounts of I/O and suffer poor performance. Substantial gains in performance may be possible by incorporating locality *directly* into the algorithm design and by explicit management of the contents of each level of the memory hierarchy, thereby bypassing the virtual memory system.

We refer to algorithms and data structures that explicitly manage data placement and movement as *external memory* (or *EM*) *algorithms and data structures*. Some authors use the terms *I/O algorithms* or *out-of-core algorithms*. We concentrate in this manuscript on the I/O

4 Introduction

communication between the random access internal memory and the magnetic disk external memory, where the relative difference in access speeds is most apparent. We therefore use the term I/O to designate the communication between the internal memory and the disks.

1.1 Overview

In this manuscript, we survey several paradigms for exploiting locality and thereby reducing I/O costs when solving problems in external memory. The problems we consider fall into two general categories:

- (1) *Batched problems*, in which no preprocessing is done and the entire file of data items must be processed, often by streaming the data through the internal memory in one or more passes.
- (2) *Online problems*, in which computation is done in response to a continuous series of query operations. A common technique for online problems is to organize the data items via a hierarchical index, so that only a very small portion of the data needs to be examined in response to each query. The data being queried can be either *static*, which can be pre-processed for efficient query processing, or *dynamic*, where the queries are intermixed with updates such as insertions and deletions.

We base our approach upon the *parallel disk model* (PDM) described in the next chapter. PDM provides an elegant and reasonably accurate model for analyzing the relative performance of EM algorithms and data structures. The three main performance measures of PDM are *the number of (parallel) I/O operations*, *the disk space usage*, and *the (parallel) CPU time*. For reasons of brevity, we focus on the first two measures. Most of the algorithms we consider are also efficient in terms of CPU time. In Chapter 3, we list four fundamental I/O bounds that pertain to most of the problems considered in this manuscript. In Chapter 4, we show why it is crucial for EM algorithms to exploit locality, and we discuss an automatic load balancing technique called disk striping for using multiple disks in parallel.

Our general goal is to design optimal algorithms and data structures, by which we mean that their performance measures are within a constant factor of the optimum or best possible.¹ In Chapter 5, we look at the canonical batched EM problem of external sorting and the related problems of permuting and fast Fourier transform. The two important paradigms of distribution and merging — as well as the notion of duality that relates the two — account for all well-known external sorting algorithms. Sorting with a single disk is now well understood, so we concentrate on the more challenging task of using multiple (or parallel) disks, for which disk striping is not optimal. The challenge is to guarantee that the data in each I/O are spread evenly across the disks so that the disks can be used simultaneously. In Chapter 6, we cover the fundamental lower bounds on the number of I/Os needed to perform sorting and related batched problems. In Chapter 7, we discuss grid and linear algebra batched computations.

For most problems, parallel disks can be utilized effectively by means of disk striping or the parallel disk techniques of Chapter 5, and hence we restrict ourselves starting in Chapter 8 to the conceptually simpler single-disk case. In Chapter 8, we mention several effective paradigms for batched EM problems in computational geometry. The paradigms include distribution sweep (for spatial join and finding all nearest neighbors), persistent B-trees (for batched point location and visibility), batched filtering (for 3-D convex hulls and batched point location), external fractional cascading (for red-blue line segment intersection), external marriage-before-conquest (for output-sensitive convex hulls), and randomized incremental construction with gradations (for line segment intersections and other geometric problems). In Chapter 9, we look at EM algorithms for combinatorial problems on graphs, such as list ranking, connected components, topological sorting, and finding shortest paths. One technique for constructing I/O-efficient EM algorithms is to simulate parallel algorithms; sorting is used between parallel steps in order to reblock the data for the simulation of the next parallel step.

¹In this manuscript we generally use the term “optimum” to denote the absolute best possible and the term “optimal” to mean within a constant factor of the optimum.

6 *Introduction*

In Chapters 10–12, we consider data structures in the online setting. The dynamic dictionary operations of insert, delete, and lookup can be implemented by the well-known method of hashing. In Chapter 10, we examine hashing in external memory, in which extra care must be taken to pack data into blocks and to allow the number of items to vary dynamically. Lookups can be done generally with only one or two I/Os. Chapter 11 begins with a discussion of B-trees, the most widely used online EM data structure for dictionary operations and one-dimensional range queries. Weight-balanced B-trees provide a uniform mechanism for dynamically rebuilding substructures and are useful for a variety of online data structures. Level-balanced B-trees permit maintenance of parent pointers and support cut and concatenate operations, which are used in reachability queries on monotone subdivisions. The buffer tree is a so-called “batched dynamic” version of the B-tree for efficient implementation of search trees and priority queues in EM sweep line applications. In Chapter 12, we discuss spatial data structures for multidimensional data, especially those that support online range search. Multidimensional extensions of the B-tree, such as the popular R-tree and its variants, use a linear amount of disk space and often perform well in practice, although their worst-case performance is poor. A non-linear amount of disk space is required to perform 2-D orthogonal range queries efficiently in the worst case, but several important special cases of range searching can be done efficiently using only linear space. A useful design paradigm for EM data structures is to “externalize” an efficient data structure designed for internal memory; a key component of how to make the structure I/O-efficient is to “bootstrap” a static EM data structure for small-sized problems into a fully dynamic data structure of arbitrary size. This paradigm provides optimal linear-space EM data structures for several variants of 2-D orthogonal range search.

In Chapter 13, we discuss some additional EM approaches useful for dynamic data structures, and we also investigate kinetic data structures, in which the data items are moving. In Chapter 14, we focus on EM data structures for manipulating and searching text strings. In many applications, especially those that operate on text strings, the data are highly compressible. Chapter 15 discusses ways to develop data structures that are themselves compressed, but still fast to query.

Table 1.1 Paradigms for I/O efficiency discussed in this manuscript.

Paradigm	Section
Batched dynamic processing	11.4
Batched filtering	8
Batched incremental construction	8
Bootstrapping	12
Buffer trees	11.4
B-trees	11, 12
Compression	15
Decomposable search	13.1
Disk striping	4.2
Distribution	5.1
Distribution sweeping	8
Duality	5.3
External hashing	10
Externalization	12.3
Fractional cascading	8
Filtering	12
Lazy updating	11.4
Load balancing	4
Locality	4.1
Marriage before conquest	8
Merging	5.2
Parallel block transfer	4.2
Parallel simulation	9
Persistence	11.1
Random sampling	5.1
R-trees	12.2
Scanning (or streaming)	2.2
Sparsification	9
Time-forward processing	11.4

In Chapter 16, we discuss EM algorithms that adapt optimally to dynamically changing internal memory allocations.

In Chapter 17, we discuss programming environments and tools that facilitate high-level development of efficient EM algorithms. We focus primarily on the TPIE system (Transparent Parallel I/O Environment), which we use in the various timing experiments in this manuscript. We conclude with some final remarks and observations in the Conclusions.

Table 1.1 lists several of the EM paradigms discussed in this manuscript.

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152 *References*

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160 *References*

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174 *References*

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