ESE 570: Digital Integrated Circuits and VLSI Fundamentals

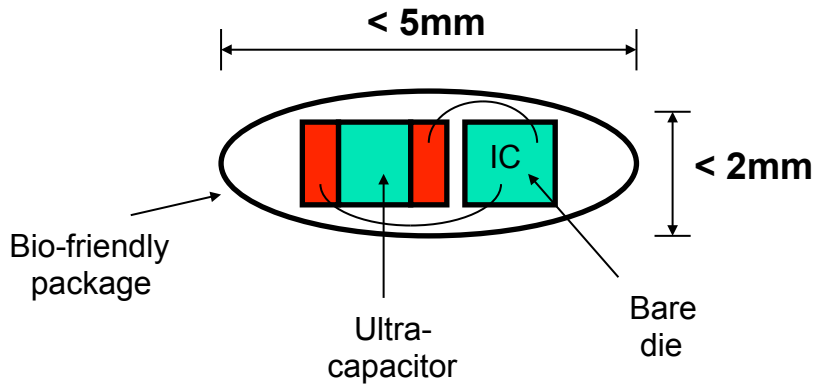
Lec 1: January 12, 2017

Introduction and Overview

Where I come from

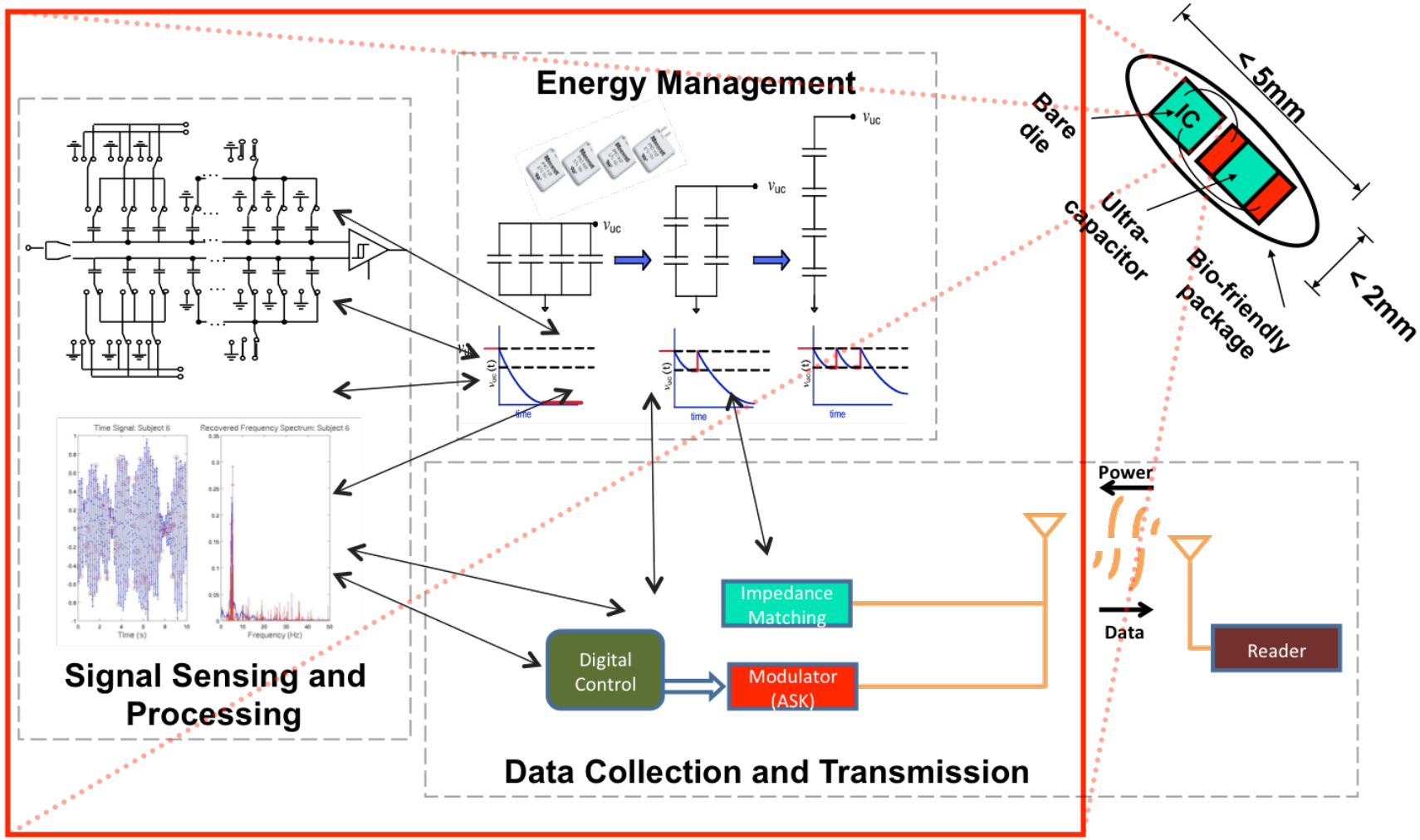
- Analog VLSI Circuit Design
- Convex Optimization
  - System Hierarchical Optimization
- Biomedical Electronics
- Biometric Data Acquisition
  - Compressive Sampling
- ADC Design
  - SAR, Pipeline, Delta-Sigma
- Low Energy Circuits
  - Adiabatic Charging

Minimally Invasive Implant to Combat Healthcare Noncompliance



- Model for implants: reconfigurable RFID tags that continuously record specific biometric
  - During the read operation, energy storage element is recharged
- Size of package small enough to allow injection
- Actigraphy expected to be clinically useful
  - Platform allows for any sensor that gathers information on a slow time scale

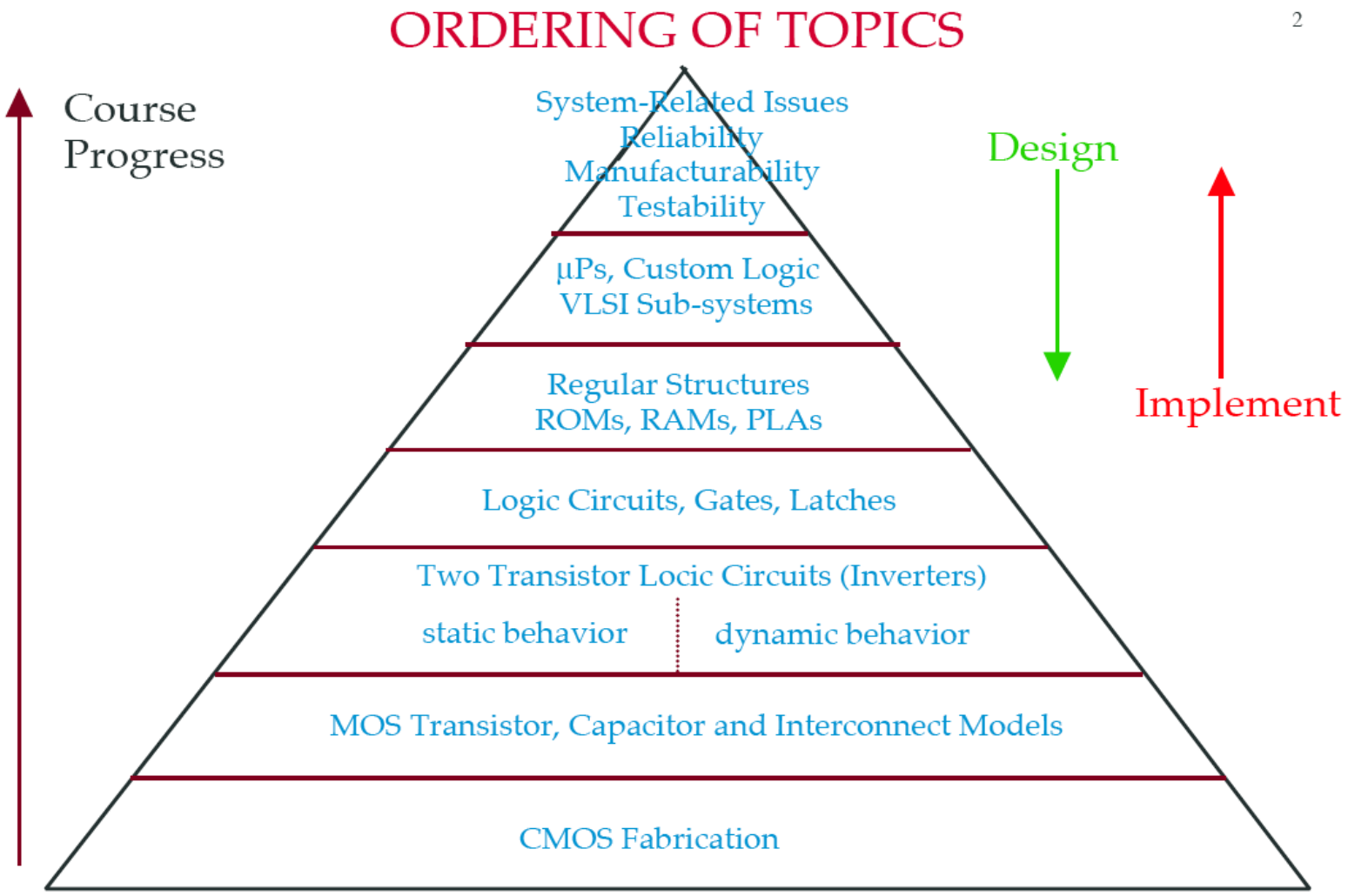
MicroImplant: An Electronic Platform for Minimally Invasive Sensory Monitors



Lecture Outline

- Course Topics Overview
- Learning Objectives
- Course Structure
- Course Policies
- Course Content
- Industry Trends
- Design Example

Course Topics Overview



Learning Objectives

- Apply principles of hierarchical digital CMOS VLSI, from the transistor up to the system level, to the understanding of CMOS circuits and systems that are suitable for CMOS fabrication.
- Apply the models for state-of-the-art VLSI components, fabrication steps, hierarchical design flow and semiconductor business economics to judge the manufacturability of a design and estimate its manufacturing costs.
- Design simulated experiments using Cadence to verify the integrity of a CMOS circuit and its layout.
- Design digital circuits that are manufacturable in CMOS.
- Apply the Cadence VLSI CAD tool suite layout digital circuits for CMOS fabrication and verify said circuits with layout parasitic elements.
- Apply course knowledge and the Cadence VLSI CAD tools in a team based capstone design project that involves much the same design flow they would encounter in a semiconductor design industrial setting. Capstone project is presented in a formal report due at the end of the semester.

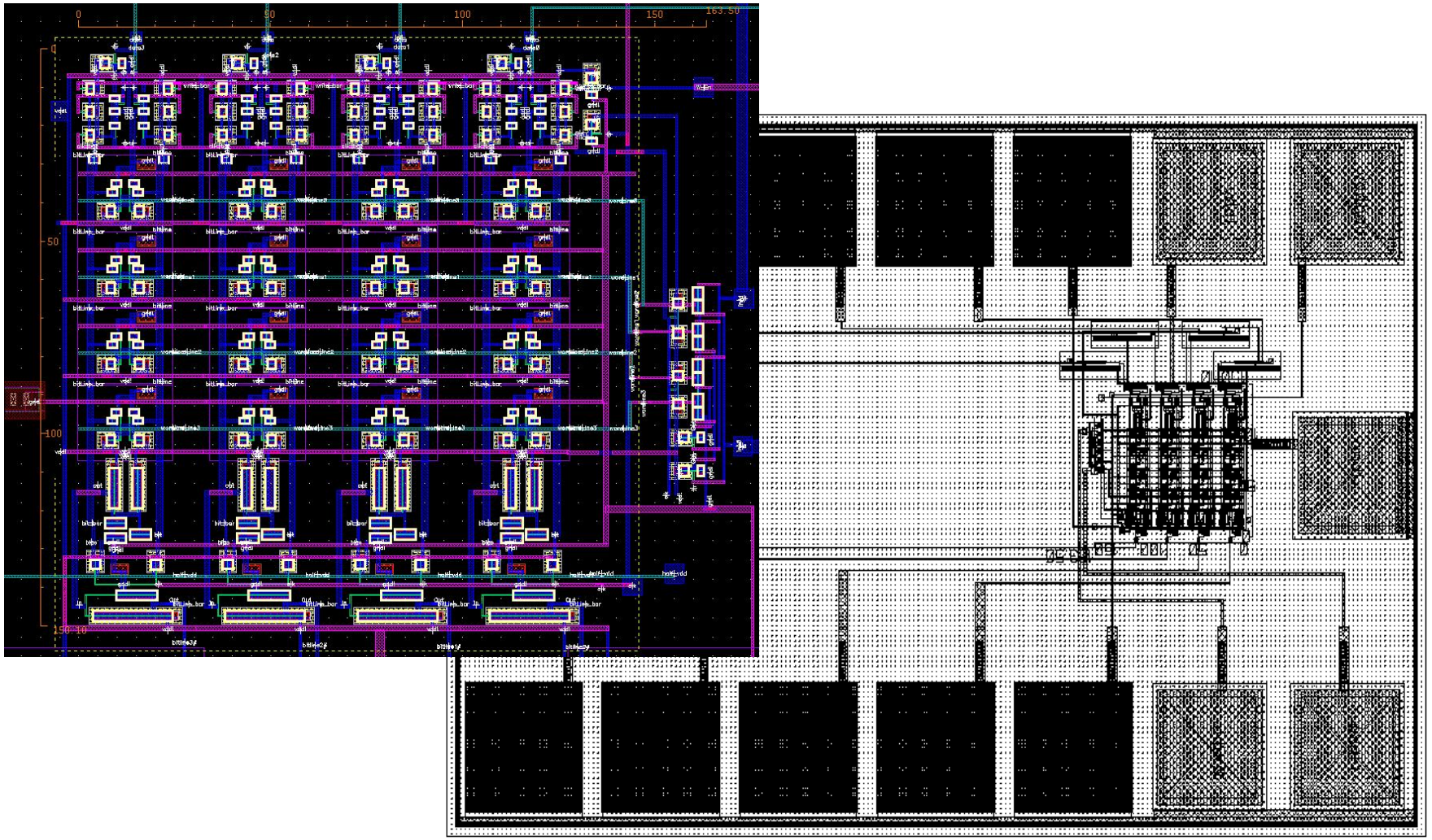
Learning Objectives

- In other words…

- Design in CADENCE*

*All the way to layout/manufacturability

Layout in Cadence



Course Structure

- TR Lecture, 1:30-3:00pm in Towne 321
  - Start 5 minutes after, end 5 minutes early (~75-80min)
- Website (http://www.seas.upenn.edu/~ese570/)
  - Course calendar is used for all handouts (lectures slides, assignments, and readings)
  - Canvas used for assignment submission and grades
  - Piazza used for announcements and discussions
  - Previous years' websites linked at bottom of this year

Course Structure

- Course Staff (complete info on course website)
- Instructor: Tania Khanna
  - Office hours – Wednesday 2-4:30 pm or by appointment
  - Email: taniak@seas.upenn.edu
    - Best way to reach me
- TA: Ryan Spicer
  - Office hours – TBD
- Grader: TBD

Course Structure

- Lectures
  - Statistically speaking, you will do better if you come to lecture
  - Better if interactive, **everyone** engaged
    - Asking and answering questions
    - Actively thinking about material
- Textbook
  - CMOS Digital Integrated Circuits Analysis and Design, Kang, Leblebici, and Kim, 4th edition
  - Class will follow text structure

Course Structure

- Cadence
  - Technology: AMI .6u C5N (3M, 2P, high-res)
  - Schematic simulation (SPECTRE simulator)
    - Design, analysis and test
  - Layout and verification
  - Analog extracted simulation
  - Standard Cells (?)

Course Structure - Assignments/Exams

- Homework – 1-2 week(s) long (8 total) [25%]
  - Due Thursdays at start of class (1:30pm)
  - HW 1 out now
- Project – two+ weeks long (2 total) [30%]
  - Design oriented
  - Project – design and layout SRAM memory
    - Propose alternate project
    - Propose extra credit to use your memory (eg. FIFO, shift reg, etc.)
- Midterm exam [20%]
- Final exam [25%]

Course Policies

See web page for full details

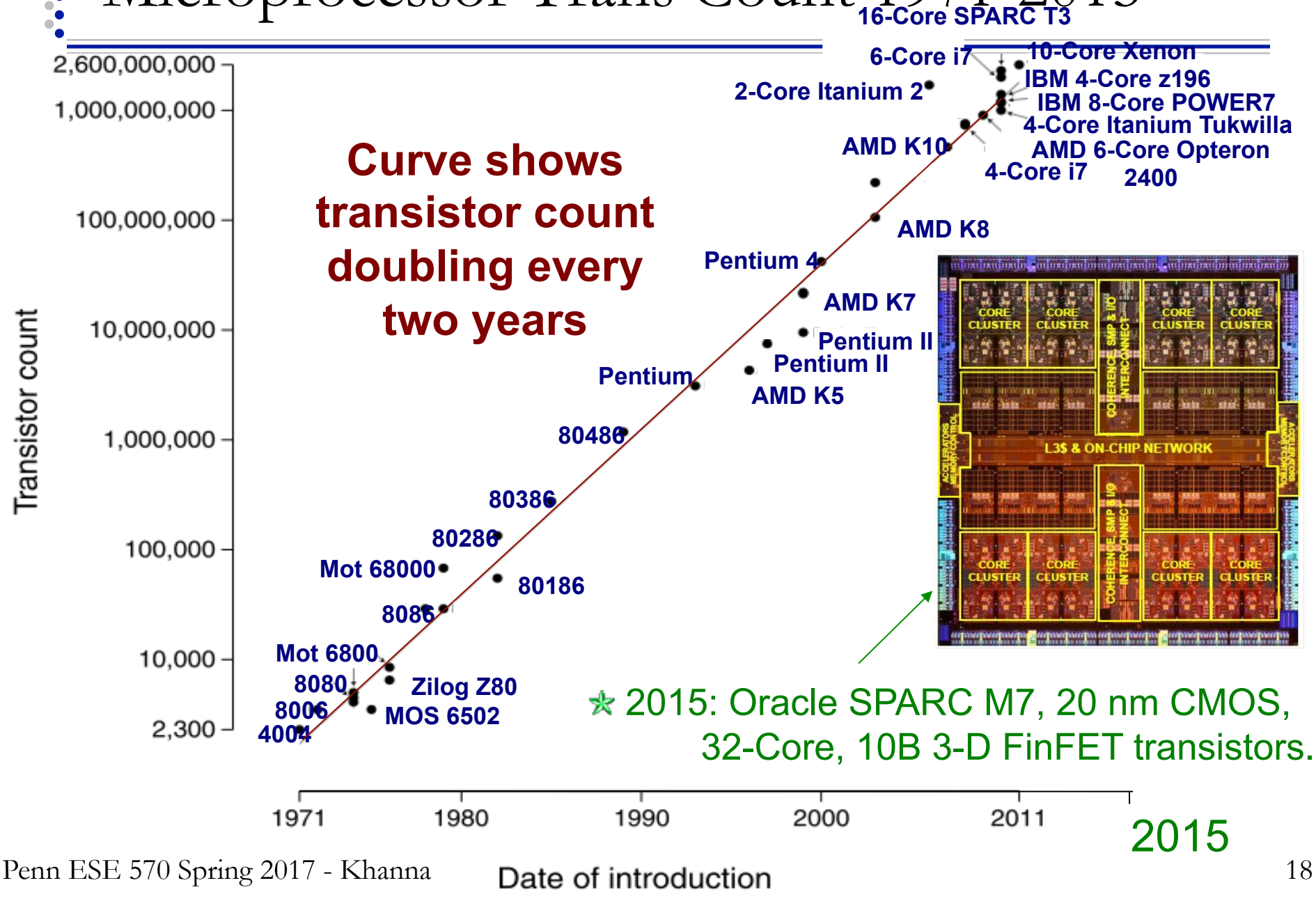
- Turn homework in Canvas before lecture starts
  - Anything handwritten/drawn must be clearly legible
  - Submit CAD generated figures, graphs, results when specified
  - NO LATE HOMEWORKS!
- Individual work (except project)
  - CAD drawings, simulations, analysis, writeups
  - May discuss strategies, but acknowledge help

Course Content

- Introduction
- Fabrication
- MOS Transistor Theory and Models
- MOS Models and IV characteristics
- Inverters: Static Characteristics and Performance
- Inverters: Dynamic Characteristics and Performance
- Combinational Logic Types (CMOS, Ratioed, Pass) and Performance
- Sequential Logic
- Dynamic Logic
- VLSI design and Scaling
- Memory Design
- I/O Circuits and Inductive Noise
- CLK Generation
- Robust VLSI Design for Variation

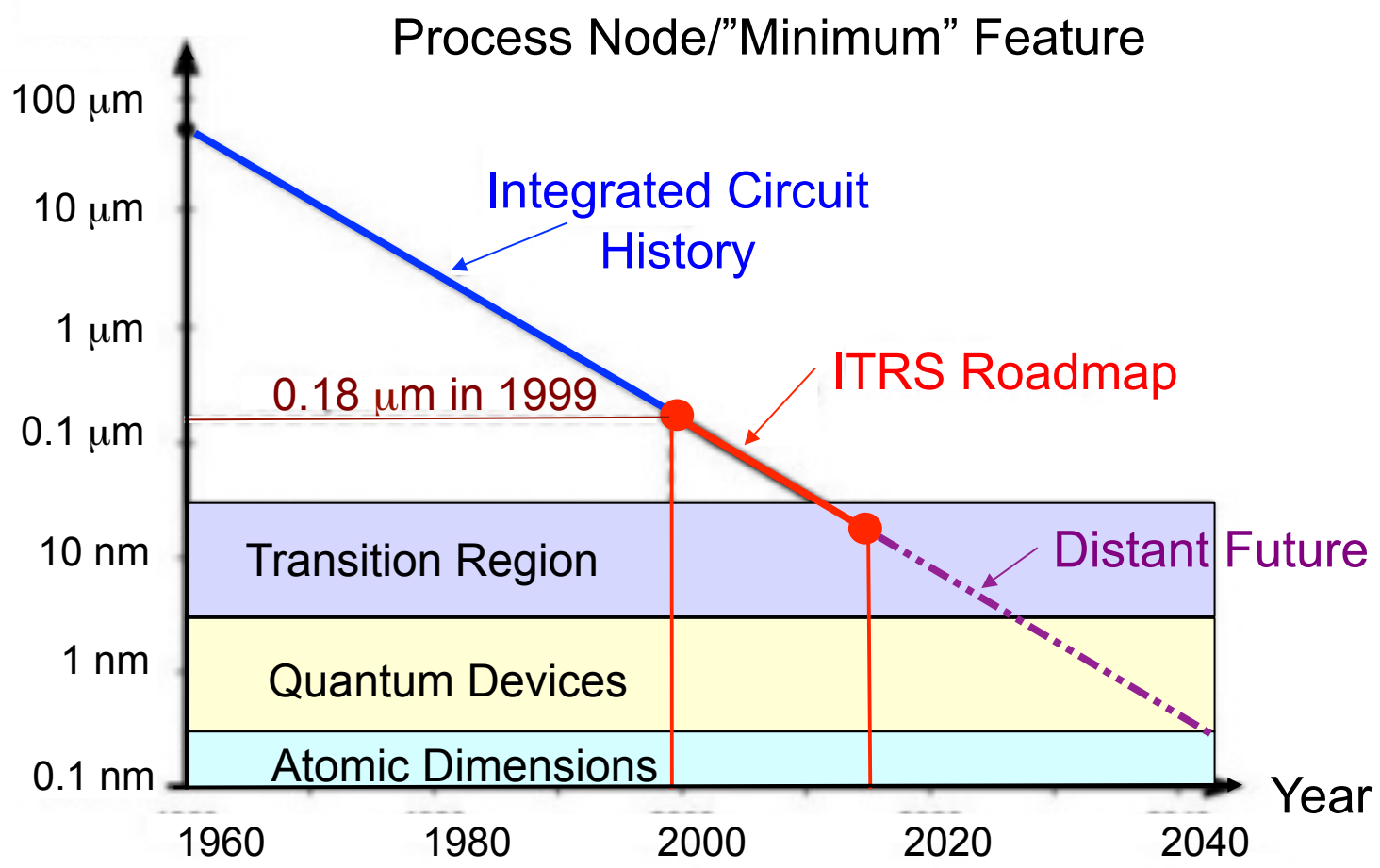
Industry Trends

Microprocessor Trans Count 1971-2015



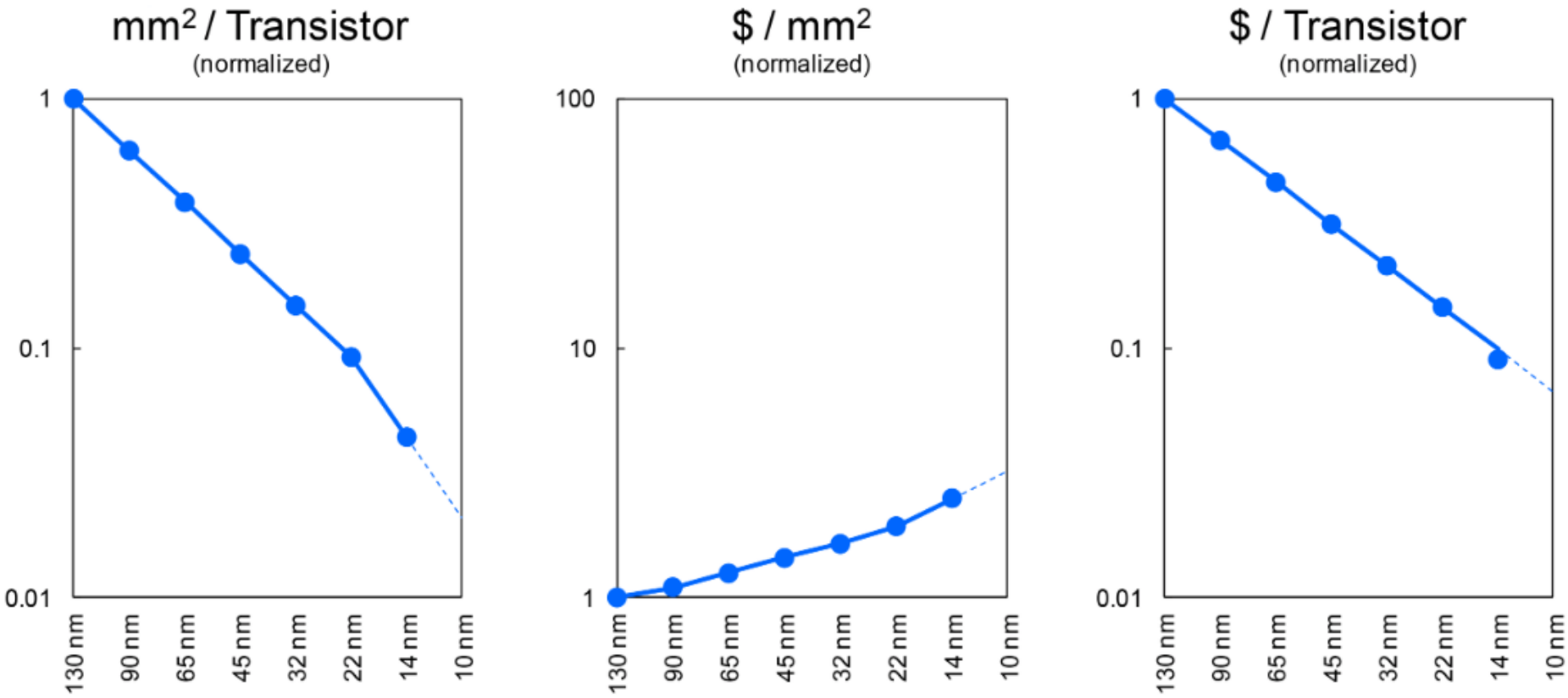
★ 2015: Oracle SPARC M7, 20 nm CMOS, 32-Core, 10B 3-D FinFET transistors.

Trend – "Minimum Feature Size vs. Year



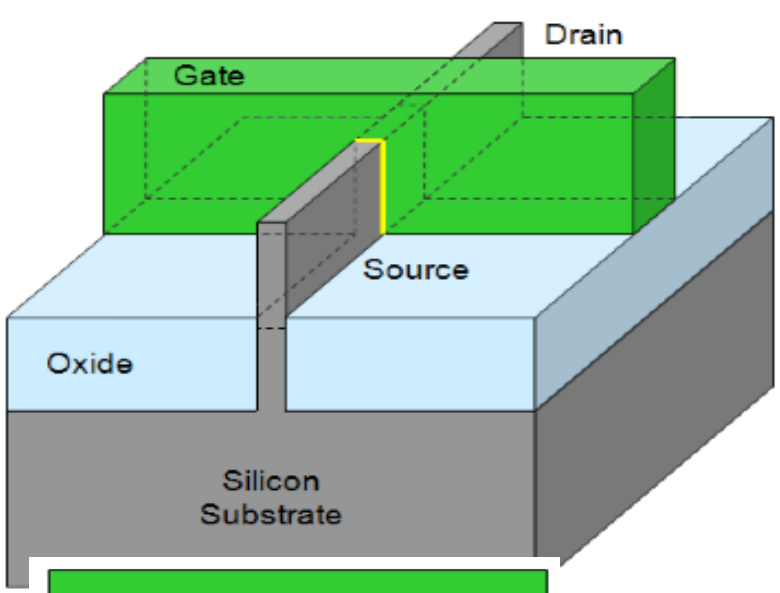
"Minimum" Feature Measure = line/gate conductor width or half-pitch (adjacent 1st metal layer lines or adjacent transistor gates)

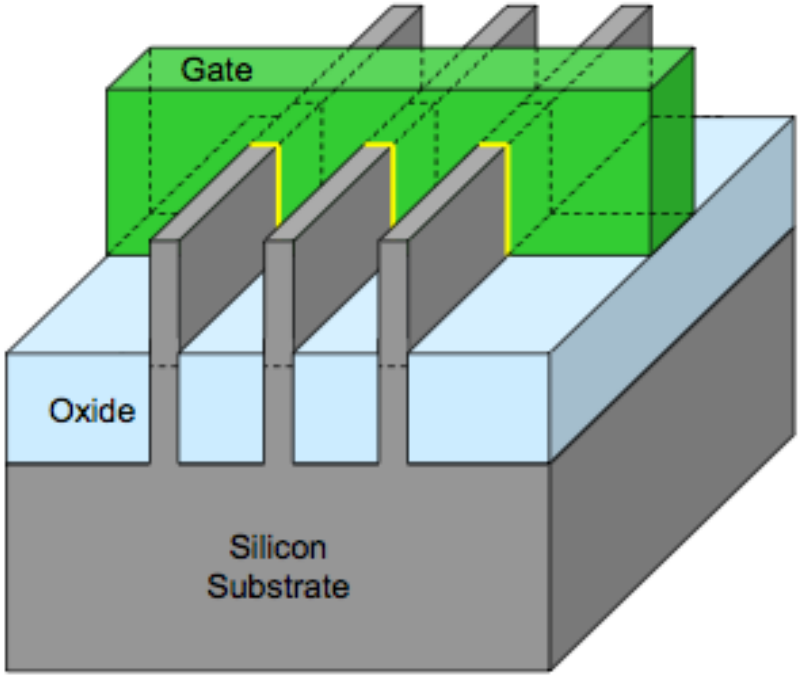
Intel Cost Scaling

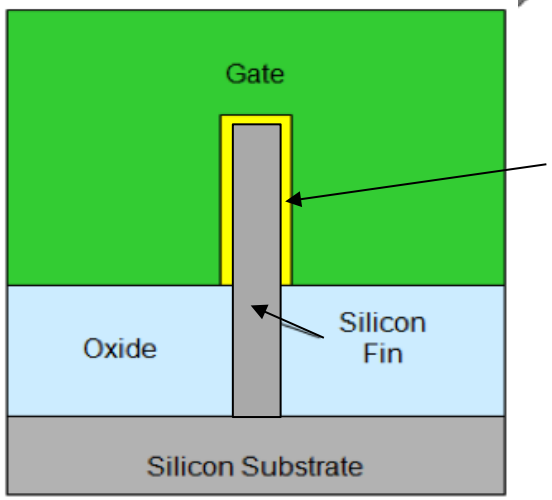


http://www.anandtech.com/show/8367/intels-14nm-technology-in-detail

22nm 3D FinFET Transistor





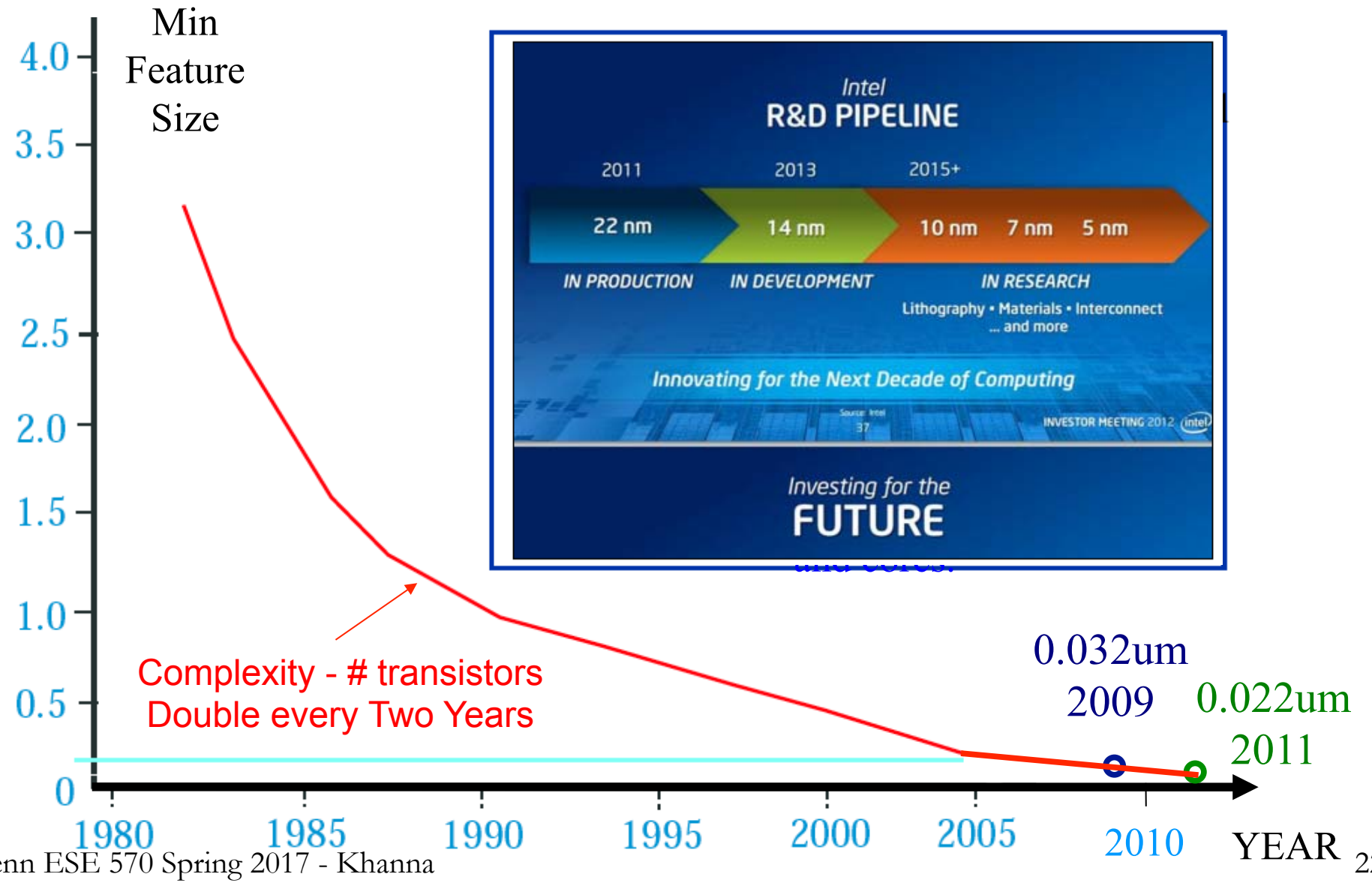


High-k gate dielectric

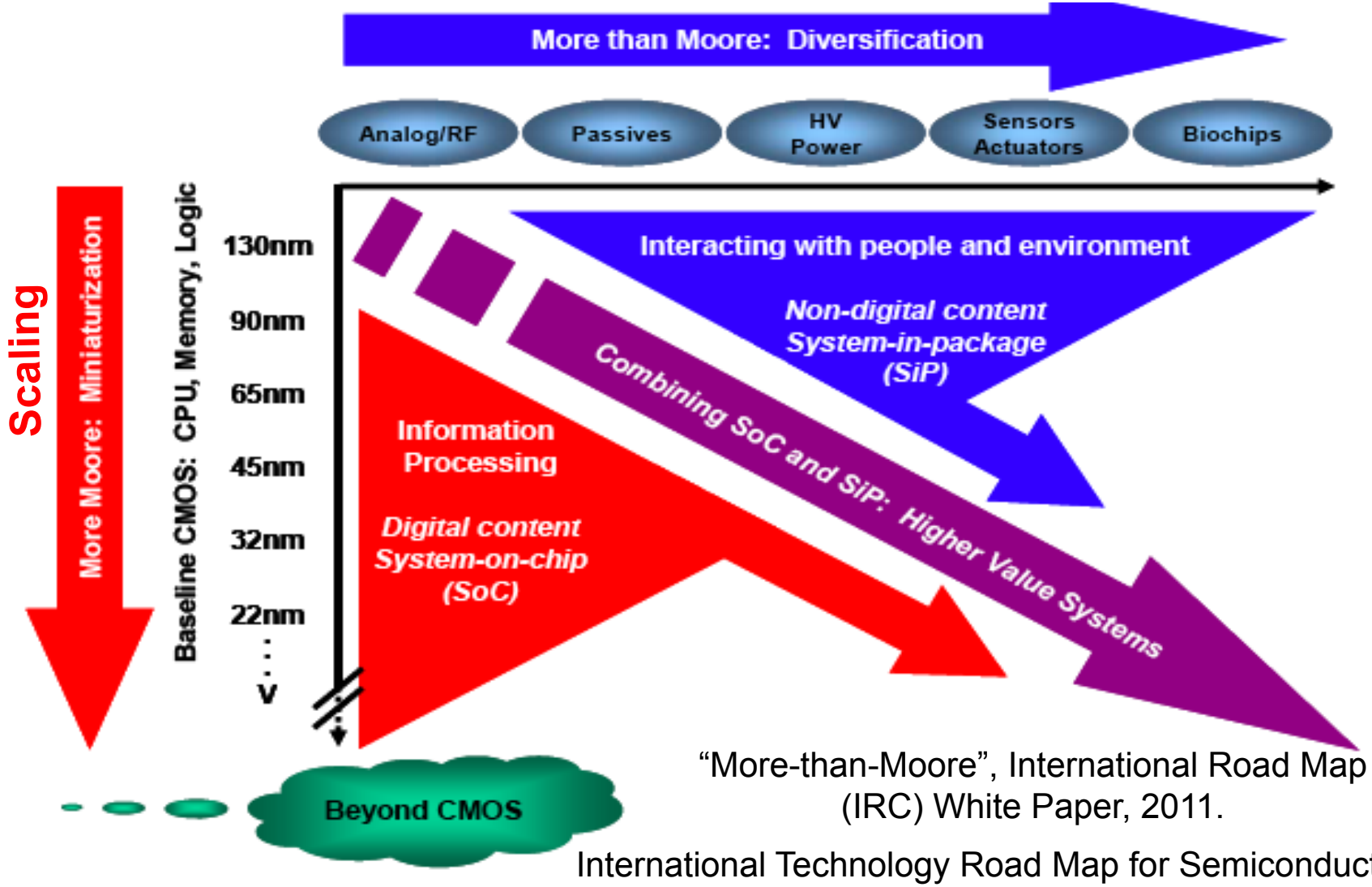
Tri-Gate transistors with multiple fins connected together increases total drive strength for higher performance

http://download.intel.com/newsroom/kits/22nm/pdfs/22nm-Details_Presentation.pdf

Moore's Law Impact on Intel uComputers



More-than-Moore



"More-than-Moore", International Road Map (IRC) White Paper, 2011.

International Technology Road Map for Semiconductors

More Moore → Scaling

- Geometrical Scaling
  - continued shrinking of horizontal and vertical physical feature sizes
- Equivalent Scaling
  - 3-dimensional device structure improvements and new materials that affect the electrical performance of the chip even if no geometrical scaling
- Design Equivalent Scaling
  - design technologies that enable high performance, low power, high reliability, low cost, and high design productivity even if neither geometrical nor equivalent scaling can be used

More Moore → Scaling

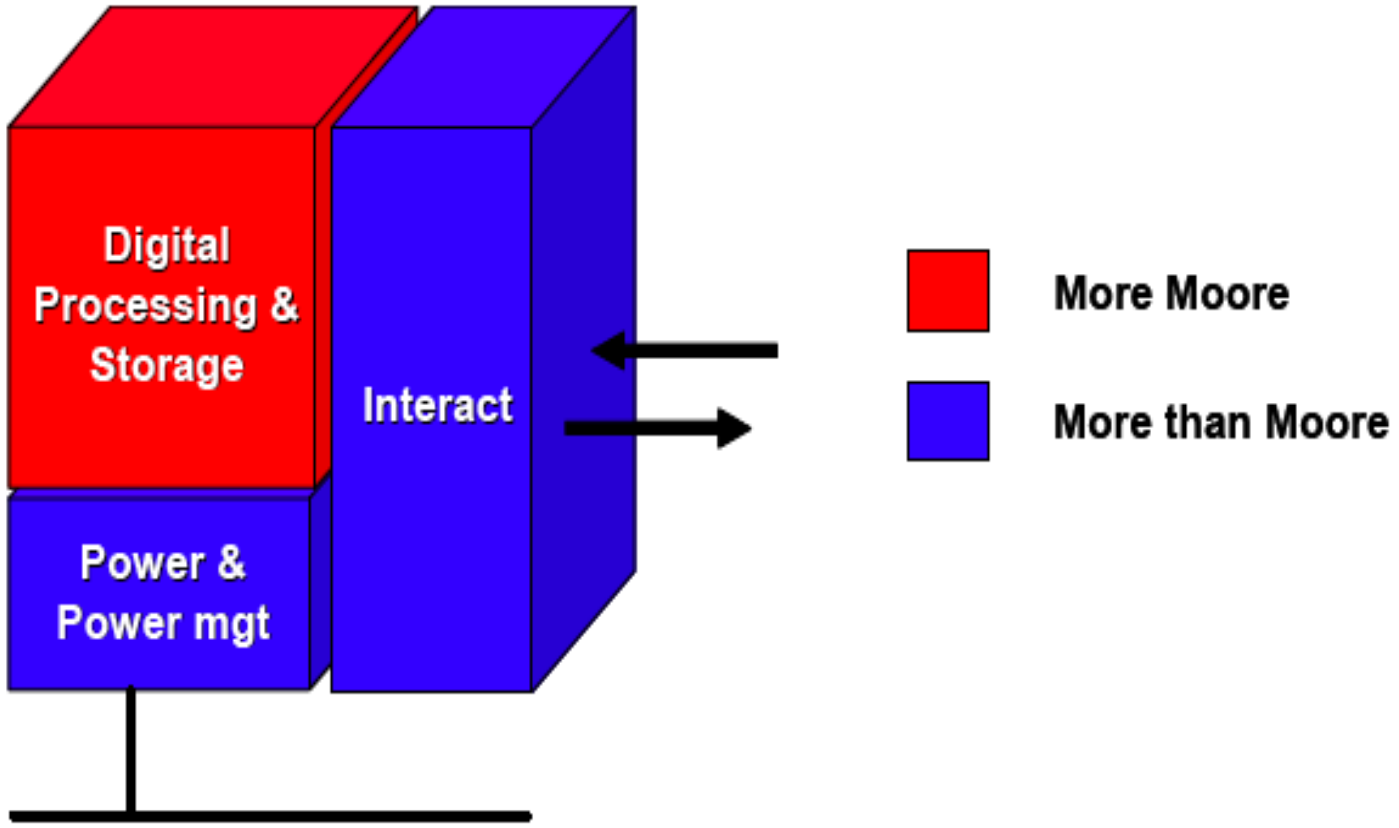
- Examples:
  - Design-for-variability
  - Low power design (sleep modes, clock gating, multi-Vdd, etc.)
  - Multi-core SOC architectures

More than Moore → Functional Diversification

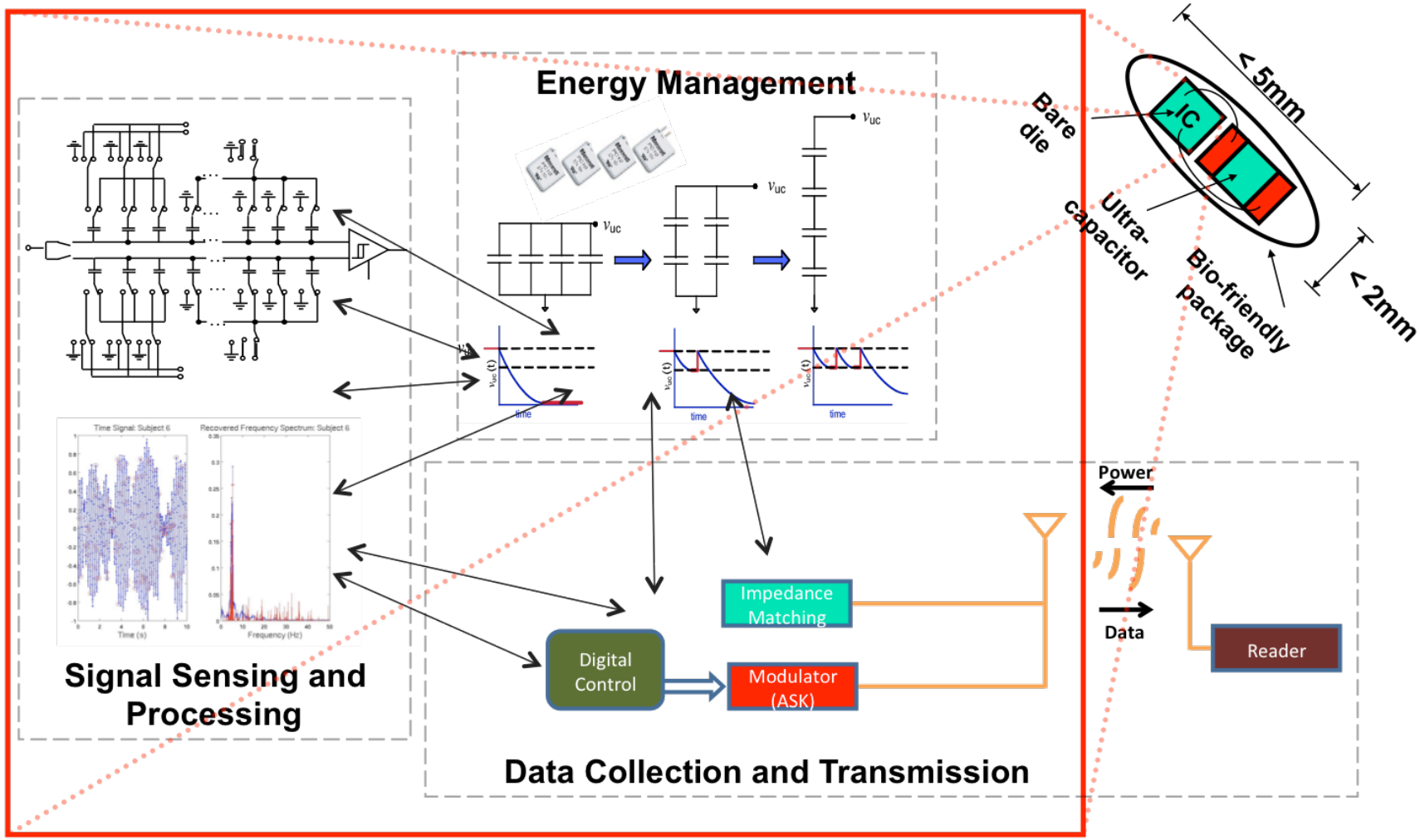
- Interacting with the outside world
  - Electromagnetic/Optical
    - Radio-frequency domain up to the THz range
    - Optical domain from the infrared to the near ultraviolet
    - Hard radiation (EUV, X-ray, γ-ray)
  - Mechanical parameters (sensors/actuators)
    - MEMS/NEMS position, speed, acceleration, rotation, pressure, stress, etc.
  - Chemical composition (sensors/actuators)
  - Biological parameters (sensors/actuators)
- Power/Energy
  - Integration of renewable sources, Energy storage, Smart metering, Efficient consumption

"More-than-Moore"

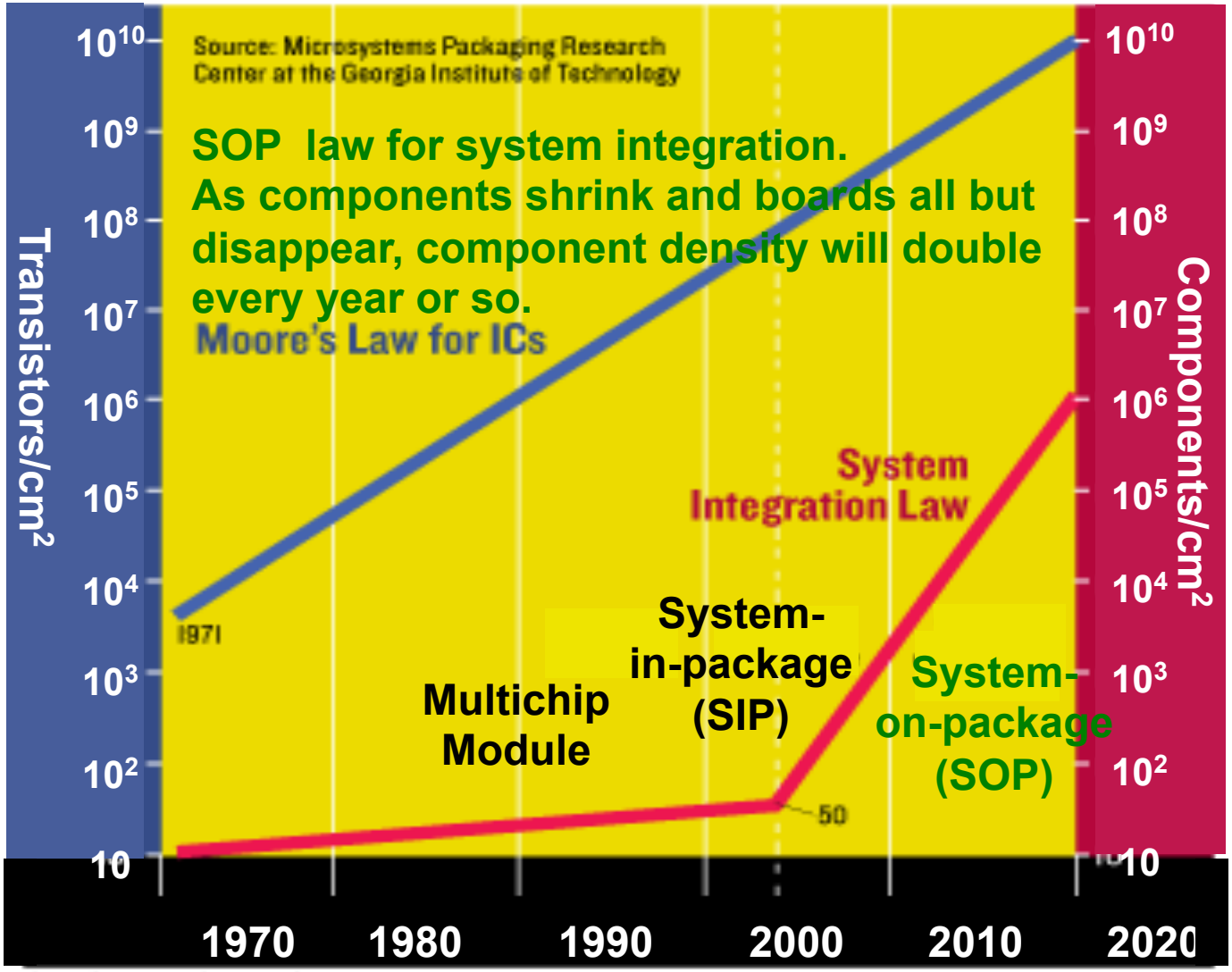
- Components Complement Digital Processing/ Storage Elements in an Integrated System



MicroImplant: An Electronic Platform for Minimally Invasive Sensory Monitors



Semiconductor System Integration – More Than Moore's Law



R. Tummala, "Moore's Law Meets Its Match", IEEE Spectrum, June, 2006

Improvement Trends for VLSI SoCs Enabled by Geometrical and Equivalent Scaling

- TRENDS:
- Higher Integration level
  - exponentially increased number of components/ transistors per chip/package.
- Performance Scaling
  - combination of Geometrical (shrinking of dimensions) and Equivalent (innovation) Scaling.
- System implementation
  - SoC + increased use of SiP -> SOP

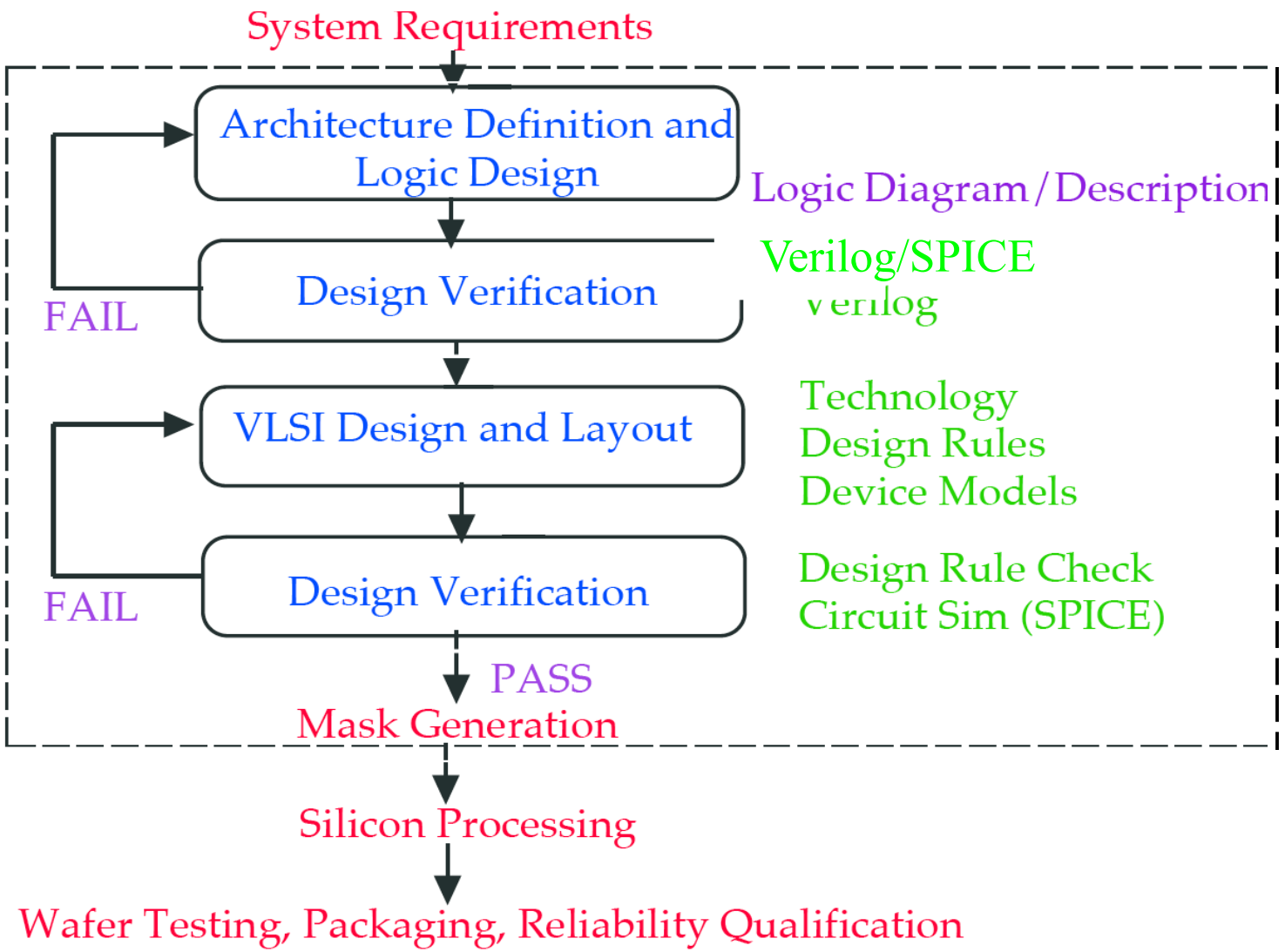
- CONSEQUENCES:
- Higher Speed
  - CPU clock rate at multiple GHz + parallel processing.
- Increased Compactness & less weight
  - increasing system integration.
- Lower Power
  - Decreasing energy requirement per function.
- Lower Cost
  - Decreasing cost per function.

Trends in Practice at ISSCC (HW 1)

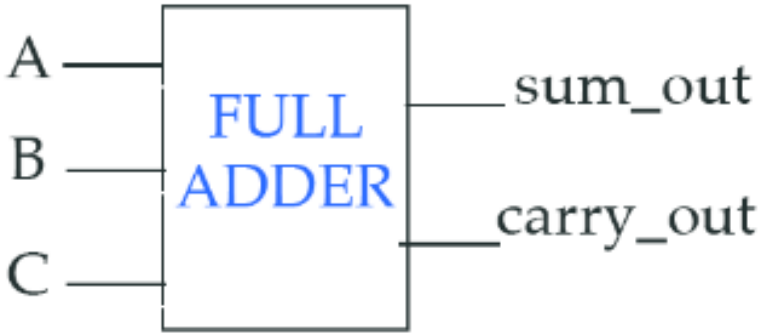
Article Title (IEEE Journal of Solid State Circuits, Volume 52, Issue 1, Feb. 2017)	System application(s) for the chip or system or technology	Fabrication technology description	Minimum feature size	Operating or clock speed	Die size	Most interesting features of the chip or system or technology reported
PROCESSORS, NOC & DIGITAL PLLS	-	-	-	-	-	-
A 0.0021 mm2 1.82 mW 2.2 GHz PLL Using Time-Based Integral Control in 65 nm CMOS; pp 8 - 20						
A 16 nm FinFET Heterogeneous Nona-Core SoC Supporting ISO26262 ASIL B Standard, pp 77 - 88						
ENERGY EFFICIENT DIGITAL	-	-	-	-	-	-
Eyeriss: An Energy-Efficient Reconfigurable Accelerator for Deep Convolutional Neural Networks, pp 127 - 138						
5.6 Mb/mm2 1R1W 8T SRAM Arrays Operating Down to 560 mV Utilizing Small-Signal Sensing With Charge Shared Bitline and Asymmetric Sense Amplifier in 14 nm FinFET CMOS Technology, pp 229 - 239						
MEMORY	-	-	-	-	-	-
A 10 nm FinFET 128 Mb SRAM With Assist Adjustment System for Power, Performance, and Area Optimization, pp 240 - 249						
A 1.2 V 20 nm 307 GB/s HBM DRAM With At-Speed Wafer-Level IO Test Scheme and Adaptive Refresh Considering Temperature Distribution, pp 250 - 260						
TECHNOLOGY DIRECTIONS	-	-	-	-	-	-
Postsilicon Voltage Guard-Band Reduction in a 22 nm Graphics Execution Core Using Adaptive Voltage Scaling and Dynamic Power Gating, pp 50 - 63						
256 Gb 3 b/Cell V-nand Flash Memory With 48 Stacked WL Layers, pp 210 - 217						
IMAGERS, MEMS, MEDICAL & DISPLAYS	-	-	-	-	-	
A 0.6-V, 0.015-mm2, Time-Based ECG Readout for Ambulatory Applications in 40-nm CMOS, pp 298 - 308						
An EEG Acquisition and Biomarker-Extraction System Using Low-Noise-Amplifier and Compressive-Sensing Circuits Based on Flexible, Thin-Film Electronics, pp 309 - 321						

Design Example

VLSI Design Cycle or Flow



Illustrative Circuit Design Example



Input Variables:
addends: A, B
carry-in: C
Output Variables:
sum_out, carry_out

Design a One-Bit Adder Circuit using 0.8 twin-well CMOS Technology. The design specifications are:

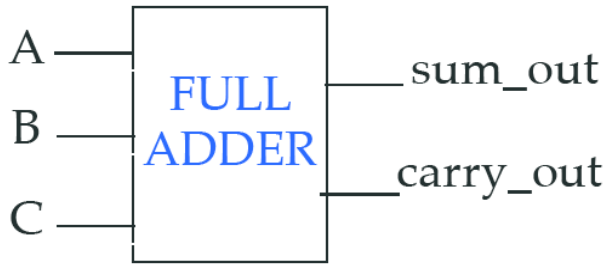
1. Propagation Delay Times of SUM and CARRY_Out signals: ≤ 1.2 ns
2. Rise and Fall Times of SUM and CARRY_Out signals: ≤ 1.2 ns
3. Circuit Die Area: ≤ 1500 um^2
4. Dynamic Power Dissipation (@ V_{DD} = 5 V and f_{max} = 20 MHz): ≤ 1 mW
5. Functional:

$$sum\_out = A \oplus B \oplus C = ABC + A\overline{B}\,\overline{C} + \overline{A}B\overline{C} + \overline{A}\overline{C}B$$

$$carry\_out = AB + AC + BC$$

Illustrative Circuit Design Example

START: Boolean description of binary adder circuit:



A	B	C	sum_out	carry_out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

DEFINE:

Input Variables:

addends: A, B

carry-in: C

Output Variables:

sum_out, carry_out

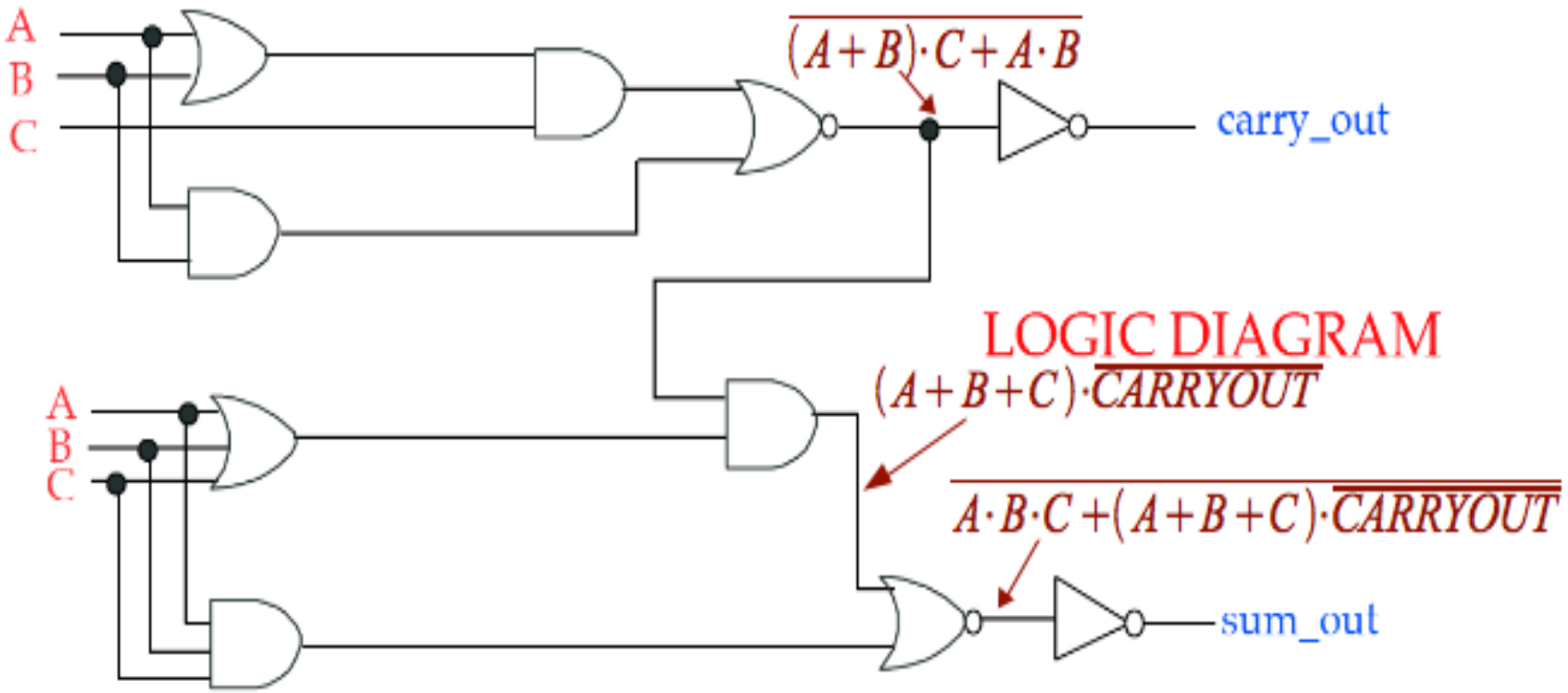
BOOLEAN FUNCTION:

$$\text{sum\_out} = A \oplus B \oplus C = ABC + A\overline{BC} + \overline{AB}C + \overline{AC}B = ABC + (A + B + C)\,\overline{\text{carry\_out}}$$

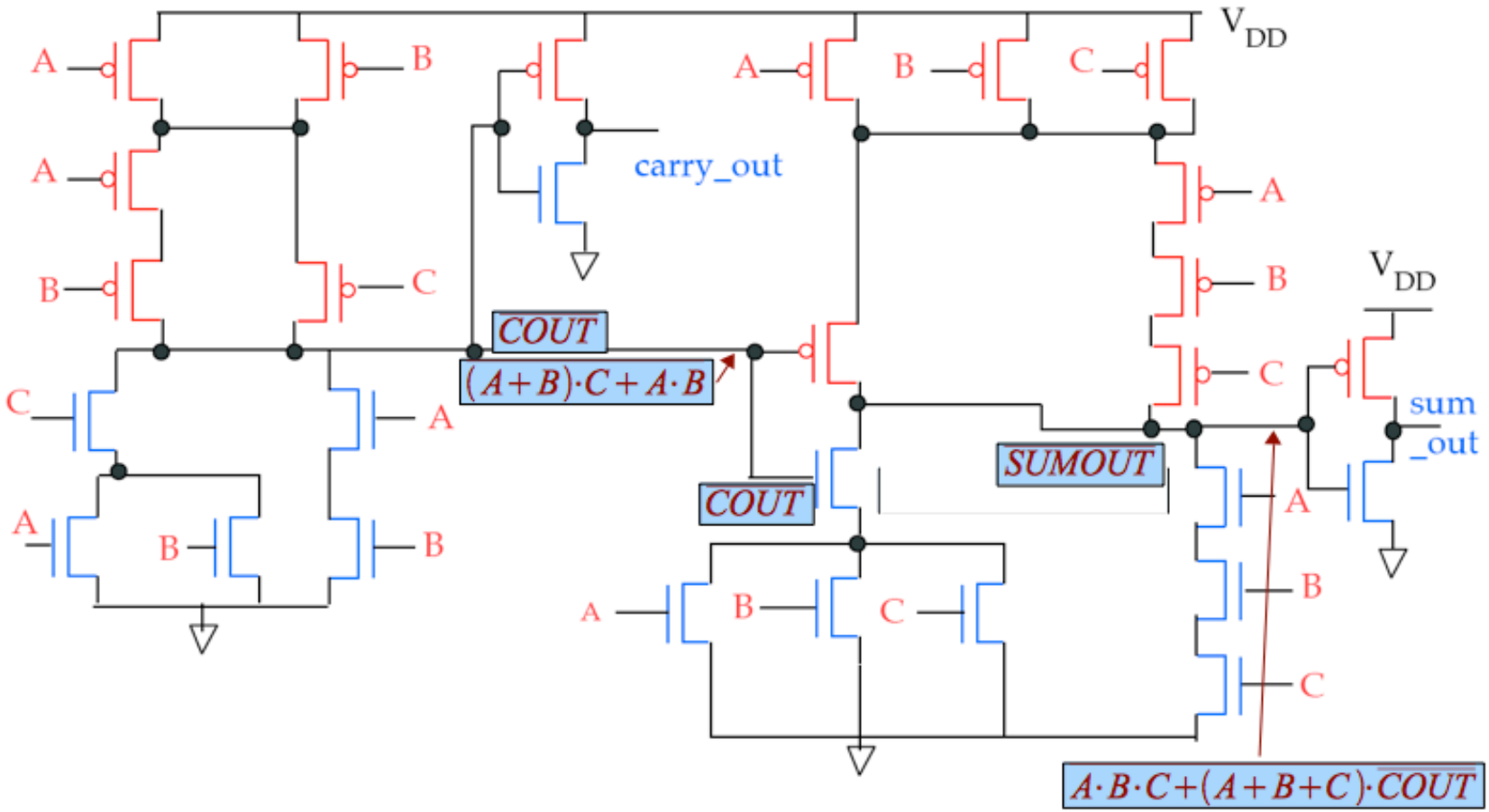
$$\text{carry\_out} + AB + AC + BC$$

Use of carry_out to realize sum_out reduces circuit complexity and die area.

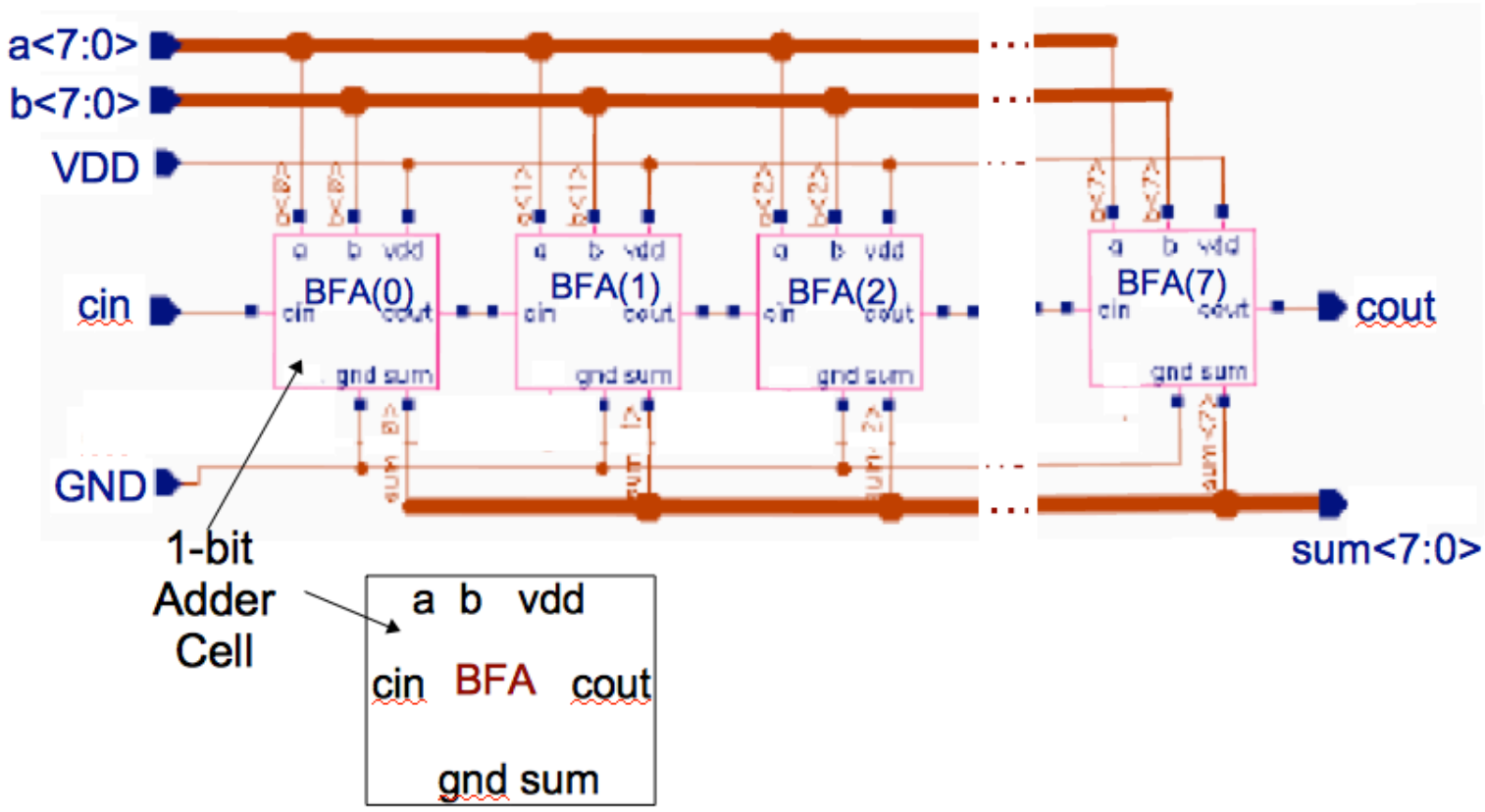
Gate Level Schematic of One-Bit Full Adder Circuit



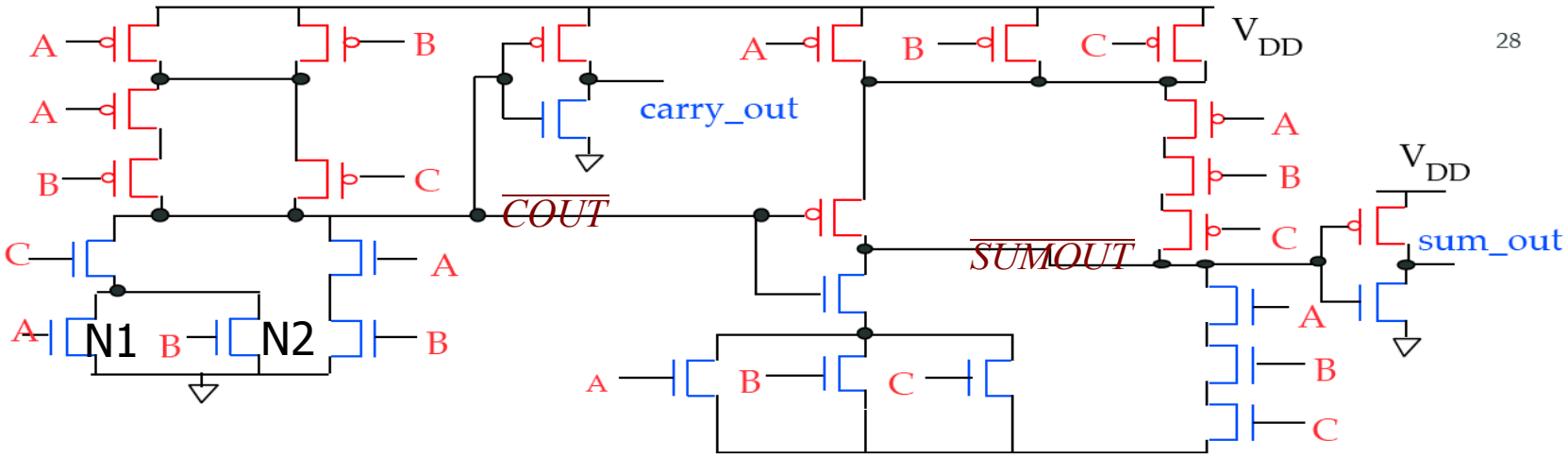
Transistor Level Schematic of One-Bit Full Adder Circuit

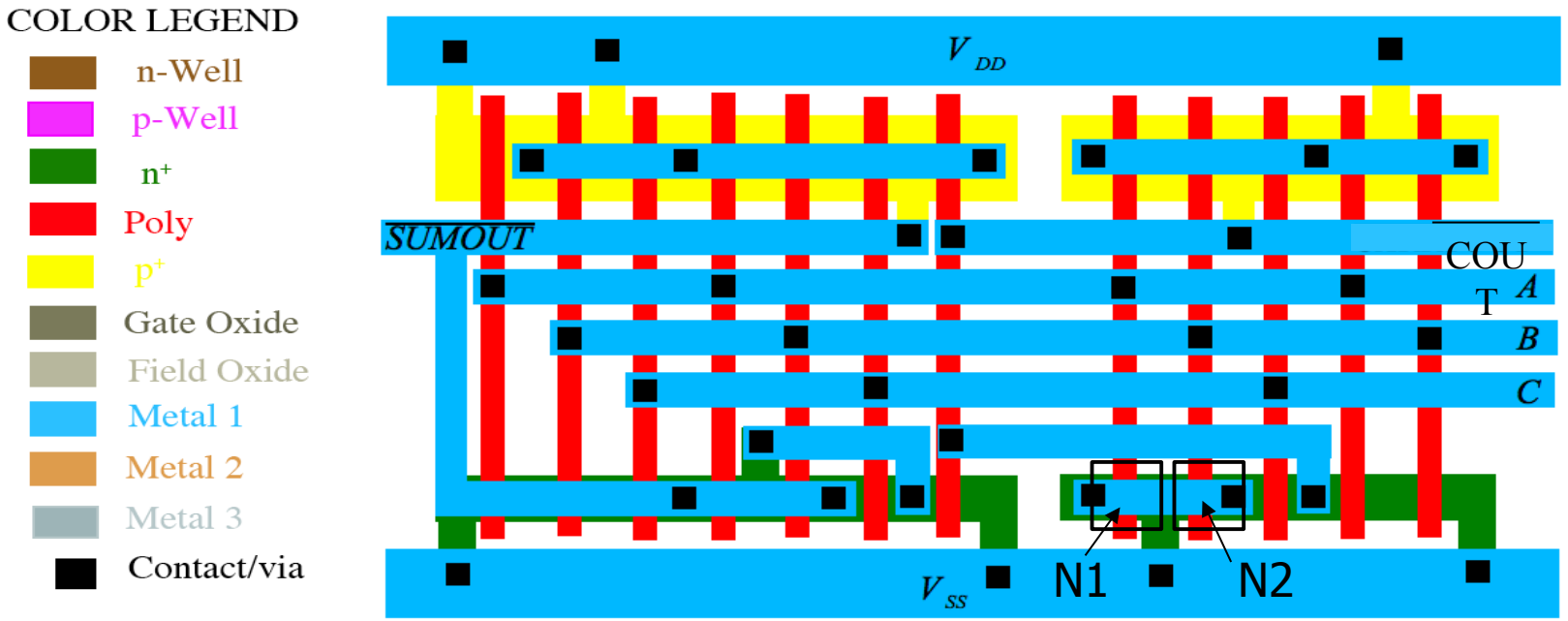


8-bit Ripple Adder

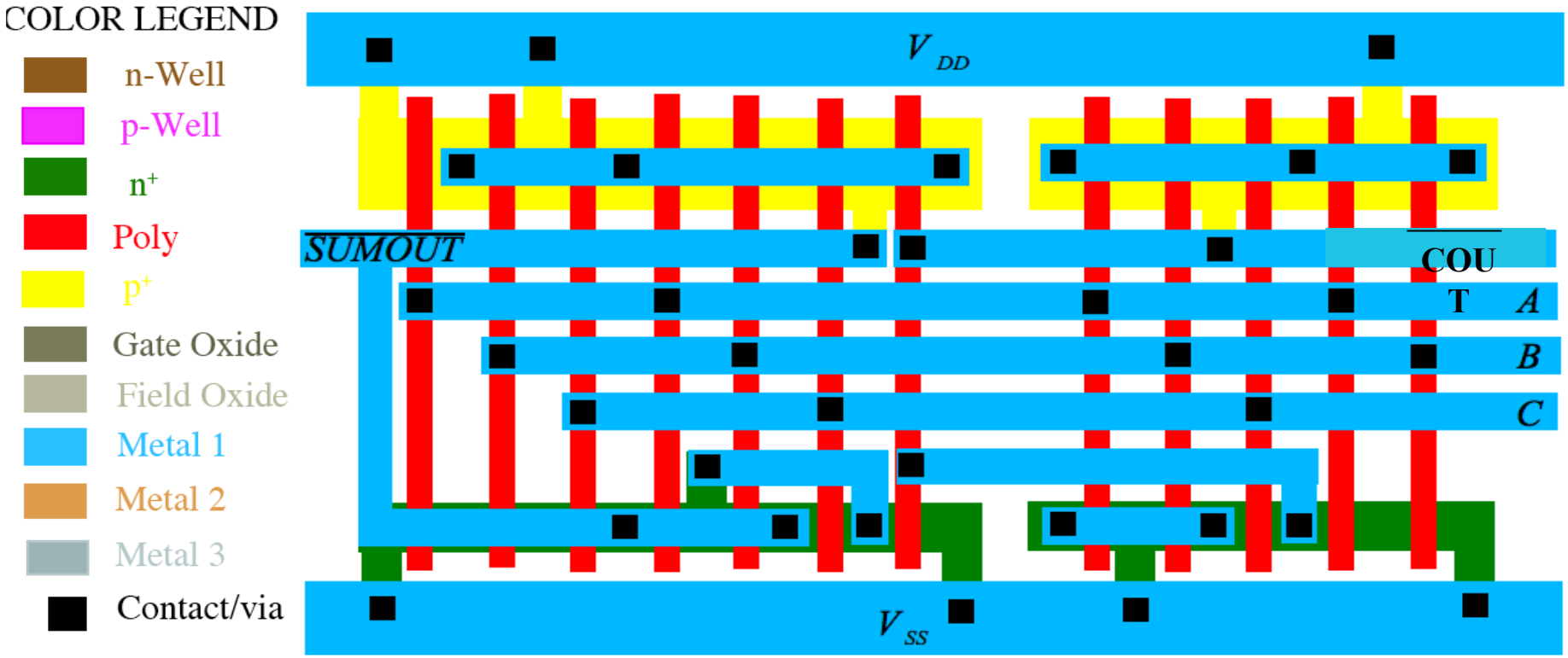


Initial Layout of One-Bit Full Adder Circuit





Initial Layout of One-Bit Full Adder Circuit



Layout with W/L = 2 µm/0.8 µm

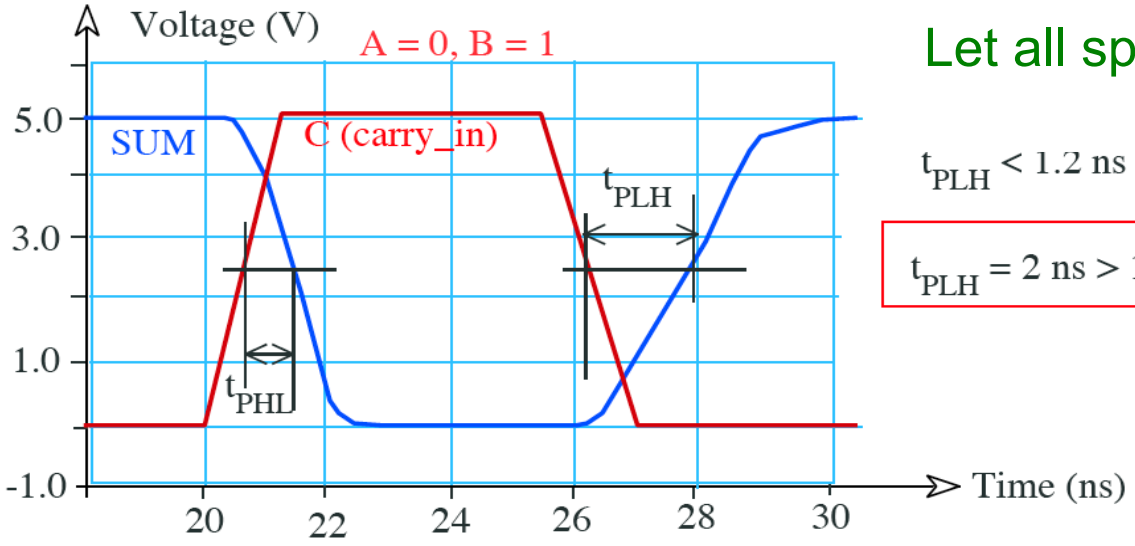
Area 21 µm x 54 µm = 1134 µm^2 ≤ 1500 um^2

Dynamic Power Dissipation (@ V_{DD} = 5V, f_{max} = 20 MHz): = 0.7 mW ≤ 1 mW

Simulated Performance of One-Bit Full Adder Circuit

SPECIFICATIONS:
1. Propogation Delay Times of SUM & CARRY_OUT signals: ≤ 1.2 ns
2. Transition Delay Times of SUM & CARRY_OUT signals: ≤ 1.2 ns
3. Circuit Die Area: ≤ 1500 µm²
4. Dynamic Power Dissipation (@ V_{DD} = 5 V and f_{max} = 20 MHz): ≤ 1 mW

Layout with W/L = 2 µm/0.8 µm



Let all specs be met except t_{PLH}, i.e.

t_{PLH} < 1.2 ns

t_{PLH} = 2 ns > 1.2 ns

Spec NOT met.

Modified Layout Required

1. Increase W/L's of transistors
2. Consider more compact placement of transistors and reduce interconnect in critcal paths

Wrap up

- Admin
  - Find web, get text, assigned reading…
  - http://www.seas.upenn.edu/~ese570
  - https://piazza.com/upenn/spring2017/ese570/
  - https://canvas.upenn.edu/
- Big Ideas/takeaway
  - Model (a.k.a. analysis and simulation) to enable real-life design
- Remaining Questions?