Interconnection Networks for Parallel and Distributed Processing: An Overview

CURRENT integrated circuit technology is making feasible computer systems consisting of hundreds or thousands of processors. One of the most difficult problems in the design of large-scale parallel and distributed computer systems is the choice of a communications network. An efficient method is needed for linking the system's processors, memories, and other devices to each other. As can be observed from the papers in this Special Issue, there are many different approaches to the solution of this problem. The best "solution" for a particular system is a function of the system's intended applications, size, speed requirements, cost constraints, etc.

The topic of this Special Issue spans the "traditional" categories of computer architecture, computer communications, distributed computing, and parallel processing. Furthermore, a variety of aspects of interconnection networks are considered here, from a network's mathematical graph theoretical basis to a network's VLSI implementation.

The emphasis of the papers in this Special Issue is on local interconnection networks which could, conceptually, fit in a single room and could connect a very large number of processors. The two basic types of approaches explored are shared bus networks (e.g., tree, hypercube, Chordal Ring) and multistage networks (e.g., omega, banyan, delta). The methods used to evaluate the networks include both mathematical analyses and simulation studies. The impact of VLSI technology on network implementation is also examined.

The use and VLSI implementation of the binary tree as an interconnection network is described in the paper by Horowitz and Zorat. An algorithm for mapping an arbitrary binary tree onto the plane is presented and analyzed in terms of the amount of chip area required. The problem of routing information among the nodes of the tree in an environment where some nodes may be faulty is investigated. The average message handling capacity of the binary tree is compared to that of the linear array and the square grid interconnection schemes.

In the paper by Wu and Liu, a cluster structure is proposed as a conceptual interconnection scheme for large multiprocessor systems. A cluster structure is a hierarchical organization with levels of subclusters. By specifying various structural parameters, different networks can be modeled. Examples of networks which authors consider as special cases of cluster structures are the hypercube and tree. The problems of traffic congestion and message delay for three cluster networks (e.g., omega, banyan, delta) are presented. The methods used to evaluate the networks include both mathematical analyses and simulation studies. The impact of VLSI technology on network implementation is also examined.

In the paper by Wirsching and Kishi describes a simulation program called CONET, used for studying interconnection properties of the omega network and the control algorithm for the omega network more than once. A multiple-pass control algorithm which is adaptive and fail-soft is presented.

A pi network, which is a concatenation of two omega networks, is proposed by Yew and Lawrie in their paper. The omega network is a multistage interconnection network in the same family as the SW-banyan and delta discussed above. This paper is concerned with the data permuting capability of a network, i.e., the ability to connect, in a one-to-one fashion, all inputs to all outputs simultaneously. In order to perform certain permutations, data must be passed through the omega network more than once. A multiple-pass control algorithm for the omega is presented and applied to the pi network. Various properties of the pi network and the control algorithm are described.

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