VLSI Designs for Low Power Applications

Deepak Kumar

Electronics & Communication Dept.

Rama University, Kanpur, India

Deepakpatel03@gmail.com

Naveen Tiwari

Electronics & Communication Dept.

Rama University, Kanpur, India

Naveentiwari555@gmail.com

Abstract— **Low power has emerged as a principal theme in today's world of electronics industries. Power dissipation has become an important consideration as performance and area for VLSI Chip design. With shrinking technology reducing power consumption and over all power management on chip are the key challenges below 100nm due to increased complexity. For many designs, optimization of power is important as timing due to the need to reduce package cost and extended battery life. For power management leakage current also plays an important role in low power VLSI designs. Leakage current is becoming an increasingly important fraction of the total power dissipation of integrated circuits. This paper describes about the various strategies, methodologies and power management techniques for low power circuits and systems. Future challenges that must be met to designs low power high performance circuits are also discussed**.

Keywords——*Power Dissipation, low power, process nodes, leakage current, power management.*

I.   INTRODUCTION

The advantage of utilizing a combination of low-power components in conjunction with low-power design techniques is more valuable now than ever before. Requirements for lower power consumption continue to increase significantly as components become battery-powered, smaller and require more functionality. In the past the major concerns for the VLSI designers was area, performance and cost. Power consideration was the secondary concerned. Now a day's power is the primary concerned due to the remarkable growth and success in the field of personal computing devices and wireless communication system which demand high speed computation and complex functionality with low power consumption. The motivations for reducing power consumption differ application to application. In the class of micro-powered battery operated portable applications such as cell phones, the goal is to keep the battery lifetime and weight reasonable and packaging cost low. For high performance portable computers such as laptop the goal is to reduce the power dissipation of the electronics portion of the system to a point which is about half of the total power dissipation. Finally for the high performance non battery operated system such as workstations the overall goal of power minimization is

to reduce the system cost while ensuring long term device reliability. For such high performance systems, process technology has driven power to the fore front to all factors in such designs. At process nodes below 100 nm technology, power consumption due to leakage has joined switching activity as a primary power management concern. There are many techniques [1] that have been developed over the past decade to address the continuously aggressive power reduction requirements of most of the high performance. The basic low-power design techniques, such as clock gating for reducing dynamic power, or multiple voltage thresholds (multi-Vt) to decrease leakage current, are well-established and supported by existing tools [2]. From figure 1 we can analyze how many changes takes place in circuit design using power dissipation [1].
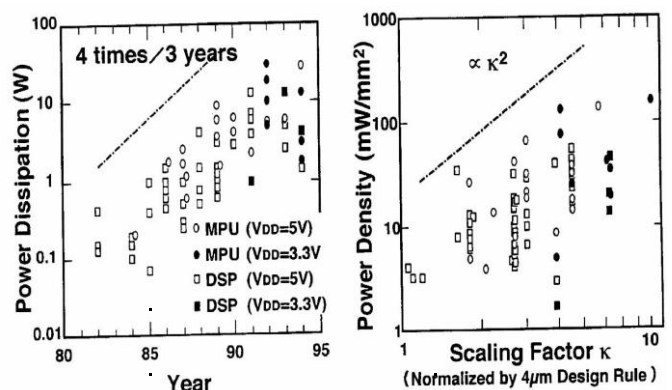

Fig.1.Evolution in Power dissipation [15]

II.   LOW POWER STRATEGIES

There (table-I) are different strategies available at different level in VLSI design process for optimizing the power consumption.
Effective power management is possible by using the different strategies at various levels in VLSI Design process. So designers need an intelligent approach for optimizing power consumptions in designs

Design Level	Strategies
Operating System Level	Portioning, Power down
Software level	Regularity, locality, concurrency
Architecture level	Pipelining, Redundancy, data encoding
Circuit/Logic level	Logic styles, transistor sizing and energy recovery
Technology Level	Threshold reduction, multi threshold devices

III.   POWER DISSIPATION BASICS

In a circuit three components are responsible for power dissipation: dynamic power, short-circuit power and static power. Out of these, dynamic power or switching power is primarily power dissipated when charging or discharging capacitors and is described below [3, 4]:

$$P_{dyn} = C_L \, Vdd^2 \, \alpha \, f \qquad (1)$$

Where C_L: Load Capacitance, a function of fan-out, wire length, and transistor size, Vdd: Supply Voltage, which has been dropping with successive process nodes, α: Activity Factor, meaning how often, on average, the wires switch, f: Clock Frequency, which is increasing at each successive process node. Static power or leakage power is a function of the supply voltage (Vdd), the switching threshold (Vt), and transistor sizes (figure2). As process nodes shrink, leakage becomes a more significant source of energy use, consuming at least 30% of total power [5]. Crowbar currents, caused when both the PMOS and NMOS devices are simultaneously on, also contribute to the leakage power dissipation [2]. Most circuit level minimization techniques focus only on Sub threshold leakage reduction without considering the effects of gate leakage [1] .For this MTCMOS scheme [6] has been proposed for reduction of sub threshold leakage current in sleep mode. Figure-2 shows the various components responsible for power dissipation in CMOS.
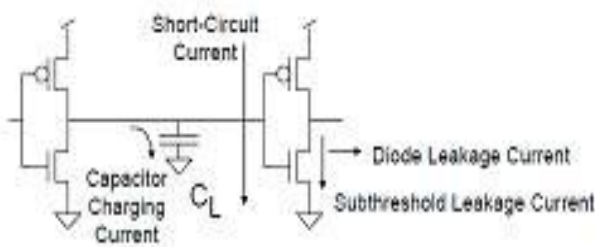

Fig.2. Power Dissipation in CMOS [6]

IV.   LOW POWER DESIGN SPACE

From the above section it is revealed that there are three degrees of freedom in the VLSI design space: Voltage, Physical Capacitance and data activity. Optimizing for more power entails an attempt to reduce one or more of these factors. This section briefly describes about their importance in power optimization process.

1) *Voltage:*
Because of its quadratic relationship to power , voltage reduction offers the most effective means of minimizing power consumption. Without requiring any special circuits and technologies, a factor of two reduction in supply voltage yields a factor of four decreases in power consumption. Unfortunately, there is speed penalty for supply voltage reduction and delays drastically increase as Vdd approaches to the threshold voltage Vt of the device. The approach to reduce the supply voltage without loss in throughput is to modify the threshold voltage of the devices. Reducing the Vt allows the supply voltage to be scaled down without loss in speed.The limit of how low low the Vt can go is set by the reqirement to set adequate noise margins and control the increase in the subtreshold leakage current [4,7,8].

Traditional Techniques	Dynamic Power Reduction	Leakage power reduction	Other Power reduction Techniques
Clock Gating	Clock Gating	Minimize usage of low Vt cells	Multi Oxide devices
Power Gating	Power Efficient Techniques	Power Gating	Minimize capacitance
Variable Frequency	Variable Frequency	Back Biasing	Power circuits
Variable Voltage Supply	Variable Voltage Supply	Reduce Oxide Thickness	
Variable Device Threshold	Variable Island	Use Fin FET	

2) *Physical Capacitance:*
Dynamic power consumption depends linearly on the physical capacitance being switched. So, in addition to operating at low voltages, minimizing capacitances offer another technique for minimizing power consumption. The capacitances can be kept at a minimum by using less logic, smaller devices , fewer and shorter wires[4,7,8]. As with voltage, however, we are not free to optimize capacitances independently, for example reducing device sizes reduces physical capacitance, but it also reduces the current drive of the transistor making the circuit operate more slowly.

1) *Switching Activity:* There are two components to switching activity : F_{clk} which determines the average

periodicityof data arrivals and E(sw) which determines how many transitions each arrival will generate[9]. E(sw) is reduced by selecting proper algorithms architecture optimization, by proper choice of logic topology and by logic level optimization which results in less power[1]. The data activity E(sw) are combined with the physical capacitance C to obtained switch capacitance $C_{sw}=C.E(sw)$,which describes the average capacitance charge during each data period1/Fclk which determines the power consumed by CMOS circuit[10].

V. POWER MINIMIZATION TECHNIQUES

This section addresses (table-2) the different approaches to minimize the power at different levels:

1) *Reducing Chip and package capacitance:*
This can be achieved through process development such as SOI with partially or fully depleted wells, CMOS scaling to submicron device sizes and advanced interconnect substrates such as multi chip module (MCM). This approach can be very effective but is also very expensive [1, 11].

2) *Scaling the supply voltage (Voltage Scaling):-*
This approach can be very effective in reducing the power dissipation, but often requires new IC fabrication processing [14].

3) *Using power management strategies:*
Effective power management involves selection of the right technology, the use of optimized libraries, IP (intellectual property), and design methodology [13, 11]. Figure-3 shows the effective power management strategy.

a) *The Role of Technology Selection:*
Proper technology selection is one of the key aspects of power management [13]. The goal of each technology advancement is to improve performance, density, and power consumption. The typical approach in developing a new generation of technology is to apply constant-electric-field scaling. Process designers scale both the applied voltage and the oxide thickness to maintain the same electric field [12, 15]. This approach reduces power by about 50% with every new technology node However, as the voltage gets smaller, the threshold voltage also must scale down to meet the performance targets of that technology. This scaling unfortunately increases the sub threshold current and hence the leakage power. To overcome this constraint, process engineers no longer apply constant-field scaling for processes of 65 nm or smaller; instead, they used a more generalized form of scaling. Because it is impossible to optimize a technology for both performance and leakage at once, each technology usually has two variants. One variant aims for high performance, and the other shoots for low leakage. The primary differences between the two are in the oxide thickness, supply voltage, and threshold voltage. The technology variant with the thicker gate oxide aims for low-leakage design and must support a higher voltage to achieve a reasonable performance [10]. When selecting a technology to optimize the power for a given design, you must take both aspects into consideration: the need to use a smaller geometry to reduce active power and the need to use a low-leakage
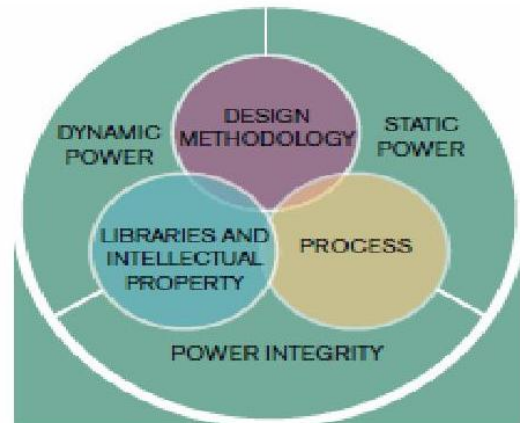
variant to reduce leakage.

Fig.3. Technology selection for [9] effective power management

b) *Circuit-Design Techniques:*
After selecting technology, the focus is on design techniques to optimize power. (Figure 5). One has to start by selecting the appropriate logic gate from the standard cell library. Each gate in a standard cell library uses the smallest transistors and has multiple versions with different drive strengths, sizes, delays, multiple-threshold voltage and power consumption. Because the main parameter for controlling active power is the power-supply voltage, cell designers typically design and characterize the gates to operate at voltages as much as 30% lower than the power-supply voltage [15]. Lowering the power-supply voltage produces smaller currents, resulting in more delay. However, this slowdown is acceptable if the design is not pushing the edges of a given technology. Increasing the threshold voltage reduces the leakage current in the device. Leakage power also controlled by designing logic gates with multiple-threshold-voltage devices [15], including standard high and low threshold voltage devices. Figure-4 shows the variation of gate delay Vs leakage power.

c) *CAD Methodologies and Technique:*
Today's EDA tools effectively support these power-management techniques [16]. They also provide additional power savings during implementation. Low power VLSI designs can be achieved at various levels of the design abstraction from algorithmic and system levels down to layout and circuit levels.

d) *Low Power management in Physical Design:*
Physical design tools interpret the power intent and implement the layout correctly, from placement of special cells to routing and optimization across power domains in the presence of multiple corners, modes, and power states, plus manufacturing variability [5, 16]. An increasingly common technique to reduce power in physical design is the use of multiple voltage islands (domains), which allows some blocks to use lower supply voltages than others, or to be completely shut off for certain modes of operation [4].Clocks are a significant source of dynamic power usage. Low-power clock tree synthesis (CTS) strategies [3, 4] include lowering overall capacitance and minimizing switching activity to achieve power saving
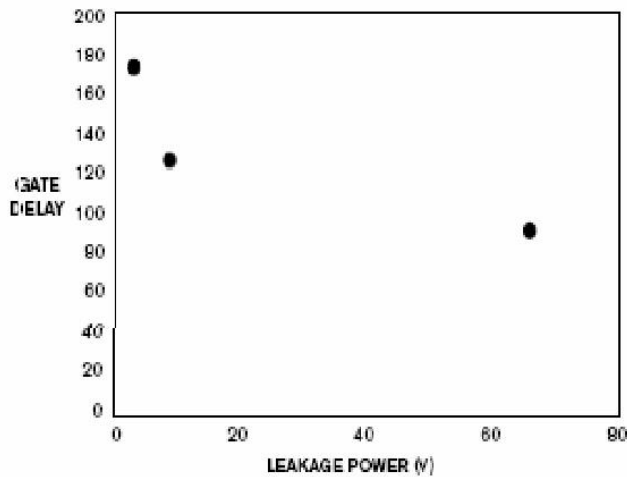
Fig.4. Trade off between leakage and Power

However, getting the best power results from CTS depends on the ability to synthesize the clocks for multiple corners and modes concurrently in the presence of design and manufacturing variability, and in multi-voltage flows [7]. Power gating technique is effective for reducing leakage power by temporarily turned off the circuit [17, 7].

This temporary shutdown time can also call as "low power mode" or "inactive mode". When circuit blocks are required for operation once again they are activated to "active mode". Shutting down the blocks can be accomplished either by software or hardware. Now-a-days a dedicated power.

management controller is used for this purpose [17]. Table-3 gives the trade-off associated with the various power management techniques [17].

TABLE III.   TRADE OFF ASSOCIATED WITH POWER MANAGEMENT TECHNIQUES

Power Reduction Technique	Power Benefit	Timing Penalty	Area Penalty	Methodology Impact			
				Architecture	Design	Verification	Implementation
Multi Vt optimization	Medium	Little	Little	Low	Low	None	Low
Clock Gating	Medium	Little	Little	Low	Low	None	Low
Multi supply voltage	Large	Some	Little	High	Medium	Low	Medium
Power Shut off	Huge	Some	Some	High	High	High	High
Dynamic and adaptive Voltage frequency scaling	Large	Some	Some	High	High	High	High
Substrate Biasing	Large	Some	Some	Medium	None	None	High

VI.   CONCLUSION

The need for lower power systems is being driven by many

market segments. Unfortunately designing for low power adds another dimension to the already complex design problem and the design has to be optimized for power as well as Performance and Area. In conclusion various issues and major challenges regarding low power designs are:-

1) *Technology Scaling:-*
It relates with the following factors like: Capacitance per node reduces by 30%, Electrical nodes increases by 2X, Die size grows by 14% (Moore's Law), Supply Voltage reduces by 15% and Frequency Increases by 2X. To meet these issues relatively 2.7 X active power will increase.

2) *Leakage power:*
 To meet frequency demand Vt will be scaled which results high leakage power. A low voltage / low threshold technology and circuit design approach, targeting supply voltage around 1V and operating with reduced thresholds.

3) Dynamic power management techniques:
 Varying supply voltage and execution speed according to the activity measurement.

4) Low power interconnect:
using advance technology, reduced swing or activity approach.

5) Development of power:
Development of power conscious techniques and tools for behavioral synthesis, logic synthesis and layout optimization.

6) Power saving techniques
Power saving techniques that recycle the signal energies using the adiabatic switching principals rather them dissipating them as a heat and promising in certain applications where speed can be trades for low power.

REFERENCES

[1]   Rahul. M.Rao, Jeffery L.Burns, Richard B.Brown, "Circuit Techniques for gate and subthreshold leakage minimization in future CMOS technologies" Proc. ISLPED, pp70-73, 2002.
[2]   Prasad Subramanian, "Power management for optimal power design", ESILICON, Corp.2010.
[3]   Shekar Borkar, "Design Challenges of Technology Scaling," *IEEE Micro*, July/August 1999, pg 23.
[4]   T. Inukai, et.al, "Boosted Gate MOS (BGMOS): Device/Circuit Cooperation Scheme to Achieve Leakage-Free Giga- Scale Integration," Proc. CICC 2000, pp.409-412.
[5]   Creating Low-Power Digital Integrated Circuits The Implementation Phase, Cadence, 2007.
[6]   Glasser, Lance A, and Daniel W Dobberpuhl, *TheDesign and Analysis of VLSI Circuits*, Addison-Wesley Publishing Co, 1985.
[7]   Y. Yeo, et.al, "Direct Tunneling Gate Leakage Current in Transistors with Ultrathin Silicon Nitride Gate Dielectric," IEEE Electron Devices Letters, vol.21, no.11, pp. 540-542, Nov.2000.
[8]   M.Alidina, j. Monterio, S. Devadas, A.Ghosh and M. Papaefthymiou. "Precomputation –based Sequential logic optimization for low power" In Proceedings of the 1994 International Workshop on Low Power Design, pages 57-62, April 1994.
[9]   Mentor Graphics, "Low power physical design with Olympus SOC", Place and route white paper, March 27, 2009.
[10]   S. Mutoh, et.al, "1-V Power Supply High-Speed Digital Circuit Technology with Multi-Threshold Voltage CMOS,"IEEE Journal of Solid State Circuits, vol. 30, no. 8, pp. 847-854, Aug. 1995.

[11] F.Hamzaoglu and M. Stan, "Circuit-Level Techniques to Control Gate Leakage for sub 100nm CMOS," Proc. ISLPED, pp. 60-63, Aug. 2002.

[12] B.Perman, "Design technologies for VLSI design", encyclopedia of computer science,1995.

[13] Michael Keating, David Flynn, Robert Aitken, Ala Gibsons and Kaijian Shi, "Low Power Methodology Manual for System on Chip Design", Springer Publications, New York, 2007.

[14] J.kao, Siva Narendra, Ananta Chandra Kasan, "Subthresh leakage modeling and reduction technique", 2002.

[15] Liu, Weidong, Xiaodong Jin, Xuemei Xi, James Chen, Min-Chie Jeng, Zhihong Liu, Yuhua Cheng, Kai Chen, Mansun Chan, Kelvin Hui, Jianhui Huang, Robert Tu, Ping K Ko, and Chenming Hu, *BSIM3v3.3 MOSFET Model User's Manual*, Department of Electrical Engineering and Computer Sciences, University of California-Berkeley, 2005.

[16] Anand Iyer, "Demystify power gating and stop leakage cold", Cadence Design Systems, Inc.

[17] De-Shiuan Chiou, Shih-Hsin Chen, Chingwei Yeh, "Timing driven power gating", Proceedings of the 43rd annual conference on Design automation,ACM Special Interest Group on Design Automation, pp.121 - 124, 2006.