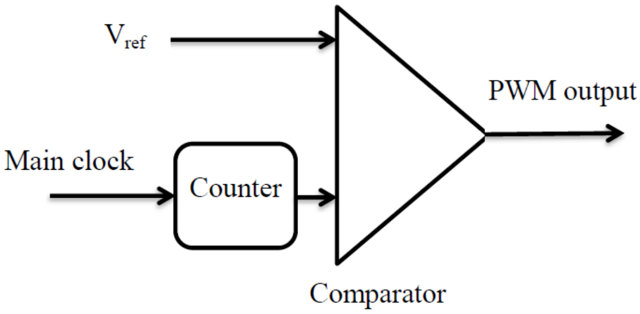

Figure 3: Block diagram of PWM Generator

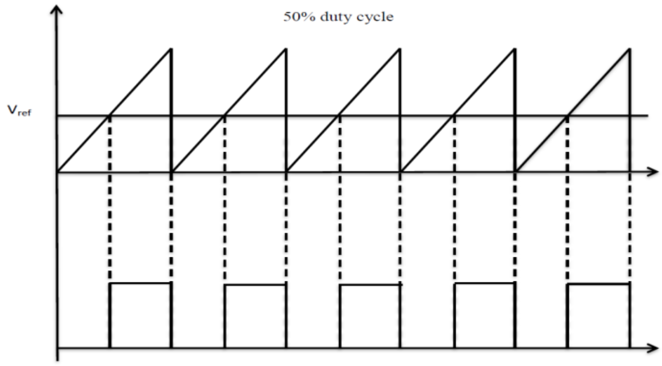

Figure 4(a): PWM with 50% duty cycle

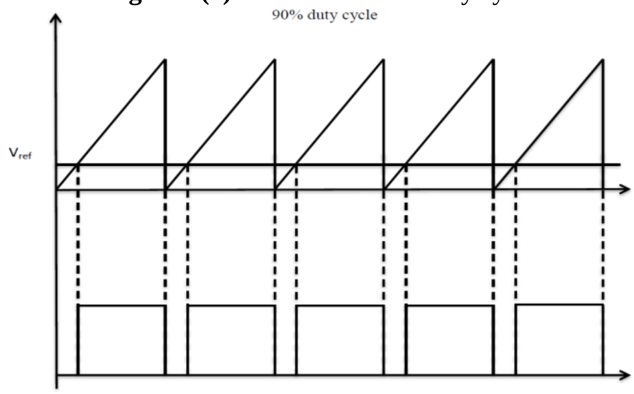

Figure 4(b): PWM with 90% duty cycle

3.4 Clock Manager

The clock frequency of the FPGA is very high, this makes the working of the motor difficult. Also, it is not easy to include an external clock to the circuit due to the increase in the complexity. Hence, the system clock, with the help of a clock divider circuit is utilized to produce the required clock frequency for the functioning of the motor.

3.5 Sigma-Delta ADC

The Sigma-Delta ADC utilizes the Sigma-Delta modulation noise shaping property and oversampling techniques to allow high-resolution conversion [11]. The noise shaping property places most of the quantization noise in the high frequency range to minimize the in-band noise. The noise shapes depends on the order of the modulator. The block diagram for the second order Sigma-Delta ADC is shown in Figure 5.

The second order Sigma-Delta ADC provides better noise shaping characteristics compared to the first order modulator. Higher order modulator allows high in-band noise reduction. But, single loop single-bit modulators higher than two have some instability issues.

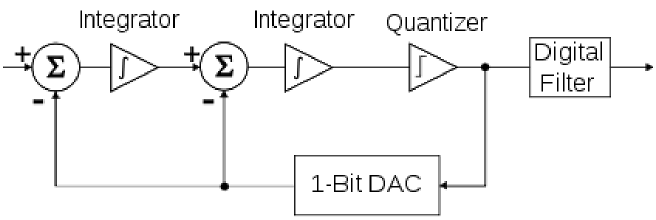

Figure 5: Block Diagram of Second order Sigma-Delta ADC

4. Results and Discussion

The forward loop of the PID controller based motor control system basically consists of three main blocks PID controller, a PWM Generator and a clock manager. Initially the coding for the individual block was completed and then all the modules were combined by using the structural modeling. Simulation is carried out using Xilinx ISim simulator and then synthesis is done using Xilinx ISE 14.2. The RTL schematic view of the PID controller based motor control system is shown in Figure 6.

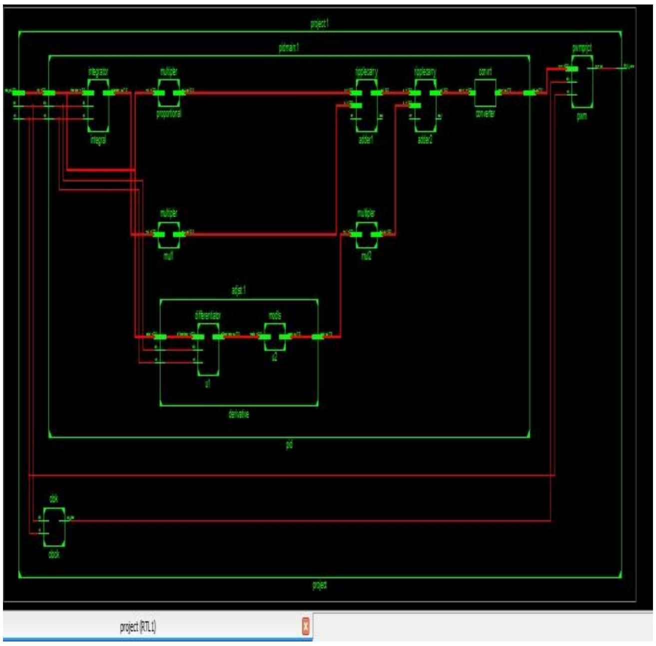

Figure 6: RTL-Schematic of Motor Control System

The simulation result of the PID controller based motor control system is shown in Figure 7. The speed of the motor is continuously monitored using a sensor, whose output is an analog voltage signal. The voltage signal is then converted into corresponding digital signal by Sigma-Delta ADC. Here, the input to the PID controller is the digitized feedback signal from Sigma-Delta ADC.

The PID controller uses the feedback signal for calculating its proportional, integral and derivative responses. This control signal from the PID controller will help to generate the PWM wave with the help of PWM Generator. The output of the simulation is a PWM wave. It helps to drive the motor accordingly.

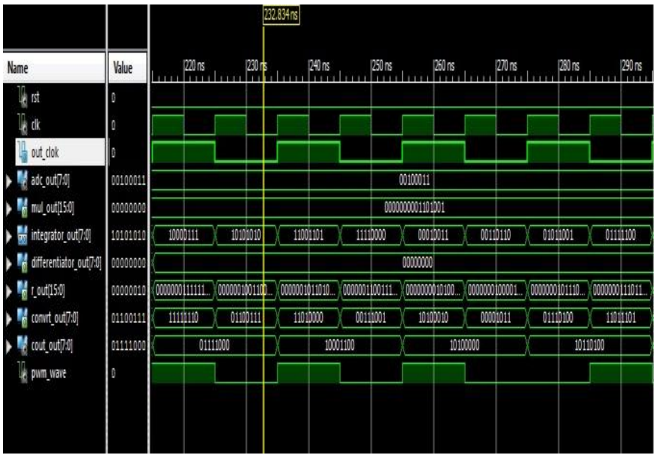

Figure 7: Simulation Result of Motor Control System

5. Conclusion

The FPGA based motor control system using PID controller and Sigma-Delta ADC has been introduced. The practical disadvantages found in the case of other controllers are solved by using this control system. The PID controller system continuously checks and corrects the speed of the motor by taking proportional, integral and derivative responses of the error signal measured from the output and the desired set points. The use of Sigma-Delta ADC in the feedback section provides high resolution and accurate conversion. The role of the FPGA is to acquire the data about the speed from the sensor through the ADC and generate control signals to the actuator after processing of acquired data. Implementation in FPGA improves the speed, accuracy, ease of design and cost effectiveness.

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