Low Power CNTFET- Based Ternary Full Adder Cell for Nanoelectronics

SeyyedAshkanEbrahimi, Peiman Keshavarzian,SaeidSorouri,MahyarShahsavari

Abstract*—In a VLSI circuit, about 70 percent of area occupies by Interconnection. Such a large number of area occupation leads to many limitations of fabricating and applying in binary circuit implementation. Multiple-valued logic is one of the most proper way to improve the ability of value and data transferring in binary systems. Nowadays as small portable devices consuming are largely increased, applying low power approaches are considerably taking into account. In this paper we suggest and evaluate a novel low power ternary full adder cell which is built with CNTFETs (Carbon Nano-Tube Field Effect Transistors). Using beneficial characteristics of CNTFET in our design and implementation notably increased the efficiency of this adder cell. Simulation results using HSPICE are reported to show that the proposed TFA (ternary full adder) consume significantly lower power and impress improvement in term of the power delay product compare to previous work.

***Index Terms*— CNTFET, Low Power,Nanoelectronic, Ternary Full Adder, Ternary Logic.**

I. INTRODUCTION

According to Moore's law the number of transistors on a chip will be doubled about every two years. For this purpose we have to shrink the size of the transistor into nano-scale region. Due to the limitations of silicon based Field Effect Transistors (FETs), finding a proper alternative is important. As transistors are scaled down to nanometer, a number of nano-scale material such as carbon nanotubes have been proposed as a replacement for silicon base devices. To find a replacement for the CMOS technology many devices and techniques are considered by researchers, such as Quantum-dot Cellular Automata (QCA), spin-wave architecture, Single electron devices, Quantum computing, etc. Carbon NanoTube Field Effect Transistor (CNTFET) is one of the emerging elements of nanoelectronic that has the better performance than all the state-of-the-art emerging technology. Nanotechnology is a new field of research that cuts across many fields - electronics , chemistry , physics ,and biology, that analyzes and synthesizes objects and stnictures in the nano scale (10^{-9} m)such as nanoparticles, nanowires, and Carbon Nano-Tubes (CNTs). CNT is one of the several cutting-edge emerging technologies within nanotechnology that is showing high efficiency and very wide range of

applications in many different streams of science and technology. Examples of such applications are: (1) TVs based on field-emission of CNTs that consume much less power, thinner, and much higher resolution than the best plasma-based TV available, and (2) nanocircuits based on CNTs such as CNT Field Effect Transistors (CNTFETs) that show big promise of consuming less power and to be much faster than the available silicon based FETs.

In the latest decade many works were presented in Multiple-Valued Logic (MVL). By using MVL we achieve a high circuit density and we can perform complex operation with less interconnection problems. Ternary logic has attracted due to its potential benefits over binary logic for the design of digital systems. For instance, it is possible for ternary logic to attain simplicity and savings in energy in digital design since the logic reduces the complexity of interconnects and reduce the number of the transistors. Researchers describe two types of Multiple-Valued logic circuits, current-mode and voltage-mode [1],[2]. In voltage-mode ternary logic, three voltage levels (low, intermediate and high) are represented by '0', '1' and '2' respectively. MVL voltage-mode circuit designs should use transistors with different threshold voltage. In CNTFET circuit designs, transistors with different threshold voltage will be achieved by controlling CNT diameters.

In the previous works there are many techniques which are demonstrated for implementing MVL circuits, based on CNTFET. Ternary logic designs base on CNTFETs in combination with the resistors, have been proposed in [3]. Using resistors will be increased power dissipation and chip area, also permanent pull-up path result in the worse power consumption. Combination of the resistors and the CNTFETs will encounter the worse performance in our circuit designs. The previous work [4], using multi-threshold CNTFETs and a resistor network to implementing logical circuit. A circuit design [5], uses a complete model technique [6] and utilizes two power supplies for implementing multiple-valued logic circuits. Two power supplies will be encountered more wiring and interconnections compared to the other techniques. Another technique based on multiple-threshold CNT-transistors has been proposed in [7]. In this design, resistors are eliminated and they used a CNTFET network with different CNT diameters to obtain different threshold voltage which can perform the expected operation. The high speed full-adder base on CNTFETs, which is proposed in [8], presented the full-adder circuits by the combination of the inverter and capacitors. Using capacitors to present expected behavioral (full-adder), will be increased the delay, chip area and also less noise margin. Ternary arithmetic circuits such as Half-adder and Multiplier have been proposed in [9]. In mentioned paper they used common logic gates to implement their circuit designs; also they used decoders to recognize the inputs. Any function can be implemented by NAND, NOR and NOT, however using universal logic gates for implementing the particular functions will be increased the

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count of transistors. In digital designs, the numbers of transistors have important effects such as design complexity, power consumption and delay, also designing with the large number of gates in the multi levels increases our computation time. In the proposed designing technique we used no universal gate and also no decoder to recognize inputs. By using this method the count of transistors will be reduced, thus reducing the count of transistors will affect delay, power dissipation and area.CNTFET-based ternary full adder cellshave been proposed by [10]which is implemented by combination of the capacitors and CNTFETs.They prepare the sum and carry by utilizing capacitor-based scaled analog summation for producing (∑in/3) together with a ternary buffer. The simulation results demonstrate that our propose designhas more than 77 percent in power saves over state-of-the-art circuit design. We used multiple-threshold CNTFETs to implement our ternary circuits and we apply CNTFET model of [11]. Our circuit design is simulated using HSPICE to confirm correct operation and evaluate its performance.

This paper is organized as follows: CNTFETs are briefly reviewed in the next section. Section III providesreview of multiple-valued logic and we introduce ternary full adder cell in section IV. Previous work including its advantages and disadvantagesdiscuss in section V. Section VI presentsour novel low power ternary CNTFET-based full-adder cell with detailed description and simulation results. Finally, conclusions and remarks are reported in Section VII.

II. REVIEW OF CNTFET

Since 1991 which Carbon Nanotube was discovered by Iijima [12] it has been studied in a wide field of science and also in nanoelectronic. Carbon Nano-Tube (CNT) has attracted attention in recent years not only for its relatively small dimensions and unique morphologies, but also for its potential of implementations in many current and emerging technologies. CNT is made up from graphite. It has been observed that graphite can be formed in the nanoscale in three forms: (1) Carbon Nano Ball (CNB) (or buckyball) - molecule consisting of 60 carbon atoms (C60) that are arranged in the form of a soccer ball (2) Carbon Nano-Tube (CNT) - narrow strip of tiny sheet of graphite that comes mainly in two types: (a) multi-wall CNT (MWCNT): each CNT contains several hollow cylinders of carbon atoms nested inside each other, and (b) single-wall CNT (SWCNT) that is made of just a single layer of carbon atoms, and (3) Carbon Nano Coil (CNC) CNT, which is a cylindrical sheet of graphite, is formed geometrically in two distinct forms which affect CNT properties: (1) straight CNT: CNT formed as a straight cut from graphite sheet and rolled into a tube, and (2) twisted CNT: CNT formed as a cut at an angle from graphite sheet and rolled into a tube. Several methods for growing CNTs exist [13]: (1) a big spark between two graphite rods, few millimeters apart, that are wired to a power supply: an approximately 102 Ampere spark between the two rods vaporizes carbon into hot plasma which partially re-condenses into the form of CNT, (2) chemical vapor deposition (CVD) of a hot gas such as methane: a substrate is placed in an oven, then the oven is heated to approximately 600 degrees Celsius and slowly methane is added. As methane decomposes, it frees carbon atoms that partially re-compose into the form of 0.6-1.2 nm in diameter SWCNTs, and (3) a laser blast of a graphite target: laser pulses blasts a graphite rod which generates hot carbon gas from which CNT forms. Although CNT has been grown into several forms, CNT use is still limited as compared to other wide spread technologies. This is mainly due to: (1) it is still difficult to exactly control CNT growth into desired forms, and (2) CNT growth is still very expensive due to the low yield of CNTs that meet desired geometrical specifications the wide usability of CNTs in so many applications is due to the unique structural properties they possess. Depending on the angle of the atom arrangement along the tube (chiralities) SWCNT can act as semiconducting or metal (conductor)[14]. Chirality vector defines arrangements of carbon atoms along the tube and is corresponding to the integer pair (n1, n2). Chirality vector has a ratio with CNT diameter (D_{CNT}) (Equation (1)). Because of the electrical properties of CNT, it is used for different applications in nanoelectronic for example quantum wire, random access memory and Nano-transistor [15]-[17]. We can use semiconducting SWCNTs as a controlling conductance channel for building CNT transistors. In MOSFETs these types of SWCNTs are situated as a channel between Drain and Source underneath Gate for carrier transport. By situating CNT as a channel in MOSFETs a new device is yielded that is generally known as Carbon Nanotube Field Effect Transistor (CNTFET) [18,19] or tube-FET [14].

In the last decade two different CNTFET circuit design techniques have been used in the literature, One of them is directly replacing the MOSFET with CNTFET to approach better performance; The second is used CNTFET as a particular nanotechnology devices with its powerful CNT characteristics [3]. Fig.1 shows the schematic diagram of CNTFET.

Transistors which use SWCNT have many benefits rather than silicon transistors counterpart such as high density of on current and moderately high Ion/Ioff ratio that has many effects on transistors behavior, molecular size, high theoretical transition frequency and changeable threshold voltage depending on carbon nanotube diameter which is an important characteristic of CNTFETs.

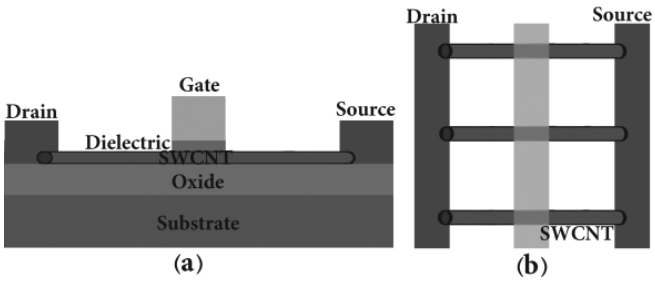

Fig.1Schematic diagram of a CNTFET: (a) Cross section view (b) top view

For CNT with (n1, n2) chirality, the diameter of CNTFET is calculated by following formula:

$$D_{CNT} = \frac{a\sqrt{n_1^2+n_1n_2+n_2^2}}{\pi} \quad (1)$$

Assume that (a) is the inter-carbon-atom distance within the hexagonal lattice which is approximately 1.44 Å then lattice constant (a) is given by $\sqrt{3}d$ = 2.49 Å. CNTFET threshold voltage is calculated as follow [19]:

(2)

$$V_{TH} = \frac{0.42}{D_{CNT}(nm)} V$$

This formula determines that CNTFETs turn on according to their CNT diameter in various voltages.We exploit this formula to obtain CNTFETs that turns on at different voltages depending on their diameters.

III. MULTIPLE-VALUED LOGIC (MVL)

Multiple-value logic system has better characteristic compared to conventional binary system such as increased data processing capability per unit area, reduced number and complexity of interconnections, as well as reduced number of active devices inside a chip. Hence, in the circuit which designs base on multiple-valued logic, circuits will be simpler and more flexible also more compact. By using MVL higher speed and less power dissipation will be achieved [20] [21]. To obtain ternary logic system we need three values, in conventional binary system we have two logics values '0' and '1', these logics represented by 0V and Vdd respectively. By appending one state between these two logics of conventional binary system ternary logic system can be achieved. In ternary logic system values represented by 0V, Vdd/2 and Vdd which denote '0', '1' and '2' respectively.MVL circuits have been designed usingcharge-coupled devices (CCDs), voltage mode CMOS, I^2L and current mode CMOS. Chip area and powerdissipation have been shown to be reduced by 50%using efficient MVL implementation of a signed 32bitmultiplier compared to its fastest binary counterpart. Let *E= {'0','1','2'}*. An *n*-variable ternary logic function *f* is a mapping from E^n into *E*, which to $X \in E^n$ assigns $f(X) \in E$.

IV. TERNARY FULL-ADDER

TFA (Ternary full-adder) is a simple ternary arithmetic unit which has three ternary inputs (A, B, C) and two ternary outputs (sum, carry);

Table I Truth table of Ternary FA

∑in=A+B	0	0	0	1	1	1	2	2	2	3	3	3	4	4	4
C	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2
Sum	0	1	2	1	2	0	2	0	1	0	1	2	1	2	0
Carry	0	0	0	0	0	1	0	1	1	1	1	1	1	1	2

It provides addition of three inputs and represents the results in two ternary signals called Sum and Carry, where A and B are operands, C is carried in signal (generally known as Cin), Sum is addition of inputs and Carry is carried out signal. C for each TFA cell is Carry of the previous TFA cell. Ternary full-adder truth table is shown in table I.According to table I, the relation between the inputs and outputsof a ternary FA (full-adder) cell can be presented as follow:

$$\textbf{Carry}=A_2B_2C_2+1\cdot(A_2B_2C_1+A_2B_2+A_2B_1C_2+A_2B_1C_1+A_2B_1+A_2C_2+A_2C_1+A_1B_2C_2+A_1B_2C_1+A_1B_2+A_1B_1C_2+A_1B_1C_1+A_1C_2+B_2C_2+B_2C_1+B_1C_2) \quad (3)$$

$$\textbf{Sum}=A_2B_2C_1+A_2B_1C_2+A_2+A_1B_2C_2+A_1B_1+A_1C_1+B_2+B_1C_1+C_2+1\cdot(A_2B_2+A_2B_1C_1+A_2C_2+A_1B_2C_1+A_1B_1C_2+A_1+B_2C_2+B_1+C_1) \quad (4)$$

V. PREVIOUS WORK

In [10] two ternary full adders have been proposed which is implemented by combination of the capacitors and CNTFETs based on the unique characteristics of the CNTFET device. The main advantages of these designs are reduction the number of transistors of ternary full adder cell and do not require any additional power supplies [10]. They prepare the sum and carry by utilizing capacitor-based scaled analog summation for producing (∑in/3)together with a ternary buffer. These works consists of 24 CNT transistors and also five capacitors for the first design and 18 CNT transistors plus five capacitors for the second design.

One of the disadvantages of works presented in [10] is high static power consumption and the other disadvantage is using capacitor to implement a particular function. Capacitor causes increasing in parasitic effects and will decrease the noise margin. Output parameters will be affected by changing the capacitance value of capacitors. Simulation results demonstrate that the proposed TFA consume significantly lower power and impress improvement in term of the power delay product compare to previous work.

VI. PROPOSED TERNARY FULL-ADDER CELL

In this paper to implement ternary logic FA cell we use multi-diameter CNTFETs. In order to observe the transient behavior of the circuits and to verify the functionality of our ternary full-adder cell, simulations have been done by means of HSPICE simulation tool. We apply the SPICE model from [11] which described in more details in [22] and [23] with the following parameters:

Table II Characterizes properties of CNTFETs which are used in this paper

Type	Diameter	Chirality	Threshold	Tubes per FET	Gate Length	Pitch
P-Type	0.783	(10,0)	-0.559	3	32E-9 m	20E-9 m
	1.018	(13,0)	-0.428			
	1.487	(19,0)	-0.289			
N-Type	1.487	(19,0)	0.289	3	32E-9 m	20E-9 m
	1.018	(13,0)	0.428			
	0.783	(10,0)	0.559			

The diameter of each CNT transistors is denoted on the schematics. Basic scheme of proposed low power CNTFET-based ternary full adder cell is depicted in fig.2. We assume that the inputs and their complement are available. This adder cell consists of two THA (Ternary Half Adder) which each half adder computes the sum value of inputs and a carry generator. The first THA adds input operands (A and B), then the result (H) is transferred to second THA and carry generator unit. In the second THA result of A+B (H) will be added to input carry (C). Then the output of the second ternary half adder is A+B+C. The transistor level scheme of the THA unit has been represented in Fig.3. This unit has 26 CNT Transistors.

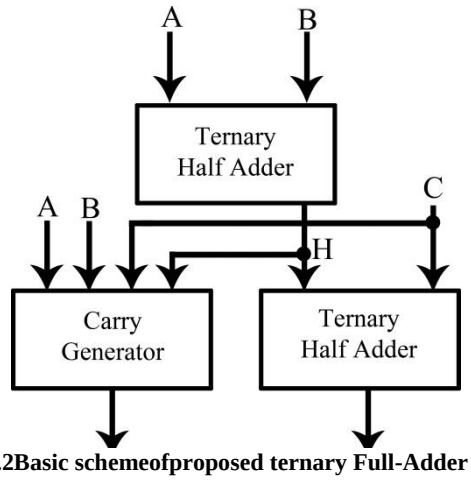

Fig.2Basic schemeofproposed ternary Full-Adder cell

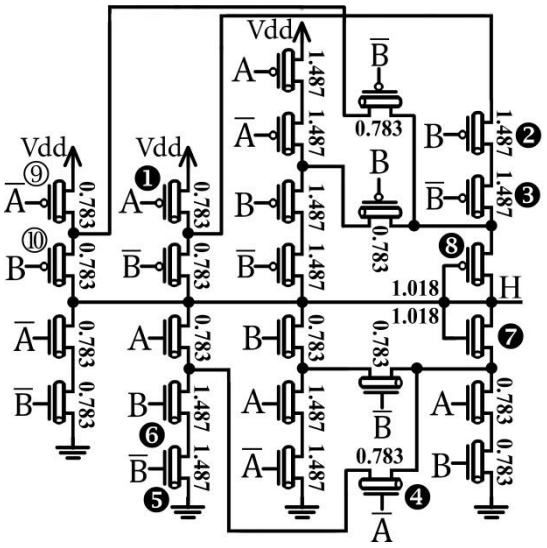

Fig.3Transistor level scheme of the THA unit

We check the circuit performance by applying some values, fig.4 shows the simulation input patterns and output waveforms. For instance if input A, has the '0' logic value and B has '1' value, the transistors number 1-8 will switch ON. Consequently a voltage division will happen and Vdd/2 which is equal to '1' drops to the outputs.

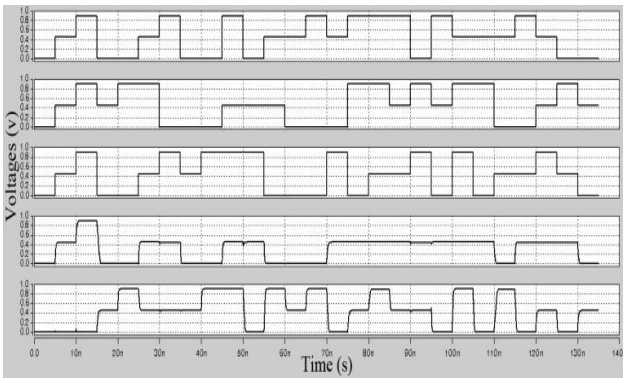

Fig.4 transiat responce of the sum and carry

The transistors with numbers 7 and 8 involve in voltage division. Now consider A and B become '2' and '0' respectively, these changes turn ON the transistors number 9 and 10. Therefore the output will be connected to Vdd through these transistors (Logic '2').The carry computation unit is shown in Fig.5. This circuit consists of 30 CNT transistors. Transistors that are denoted by8 and 9 lead to voltage division. As an example when one of the outputs is '0', and the sum of two input operands (H) becomes '0' too, transistor number 5 and one of the two transistors numbered by 6 or 7 will be set (A='0' will set 6 and B='0' sets 7). Accordingly output pulled down to GND (Logic '0'). For another example, if the value of H changes to '0' while the input carry is '1' or '2', transistors number 1, 2, 3, 4,8 and 9 switch ON thus we have '1' at the output.

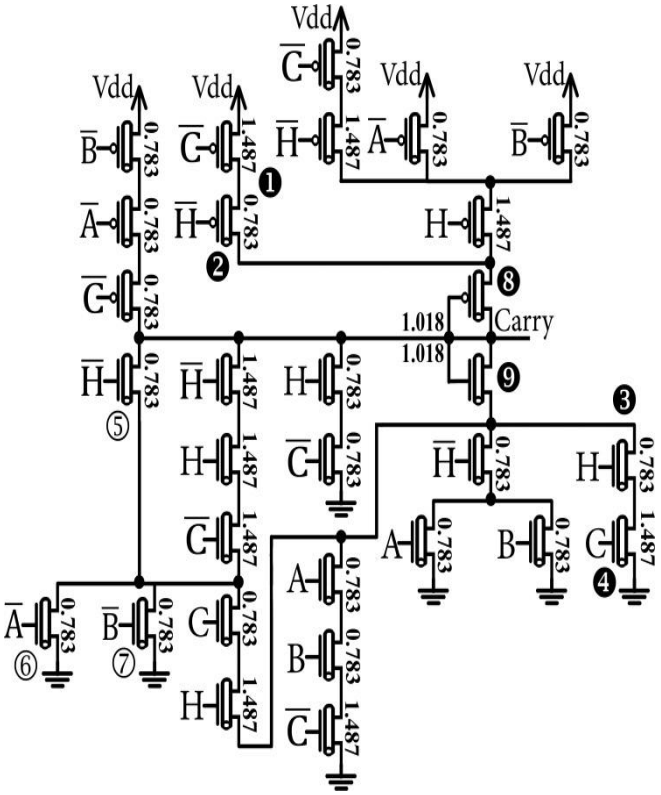

Fig.5transistor level scheme of thecarry generator unit

Standard Ternary Inverter (STI) is required to calculate H-not (Specified area in fig.6 denoted by doted-rectangle). We can find the STI output using equation (5) and truth table is shown in Table.III as well.

$$O=2-I \qquad (5)$$

Where O is output and I is input of the STI.

Table III truth table of STI

In	0	1	2
Out	2	1	0

The completion adder circuit for sum calculation is depicted in Fig.6. For implementing such a proposed adder, 88 CNT transistors are required.For testing and evaluating of our proposed design, we used HSPICE simulator in room temperature, applying 0.9 V voltage as power supply in addition 2fF and 3fF load capacitors are used at the output nodes of circuit.In each situation, the worst case propagation delay ([MAX (the worst case $delay_{Sum}$, the worst case $delay_{carry}$)]) and average power consumption were evaluated. Also PDP which is the multiplication of the worst case delay and average power consumption was calculated. The results of simulation are listed in Table.IV. As it was shown in the first situation (with loads=2fF)our proposed design has 77.02% and 68.74% also 92.6% and 89.04% improvement in

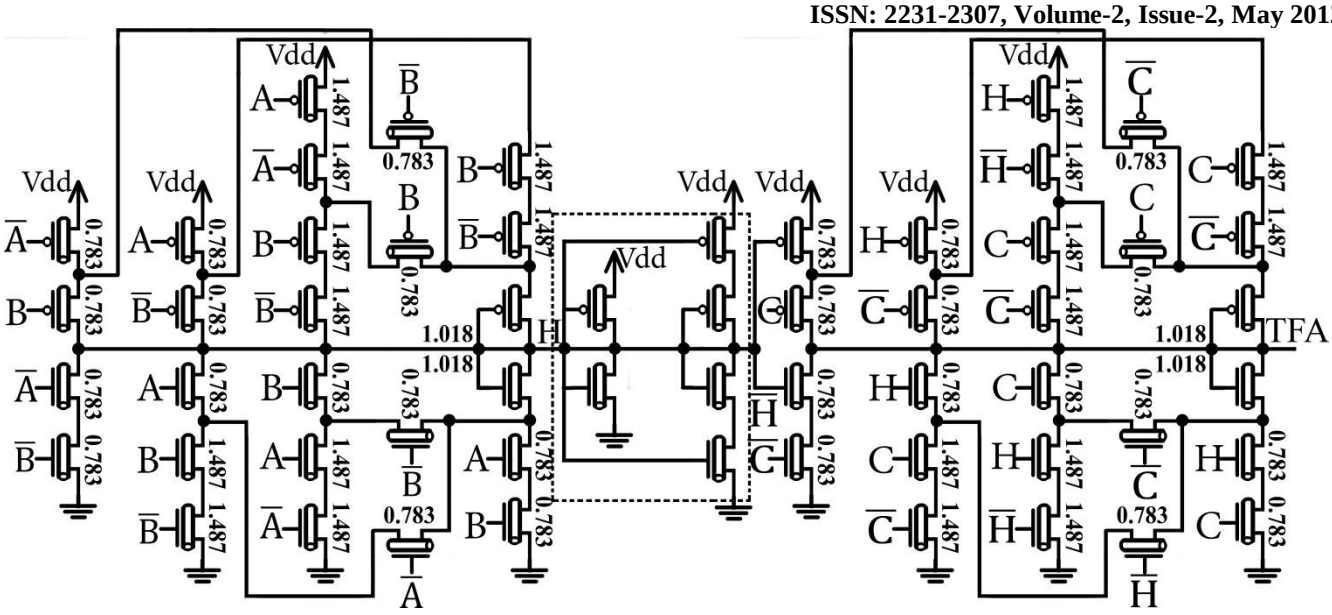

Fig.6The completion adder circuit for sum calculation

term of average power and PDP compare to the first and the second designpresented in [10], respectively and in the second situation (with loads=3fF)ithas 77.51% and 60.82% also 92.44% and 84.51% improvement in term of average power and PDP compare to the first and the second designpresented in [10], respectively.

Table IVSimulation results of full-adder cells

Loads=2fF			
design	Delay (ps)	power (uW)	PDP (e-15J)
1st [10]	283.8	6.361	1.806
2nd [10]	261.4	19.71	5.152
Proposed	386.1	1.462	0.5645
Loads=3fF			
1st [10]	327.1	6.719	2.197
2nd [10]	278.1	19.99	5.559
Proposed	569.6	1.511	0.8607

VII. CONCLUSION

Through CNTFET characteristics different threshold voltages can be achieved which make CNTFETs useful and more reliable in the MVL circuit designs. In this paper we presented the novel low power ternary full adder cell circuit designs. Simulation results are demonstrated that we have achieved the efficient circuit design parameters such as power consumption and power-delay product.

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