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Design of Risk Analysis for an Embedded System using Finite State machine Technique

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Abstract— This paper presents an approach for designing of Risk Analysis for the Embedded System components/subsystems functionality using Finite State Machine (FSM) embedded in the system. The current method of designing the Risk Analysis or Test Case designing is completely based on the Tester/Test Leads experience on the system and its internal understanding [1]. With the concept of black-box Risk Analysis test data derivation from a Finite state machine (FSM) file which has the complete data of the State Transition of the System. The approach is arrived based on the concept of state transitions of the system events and its Actions that are triggered on its transition. Using the search algorithm to list the dependencies of the Fix related to the Components are generated. An algorithm is designed to recognize the communicating transitions from the FSM file [4]. When the component related fix made by the developer using the manual Risk Analysis technique we arrive at the tests manually.

Index Terms- Risk Analysis, Finite State Machine, Black Box.

I. INTRODUCTION

In the Software Development Phase the goal of the Software testing is to find defects for the product stability and the improvement of Quality and the product we represent as system under test. We do adapt some Test Methodologies, Testing Techniques and Processes to measure and evaluate the Quality, test coverage. Basically we do adapt the Software Testing life cycle to arrive at the outcome some of the practices followed are test case design, test verification and test coverage analysis[2]. The application of test criteria for the selection of good test case sets, i.e., those that have a high chance to detect the existent defects [1].

II. FINITE STATE MACHINE ANALYSIS

Many types of functional testing technique that has been commonly used to design the test cases or the Risk areas. The application of FSMs as a technique in designing the Risk Analysis for any of the embedded system which has the FSM table embedded [2]. The FSM model represented consists on a state set and a state transition set. Given a current state and an input, the next state and an output can be determined, as presented in Figure 1. A sequence of state transitions, from the initial state to any final state is predicted based on the event occurrence [4].

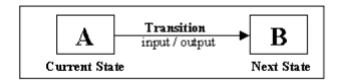


Figure 1. State transition in a state graph that represents a FSM

The functional criteria based on FSMs, used for Risk Analysis are:

- States: The states inside the FSM define the node of initial and final destination based on the event
- Transitions: The transitions inside the FSM occurs while the event occurrence and with some conditions



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III. PROBLEM DEFINITION

In a huge Embedded system which has multiple dependencies and also with lot of complicated features if there is a defect in system and developers make fix for the defect and to ensure testing only the related areas are not affected we need to perform testing [3], So the Test Engineer would arrive at the Risk Areas to test only the affected areas. The below is the list of problems stated

- At present all the test engineers design the Risk Analysis (RA) test cases based on their prior experience of the product and also there is lot of possibilities that some of Test Cases could be missed.
- Need to be well aware of the internal Technology, underlined Architecture and the event flow.
- Manually designing the Risk based Test cases with experience also there are chances of missing some component dependency tests is possible.
- No assurances with the coverage of Risk using traceability matrix criteria of the test cases wrt requirements implementation are met and also ensuring the subcomponents affecting that fix is difficult to track.

IV. DESIGN

For the above mentioned problems using the concept of underlying Finite state machine Whenever a new feature is added/deleted or modified there are various other components which get affected[4]. But with the approach of FSM which is similar to Finite state machine (FSM) will have a clear picture of the event flow and how the other subsystems are dependent on each other, the states of the other components etc, and hence we can design the Risk Analysis more efficiently[3]. From the figure 2, the flow diagram to generate the Risk Analysis from which we generate the Risk based Test Cases.

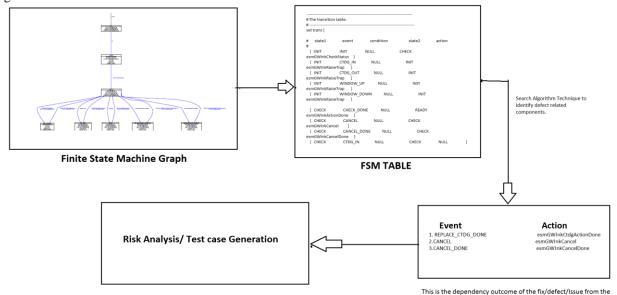


Fig 2. Flow diagram to generate the Risk Analysis

V. CONCLUSION

In functional testing we have arrived the generation of Risk Based test cases from the FSM. Using this method or technique the Software Test Engineers, Quality Assurance Team, Test Analysts can provide their maximum confidence and assurance in qualifying the defect in the Testing life cycle with a very short span of time instead of testing the whole functionality even though the others areas when not affected. Analyzing the Risk using FSM build confidence for the Individual, team and the Management as the FSM based Risk analysis provide guaranteed assurances of the affected areas and can be tested easily. While existing functional testing criteria, based only on the analysis of traditional FSMs control flow, demand just that elements such as states, arcs and loops are exercised, the proposed functional testing criteria, based on the analysis of FSM data flow, demand that elements such definitions and uses of variables are exercised as well.



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In Future

- 1. A more detailed analysis of the defect types using the FSM technique.
- 2. Tool to provide the Risk in terms of levels based on the major workflow coverage.

REFERENCES

- [1] http://mtc-m18.sid.inpe.br/col/lac.inpe.br/worcap/2003/10.31.14.20/doc/Ambrosio-Worcap2003.pdf.
- [2] http://dspace.brunel.ac.uk/bitstream/2438/3062/3/Thesis%20-%20with%20corrections.pdf.
- [3] http://www.ijsce.org/attachments/File/v2i3/C0806062312.pdf.
- [4] http://www.dsu.edu/research/ia/documents/[43]-Automated-Test-Code-Generation-from-UML-Protocol-State-Machine s.pdf

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