II. Bias circuit

Outline

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- Cascode current mirror
- Modified cascode current mirror
- High-compliance current mirrors (I - II)
- Regulated cascode current mirror
- Low-voltage current mirrors

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- Current references based on a built-in voltage
- Current references based on a reference voltage

Voltage references

- Introduction
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- Voltage references based on the band-gap voltage
- Voltage references based on MOS V_{TH} difference

II. Bias circuit

Introduction

- Active devices (transistors) have to be properly biased to process the signal
- In an analog signal processing circuit there are two fundamental parts:

  Processing part

  Bias circuit

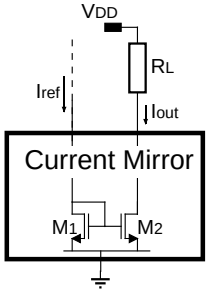
- The processing part is devoted to elaborate the signal
  Dynamic requirement

- The bias circuit is devoted to supply currents and/or voltages to the processing one in order to allow it to properly operate
  Static requirement (Low-frequency, immunity to V_{DD} noise, temperature, and technology spread)

CMOS current mirrors

Definitions

A current mirror reads a current entering in a read-node and mirror this current (with a suitable gain factor) to an output node (nodes)

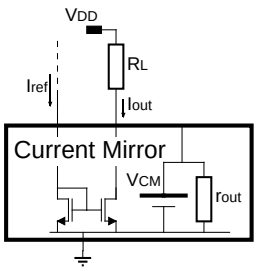


$I_{out} = k \cdot I_{Ref}$

k current gain

Current mirror non-idealities

- Current gain error
- Output impedance (r_{out})
  => reduces the output current I_{out}
  $= k \cdot I_{Ref} \cdot \frac{RL}{RL + r_{out}}$
- Saturation voltage (V_{CM})
  => for $V_o < V_{CM}$ the current mirror doesn't operate correctly
  => reduces the output voltage dynamic range



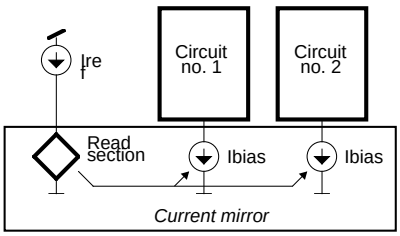
Basic trade-off: dynamic range <=> precision

- Frequency behaviour

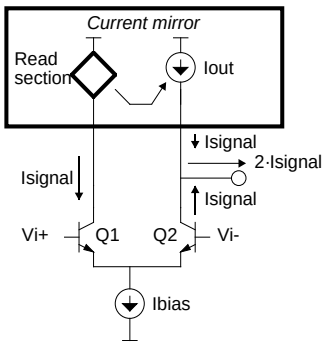
CMOS current mirrors

Applications

- Bias

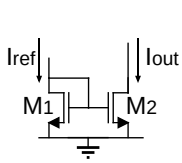


- Signal path

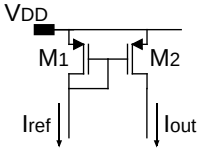


- Differential-to-Single Ended transformation
- Frequency behaviour

Simple Current Mirror
Current gain



NMOS



PMOS

- M1 operates in saturation

$$I_{Ref} = I_1 = \frac{k'}{2}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TH})^2 \ (1 + \lambda V_{DS1})$$

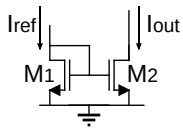
$$V_{DS1} = V_{GS1} = V_{GS2}$$

- If M2 operates in saturation

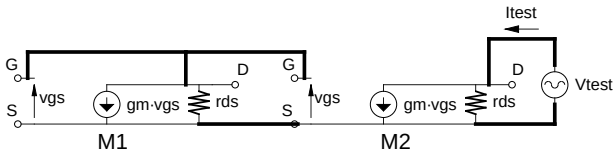
$$I_{out} = I_2 = \frac{k'}{2}\left(\frac{W}{L}\right)_2 (V_{GS2} - V_{TH})^2 \ (1 + \lambda V_{DS2})$$

$$I_{out} = I_{Ref} \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} \frac{(1 + \lambda V_{DS2})}{(1 + \lambda V_{DS1})}$$

Simple Current Mirror
Output impedance (r_{out})



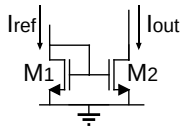
- Insert V_{test}
- Evaluate I_{test}
- Calculate $r_{out} = \frac{V_{test}}{I_{test}}$



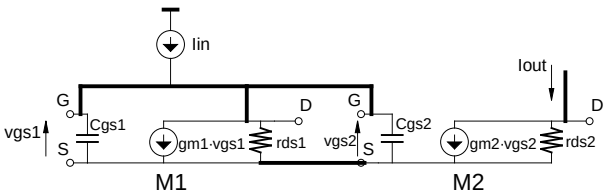
$$r_{out} = r_{ds2} = \frac{1}{\lambda \ I_2}$$

- Use of long device (large L) to increase r_{out}
- Use of large ($V_{GS} - V_{TH}$) for good matching (small importance of V_{TH} mismatch)

Simple Current Mirror
Frequency behaviour



Small signalequivalent circuit



$$\frac{i_{out}}{i_{in}} = \frac{g_{m2}/g_{m1}}{1+s\cdot(C_{gs1}+C_{gs2})/g_{m1}}$$

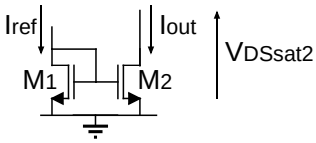
$k = g_{m2}/g_{m1} = C_{gs2}/C_{gs1}$

$$\frac{i_{out}}{i_{in}} = \frac{k}{1+s\cdot(1+k)\cdot C_{gs1}/g_{m1}}$$

$f_T = g_{m1}/C_{gs1}$

$$pole = (g_{m1}/C_{gs1})/(1+k) = f_T/(1+k)$$

Simple Current Mirror
Output swing



- The output swing in the Simple current mirror is limited to

$$V_{out,min} = V_{DSsat,2}$$

Simple Current Mirror

Factors affecting the mirror accuracy

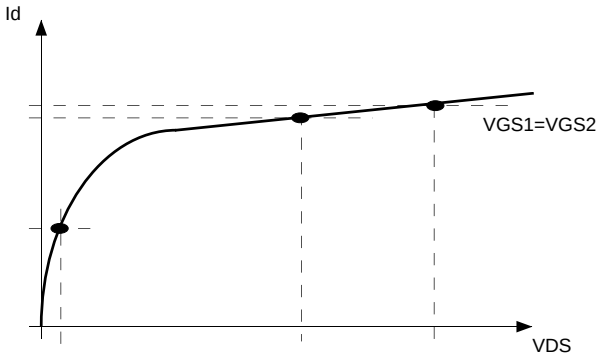
- Channel length modulation (λ)
- Threshold offset
- Parasitic resistances
- Imperfect geometrical matching and current mobility variation

Simple Current Mirror

Factors affecting the mirror accuracy

- Channel length modulation (λ)

$$\frac{I_{out}}{I_{Ref}} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2} \cdot \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}$$

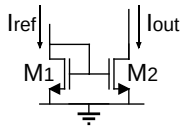


It can be improved by increasing the output resistance.

- use of large L (typically current mirrors are not realized with th eminimum technological L. This can results in a large capacitance at the output node)

Simple Current Mirror

Factors affecting the mirror accuracy



- Threshold offset

  Threshold of MOS transistors in close proximity can differ by 4 mV. For transistors hundred of μm apart, the threshold difference ΔV_{Th} can be 40 mV

$$I'_{out} = I_{out}\left(1 + 2\,\frac{\Delta V_{TH}}{V_{GS} - V_{TH}}\right)$$

  Use large ($V_{GS} – V_{TH}$) to improve matching

- Parasitic resistances

  A parasitic resistance in series with the source determines a voltage drop

  The metal resistance is of the order of 20-50 $\mu\Omega/_{q}$, with 10 squares it results 0.2-0.5 Ω. If the current is 10 mA it results an equivalent offset of 2-5 mV.

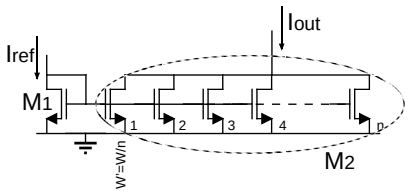
Simple Current Mirror

Factors affecting the mirror accuracy

- Imperfect geometrical matching and current mobility variation

$$\left(\frac{\delta I}{I}\right)^2 = \left(\frac{\delta k'}{k'}\right)^2 + \left(\frac{\delta C_{ox}}{C_{ox}}\right)^2 + \left(\frac{\delta W}{W}\right)^2 + \left(\frac{\delta L}{L}\right)^2$$

- $\frac{\delta k'}{k'}$ and $\frac{\delta C_{ox}}{C_{ox}}$ are minimized with closed and centroid common structures
- $\left(\frac{\delta W}{W}\right)^2 + \left(\frac{\delta L}{L}\right)^2$ depends on the lithographyc process
- For large W a good strategy is to have W not much larger than L and to put equal transistors in parallel



$$\left(\frac{\delta I}{I}\right)^2 = ... + \frac{1}{n}\left[\left(\frac{\delta W'}{W'}\right)^2 + \left(\frac{\delta L}{L}\right)^2\right]$$

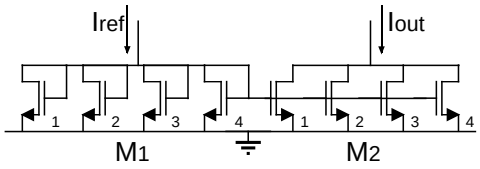
Simple Current Mirror

Factors affecting the mirror accuracy

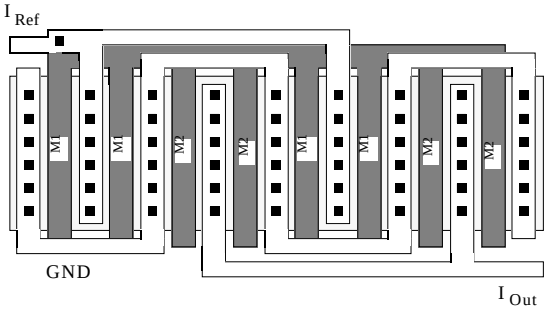
- Imperfect geometrical matching and current mobility variation

Example:

Circuit scheme



Layout solution



Simple Current Mirror

Design example

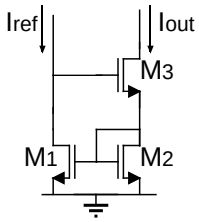
With the following technological parameter design a simple current mirror in order that it drives to the output node 1mA and it requires 400mV

$L_{min} = 0.5\mu m$; ; $\mu_n \cdot C_{ox} = 60\mu A/V^2$; $\mu_p \cdot C_{ox} = 30\mu A/V^2$;
$\lambda_n = 0.1\ V^{-1}$; $\lambda_p = 0.2\ V^{-1}$; $\gamma = 0$; $V_{THN} = -V_{THN} = 0.7V$

Which is the expected output impedance ?

Wilson current mirror

Increases the output resistance



$$V_{GS1} = V_{GS2}$$

$$I_1 \approx I_2$$

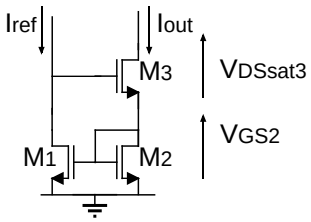
$$\frac{I_{out}}{I_{Ref}} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2} \cdot \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}$$

$$\frac{I_{out}}{I_{Ref}} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2} \cdot \frac{1 + \lambda V_{DS2}}{1 + \lambda (V_{DS2} + V_{GS3})}$$

- There is a sistematic error since $V_{DS1} = V_{DS2} + V_{GS3}$

Wilson current mirror

Output swing

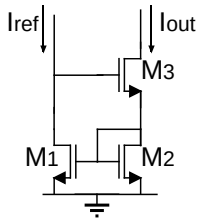


- The output swing in the Wilson current mirror is limited to

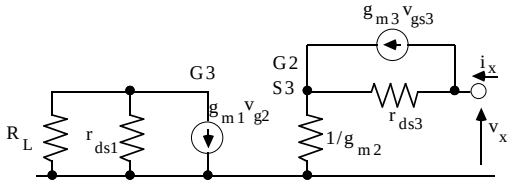
$$V_{out,min} = V_{GS2} + V_{DSsat,3} > V_{Th} + 2 \cdot V_{DSsat}$$

Wilson current mirror

Output impedance



Small signal equivalent circuit



$$v_{g2} = v_{s3} = i_x/g_{m2}$$

$$v_{g3} = - g_{m1}\, v_{g2}\, r_T \qquad (r_T = R_L \,//\, r_{ds1})$$

$$v_x = i_x/g_{m2} + (i_x - g_{m3}\, v_{gs3})\, r_{ds3}$$

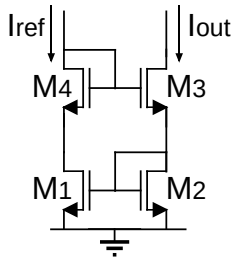
$$r_{out} = \frac{v_x}{i_x} = \frac{1}{g_{m2}} + r_{ds3}\left[1 + \frac{g_{m3}}{g_{m2}} + \frac{g_{m3}}{g_{m2}}\; g_{m1}\; r_T\right]$$

$$r_{out} \cong r_{ds3}\frac{g_{m3}}{g_{m2}}\, g_{m1} r_T$$

- R_L (i.e. I_{ref} current generator impedance) must be large

Improved Wilson current mirror

Current gain



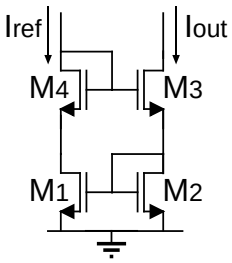
$$V_{DS1} = V_{DS2} + V_{GS3} - V_{GS4}$$

$$V_{DS1} = V_{DS2} \quad \text{if} \quad V_{GS3} = V_{GS4}$$

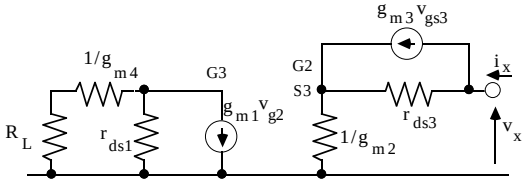
$$\frac{I_{out}}{I_{Ref}} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2} \cdot \frac{1 + \lambda\, V_{DS2}}{1 + \lambda\, V_{DS1}} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2}$$

- Higher voltage for the sensing branch (M1-M4)
- No sistematic error in the current gain

Improved Wilson current mirror



Small signal equivalent circuit



Same equations with:

$$v_{g3} = - g_{m1}\, v_{g2}\, r'_T\, \frac{R_L\, g_{m4}}{1 + R_L\, g_{m4}}$$

$$r'_T = r_{ds1} \,//\, (R_L + 1/g_{m4})$$

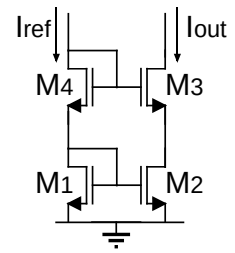
$$r_{out} \cong r_{ds3}\frac{g_{m3}}{g_{m2}}\; g_{m1}\, r'_T \frac{R_L\, g_{m4}}{1 + R_L\, g_{m4}}$$

- The output swing in the Wilson and improved Wilson schemes is limited to

$$V_{out,min} = V_{GS2} + V_{DSsat,3} > V_{Th} + 2{\cdot}V_{DSsat}$$

Cascode Current Mirror

Current gain



$$V_{DS1} = V_{DS2} + V_{GS3} - V_{GS4}$$

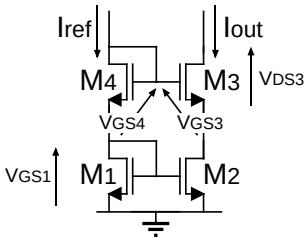
$$V_{DS1} = V_{DS2} \quad \text{if} \quad V_{GS3} = V_{GS4}$$

$$\frac{I_{out}}{I_{Ref}} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2} \cdot \frac{1 + \lambda\, V_{DS2}}{1 + \lambda\, V_{DS1}} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2}$$

- The current gain is accurate
- For large current (i.e. with $(W/L)_{M2}$ large) it allows to decrease the output capacitance using $(W/L)_{M3}$ small.

Cascode Current Mirror

Output swing



$V_{GS3} = V_{GS4}$

- The output swing is limited to:

$$V_{out,min} = V_{GS1} + V_{GS4} - V_{GS3} + V_{DSsat,3}$$

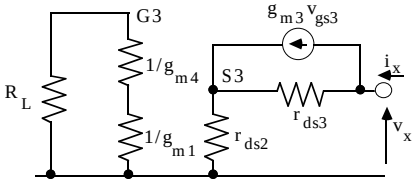
$$V_{out,min} = V_{GS2} + V_{DSsat,3} > V_{TH} + 2 \cdot V_{DSsat}$$

Cascode Current Mirror

Output impedance

- The output resistance is increased without feedback.

Small signal equivalent circuit



$$i_x = g_{m3} v_{GS3} + (v_x - v_{S3})/r_{ds3}$$

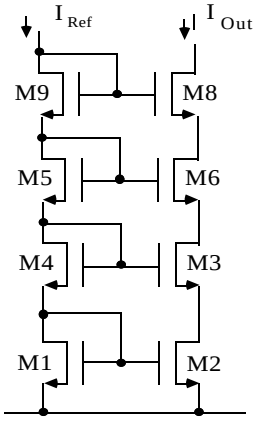
$$i_x = v_{S3}/r_{ds2}$$

$$i_x = g_{m3} (-v_{S3}) + (v_x - v_{S3})/r_{ds3}$$

$$i_x = v_{S3}/r_{ds2}$$

$$r_{out} = r_{ds2} + r_{ds3} + r_{ds3}\, g_{m3}\, r_{ds2} \cong r_{ds3}\, g_{m3}\, r_{ds2}$$

Multiple-Cascode Current Mirror



- More cascode stage can be stacked to increase output impedance.
- For n stages

  + Output impedance

$$r_{out} \cong (r_{ds} \cdot g_m)^{n-1} \cdot r_{ds}$$

  BUT:

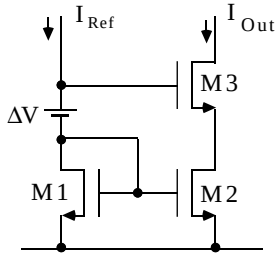
  - The saturation voltage increses to:

$$V_{out,min} = (n-1) \cdot V_{TH} + n \cdot V_{DSsat}$$

  + The current gain is accurate ($V_{DS1} = V_{DS2}$)

Modified Cascode Current Mirror

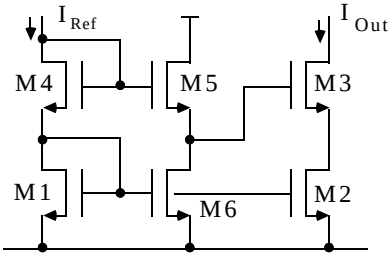
- Increase the output swing with the cascode output impedance



- M4 shifts the voltage V_{DS1} of the amount enough to bias the gate of M3 without operating M2 out of saturation.

Modified Cascode Current Mirror

Possible implementation



- M4 is matched with M3 to get $V_{DS1} = V_{DS2}$ (at the cost of the output swing limitation).
- The output swing is improved by the use of a level shift $V_{Sat} < \Delta V < V_{TH}$

$$\Delta V = V_{GS4} - V_{GS5} = \sqrt{\frac{2}{k'\left(\frac{W}{L}\right)_4} I_{Ref}} - \sqrt{\frac{2}{k'\left(\frac{W}{L}\right)_5} I_5} =$$

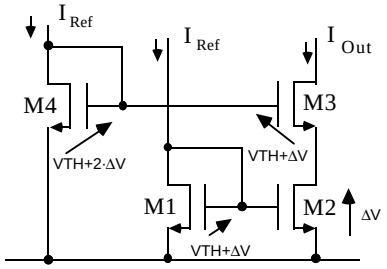
$$\sqrt{\frac{2}{k'\left(\frac{W}{L}\right)_4} I_{Ref}} \left\{1 - \sqrt{\left(\frac{L}{W}\right)_5 \left(\frac{L}{W}\right)_6 / \left[\left(\frac{W}{L}\right)_4 \left(\frac{W}{L}\right)_1\right]}\right\}$$

- ΔV is fixed by he geometrical dimensions of M_1, M_6, M_4, M_5 and by $V_{ov,4}$.
- The output swing is:

$$V_{out,min} = V_{DS2} + V_{DS3} = 2 \cdot V_{DSsat}$$

- Sistematic error in the current gain ($V_{DS1} \neq V_{DS2}$)

High-compliance current mirrors (I)



All transistors operate in saturation

$I = I_1 = I_2 = I_3 = I_4$ (current scaling is possible)

$\beta_1=\beta_2=\beta_3=\beta$ => $V_{ov1} = V_{ov2} = V_{ov3} = V_{ov}$

$I_4 = \beta 4 \cdot (V_{ov})^2$; $I_2 = \beta \cdot (V_{ov})^2$; $I_3 = \beta \cdot (V_{ov})^2$

$V_{ov}=\Delta V$ => $V_{DS2} = V_{ov}$

$V_{GS3} = V_{TH} + V_{ov}$

$V_{GS4} = V_{TH} + 2 \cdot V_{ov}$

$$V_{ov4} = \sqrt{\frac{I}{\beta 4}}; \quad V_{ov} = \sqrt{\frac{I}{\beta}}$$

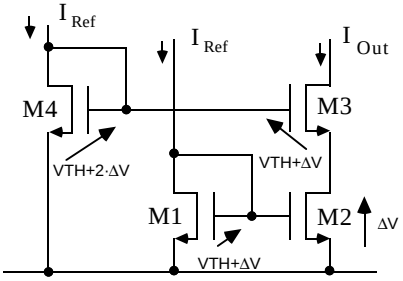
$V_{ov4} = 2 \cdot V_{ov}$ =>

$$\sqrt{\frac{I}{\beta_4}} = 2 \cdot \sqrt{\frac{I}{\beta}}$$

$$\beta = 4 \cdot \beta_4$$

$$\left(\frac{W}{L}\right)_{M1} = \left(\frac{W}{L}\right)_{M2} = \left(\frac{W}{L}\right)_{M3} = 4 \cdot \left(\frac{W}{L}\right)_{M4}$$

High-compliance current mirrors (I)



- Current gain

  Sistematic error due to $V_{DS1} \neq V_{DS2}$

  Sistematic error due to body effect on M3

- Output swing

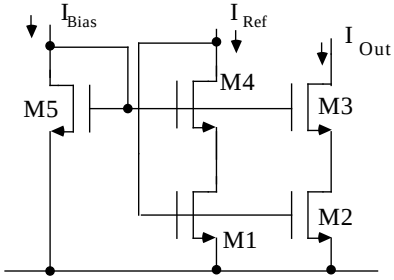
$$V_{out,min} = 2 \cdot V_{DSsat}$$

- Output impedance

$$r_{out} = r_{ds4} \cdot g_{m2} \cdot r_{ds2}$$

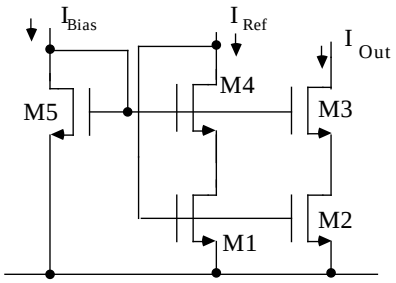
- The scheme can be stacked for multiple cascode

High-compliance current mirrors (II)

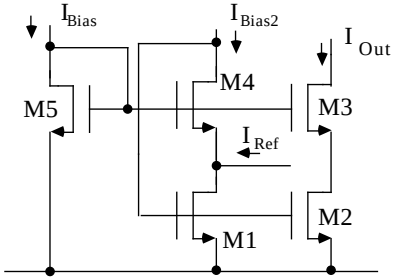


- M1=M2; M3=M4 => $I_{out} = I_{Ref}$
- $V_{DSsat4} > V_{TH}$ to properly work

High-compliance current mirrors (II)

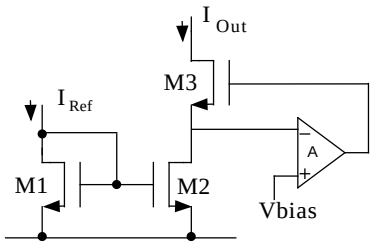


- It is also possible to enter at the drain of M1



$I_{out} = I_{Bias2} + I_{Ref}$

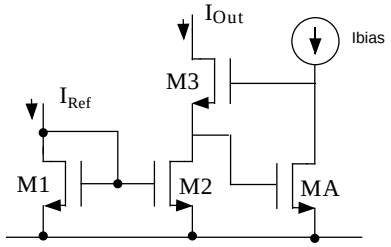
Regulated-cascode current mirror



- Output impedance

$$r_{out} = (g_{m3} \cdot r_{o3}) \cdot r_{o2} \cdot A$$

- Possible implementation



- Output impedance

$$r_{out} = (g_{m3} \cdot r_{o3}) \cdot r_{o2} \cdot (g_{mA} \cdot r_{oA})$$

- Output swing

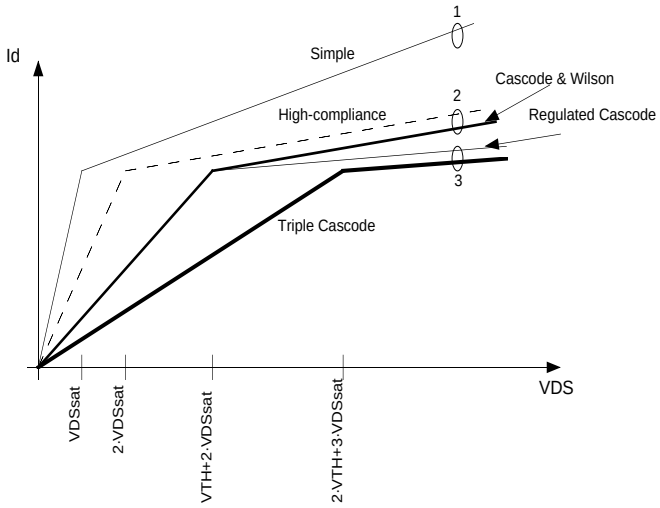
$$V_{out,min} = V_{GSA} + V_{DSsat3}$$

$$V_{out,min} = V_{TH} + 2 \cdot V_{DSsat}$$

- Sistematic error since Iref≠Ibias
  (Solution proposed by Zeki, et al., IEE El. Letters, 5th June 1997, pp. 1042)

Output swing for different current mirrors

Comparison



- The slope (1, 2, or 3) indicates the output impedance (r_{out})

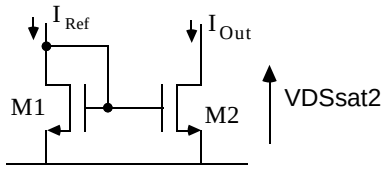
Low-voltage current mirror

For low-voltage application the dc voltage drops must be minimized in order to:

- give the maximum room for the signal swing
- not to limit the supply minimization with bias circuits

This valid both for the input stage (reading the current) and for the output stage (sinking the current)

For the simple current mirror



- The output stage (M2) requires

$$V_{out,min} = V_{DSsat}$$

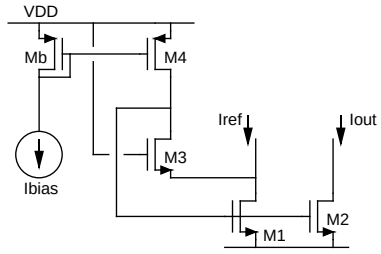
- This is minimum, thus staked-device topologies are avoided
- Output impedance is increased with large L
- The input stage (M1) requires

$$V_{out,min} = V_{TH} + V_{ov} + V(I_{Ref})$$

This value can be reduced

Low-voltage current mirror

The input stage voltage requirement can be reduced by using the low-voltage current mirror



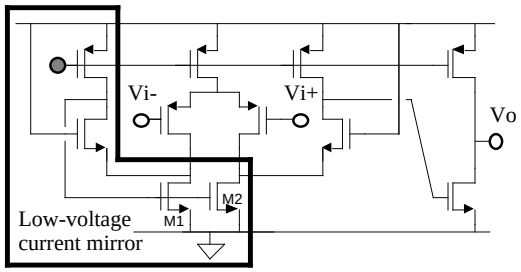
- The drain of M1 is fixed to be $V_{DD} - V_{GS3}$
- This is fixed to be equal to V_{DSsat}
- The current mirror requires one V_{DSsat} to operate.

$$I_{out} = I_{M3} + I_{ref}$$

Low-voltage current mirror

Application

- Operational amplifier



CMOS current mirrors

Comparison Table

Configuration	Current gain	Output swing	r_{out}
Simple	$\frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}$	V_{DSsat}	r_{ds}
Wilson	$\frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}$	$V_{TH} + 2 \cdot V_{DSsat}$	$g_m \cdot r_{ds}^2$
Improved Wilson	1	$V_{TH} + 2 \cdot V_{DSsat}$	$g_m \cdot r_{ds}^2$
Cascode	1	$V_{TH} + 2 \cdot V_{DSsat}$	$g_m \cdot r_{ds}^2$
Triple Cascode	1	$2 \cdot V_{TH} + 3 \cdot V_{DSsat}$	$g_m^2 \cdot r_{ds}^3$
Triple Cascode	1	$2 \cdot V_{TH} + 3 \cdot V_{DSsat}$	$g_m^2 \cdot r_{ds}^3$
High-compliance I	$\frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}$	$2 \cdot V_{DSsat}$	$g_m \cdot r_{ds}^2$
High-compliance II	1	$2 \cdot V_{DSsat}$	$g_m \cdot r_{ds}^2$
Regulated-cascode	$\frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}$	$V_{TH} + 2 \cdot V_{DSsat}$	$g_m^2 \cdot r_{ds}^3$

Exercise

1 - DC analysis of Simple CM
2 - AC analysis of Simple CM
  - Transfer function
  - Output impedance (for different L, with same W/L)
3 - Check the sistematic error in Wilson CM (different VDS)
  - Improve by using large L (with same W/L)
  - Check the signal swing (DC sim.)
4 - Cascode CM
  - Evaluate the output impedance (AC)
  - Evaluate the signal swing (DC)
5 - Multiple Cascode CM
  - Evaluate the output impedance (AC)
  - Evaluate the signal swing (DC)
6 - Large dynamic Cascode CM
  - Evaluate the output impedance (AC)
  - Evaluate the signal swing (DC)
7 - Low-voltage CM operation

Current references

Introduction

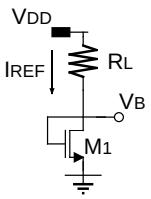
- It allows to generte on-chip (no external components) a current reference
- Necessary for biasing analog subcircuits.
- The generated current reference is mirrored where required, with a suitable scaling factor.

  Typically the reference current in the reference current generator is much smaller than the current level in the main circuit (i.e. the scale factor is larger than one) in order to reduce power consumption in the current reference generator

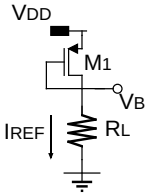
- Possible current reference generators
  - Simple current reference (supply depedent)
  - Current references based on a built-in voltage (supply indepedent)
  - Current references based on a reference voltage (supply indepedent)
- Features for a reference current
  - Supply dependence
  - Temperature dependence
  - Technology dependence

Simple current reference
(supply depedent)

NMOS



PMOS



- Voltage V_B is used to bias a current mirror
- For the NMOS case:

$$I_{REF} = \frac{V_{DD} - V_{DS1}}{R_L}$$

$$|V_{ov1}| = \sqrt{\frac{2}{k'} \cdot \frac{I_{REF}}{(W/L)_1}}$$

$$I_{REF} = \frac{V_{DD} - |V_{TH1}| - |V_{ov1}|}{R_L}$$

$$I_{REF} = \frac{V_{DD} - |V_{TH1}| - \sqrt{\frac{2}{k'} \cdot \frac{I_{REF}}{(W/L)_1}}}{R_L}$$

Supply dependence
I_{REF} depends on supply voltage V_{DD}

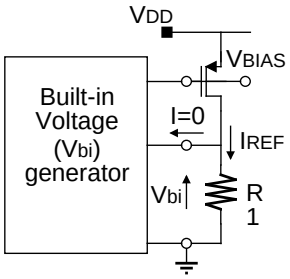
Temperature dependence
- R_1: positive temperature coefficient (TC)
- $|V_{TH}|$: negative temperature coefficient
- $|V_{ov}|$: positive temperature coefficient

- Typically the sum ($V_{GS1}=|V_{TH}| + |V_{ov}|$) has a negative TC

Current references based on a built-in voltage

Basic principle

- The current is obtained by "extracting" a built-in voltage (V_{bi}) to be applied to a given resistor

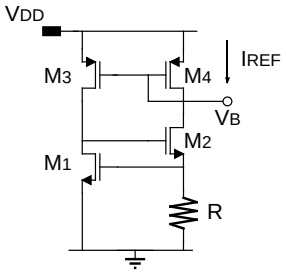


$$I_{REF} = \frac{V_{bi}}{R_1}$$

- The dependence of the built-in voltage on temperature and other parameters will affect the generated reference current.
- The generated current is substantially independent from supply voltage.
- Micropower current reference based on this principle are also available.

Self-biased current reference

(V_{TH} + V_{ov})-based



- Built-in voltage:

$$V_{bi} = V_{GS1} = V_{TH} + V_{ov}$$

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 \qquad \text{(i.e. current mirror)}$$

$$I_1 = I_2 = \frac{k'}{2} \cdot \left(\frac{W}{L}\right)_1 \cdot (V_{GS1} - V_{TH})^2$$

$$R \cdot I_2 = R \cdot I_1 = V_{GS1} = \sqrt{\frac{2 \cdot I_1}{k'} \left(\frac{L}{W}\right)_1} + V_{TH}$$

- Typically V_{ov} is designed to be much smaller than V_{TH} in order to have:

$$I_1 \approx \frac{V_{TH}}{R_1}$$

- Low currents can be generated using large resistor (V_{TH}+V_{ov} in the range of 1 V)

Temperature dependence

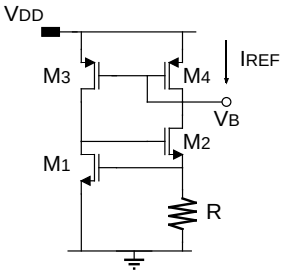
- R_1: positive TC
- V_{TH}: negative TC
- V_{ov}: positive TC (|(V_{TH}) + |V_{ov}|: negative TC)

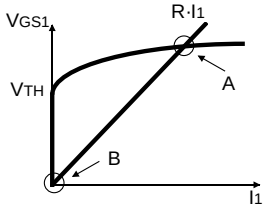
- Complementary structure is always possible

Self-biased current reference

(V_{TH} + V_{ov})-based

Start-up circuit





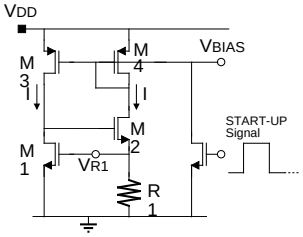
$I_1 = I_2$ (for M_3-M_4 mirror)

$$\frac{V_{GS1}}{R_1} = \frac{k'}{2} \cdot \left(\frac{W}{L}\right)_1 \cdot (V_{GS1} - V_{TH})^2$$

- Two operating points are possible (A, B) : only one (A) is the desired one

- It is necessary to use a start–up circuitry to set the desired operating point *(i.e.* to ensure I ≠ 0 at the start-up)

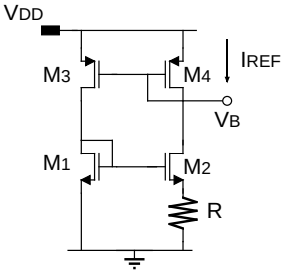
Possible start-up circuit solution



- At start-up, MS is turned on, thus forcing M4 in the saturation region. Then it is definitively turned off.

Self-biased low-current reference generator

ΔV_{ov}-based



Built-in voltage: $\Delta V_{ov} = V_{ov1} - V_{ov2}$

$$\left(\frac{L}{W}\right)_3 = \left(\frac{L}{W}\right)_4 ; \left(\frac{L}{W}\right)_1 = m \cdot \left(\frac{L}{W}\right)_2 \quad ; \; m > 1$$

- M_3-M_4 is an ideal current mirror => $I_3 = I_4 = I_1 = I_2 = I_{REF}$
- $V_{TH1} = V_{TH2}$

$$\sqrt{\frac{2 \cdot I_{REF}}{k'} \left(\frac{L}{W}\right)_1} = \sqrt{\frac{2 \cdot I_{REF}}{k'} \left(\frac{L}{W}\right)_2} + R \cdot I_{REF}$$

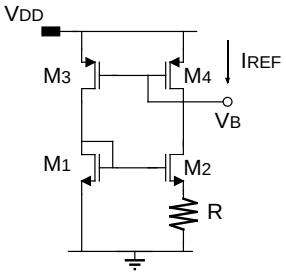
$$\sqrt{I_{REF}} = \frac{1}{R_1} \sqrt{\frac{2}{k'} \frac{1}{(W/L)_1}} \left(1 - \frac{1}{\sqrt{m}}\right)$$

- ΔV_{ov} generally ranges from tens to hundreds mV
- Small currents can be obtained with not very large R
- For m=10, $V_R \cong 60$ mV if it is required I = 1 μA

  => R = 60kΩ

Self-biased low-current reference generator

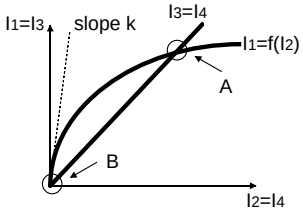
ΔV_{ov}-based



Temperature dependence:

- R_1: positive TC
- ΔV_{ov}: positive TC.

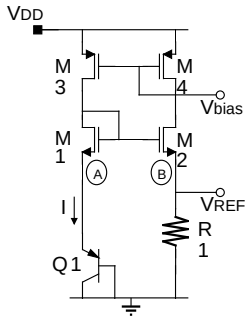
- Also for this circuit a start-up circuit is necessary



Complementary structure also available:

- M3, M4 n-channel transistors (source connected to V_{SS});
- M1, M2 p-channel transistors (source of M1 connected to V_{DD});
- R1 connected between source of M2 and V_{DD};
- in n-well processes, M1 and M2 in the same well.

V_{BE}-based current reference



Q1 is a substrate BJT

M1 to M4 operate in saturation region (improved Wilson current mirror)

$$(W/L)_3 = (W/L)_4,\ (W/L)_1 = (W/L)_2$$

$$I_1 = I_2 = I_{REF} = I$$

$V_{GS1} = V_{GS2} \Rightarrow$ $V_{S1} = V_{S2} \Rightarrow$ $V_{REF} = V_{EB}$

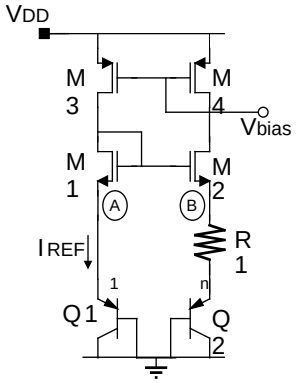
$$I = \frac{V_{EB}}{R_1}$$

- To generate low currents, a large R_1 is needed (V_{EB} in the range of 0.6 V)
- Start-up circuitry is needed
- Use the complementary structure for p-well processes

Temperature dependence:
- R_1: positive TC
- V_{EB}: negative TC

V_T-based current reference

(ΔV_{BE}-based current reference)



Built-in voltage:

$\Delta V_{EB} = V_{EB1} - V_{EB2} = V_T \ln(n)$

- Q1, Q2: substrate BJT with different emitter areas:

$$A_{Q2} = nA_{Q1} \quad n > 1$$

$$\left(\frac{L}{W}\right)_1 = \left(\frac{L}{W}\right)_2 ; \left(\frac{L}{W}\right)_3 = \left(\frac{L}{W}\right)_4$$

$$I_1 = I_2 = I_{REF} ; V_A = V_B$$

$$V_{EB1} = V_T \cdot \ln \frac{I_1}{I_{SS}}$$

$$V_{EB2} = V_T \cdot \ln \frac{I_2}{nI_{SS}}$$

$$R_1 \cdot I_{REF} = V_{EB1} - V_{EB2} = V_T \cdot R_1 \cdot \ln(n)$$

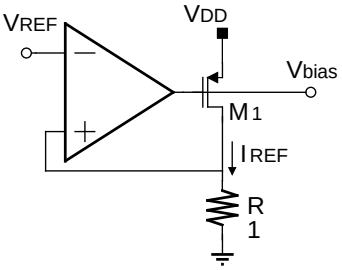
$$I_{REF} = \frac{V_T}{R_1} \cdot \ln(n)$$

- Small currents can be obtained with small R_1

Temperature dependence:
- R_1: positive TC
- V_T: positive TC

- Start-up circuitry is needed
- Complementary structure available only in a p-well processes

Current references based on a reference voltage



- Useful when a reference voltage is available.

- This circuit has to operate at low-frequency (dc). The opamp gain can be extremely large.

$$I_{REF} = \frac{V_{REF}}{R_1}$$

- M1 in saturation region, for current mirror

Temperature dependence:
- R_1: positive TC
- V_{REF}: depends on the kind of voltage reference used

- It is difficult to obtain a stable V_{REF} with a small value.
  => Low reference currents need large R_1

Voltage references

Introduction

- Voltage references are required in a number of analog applications (e.g. signal processing, A/D converters, D/A converters, ...).

- Different voltage references

  Supply voltage dividers

  Voltage references based on a built-in voltage

  Voltage references based on the band-gap voltage

  Voltage references based on MOS threshold voltage difference

  (the last two types are actually special kinds of voltage references based on a built-in voltage).

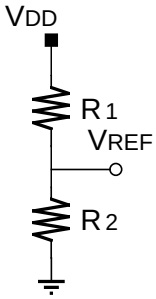
- In the following, all voltages will be referred to GND

- Features for a reference current
  Supply dependence
  Temperature dependence
  Technology dependence

Supply voltage divider

Resistive dividers

- Analog circuits normally have only two dc voltage supplies (V_{DD} and ground)
- In order to obtain dc-bias voltages, voltage dividers can be used



$$V_{REF} = \frac{R_2}{R_1 + R_2} \cdot V_{DD} = \alpha \cdot V_{DD}$$

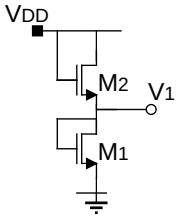
with $\alpha < 1$

- Large power dissipation (small resistors) or large silicon area occupation (large resistors).
- V_{REF} depends on supply voltage.
- To obtain good matching, R_1 and/or R_2 area realized by means of a suitable number of unity resistors

Supply voltage divider

Diode-connected NMOS transistors

- Resistive or capacitive dividers are complex or silicon area consuming
- MOS in the diode configuration (i.e. operwting in saturation region) can be used



$$\frac{k'}{2} \cdot \left(\frac{W}{L}\right)_1 \cdot (V_{DS1} - V_{TH1})^2 = \frac{k'}{2} \cdot \left(\frac{W}{L}\right)_2 \cdot (V_{DS2} - V_{TH2})^2$$

$$V_{DS1} + V_{DS2} = V_{DD}$$

$$V_1 = V_{DS1} = \frac{\alpha_2}{\alpha_1 + \alpha_2} \cdot V_{DD} + \frac{\alpha_1 \cdot V_{TH1} - \alpha_2 \cdot V_{TH2}}{\alpha_1 + \alpha_2}$$

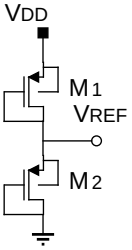
$$\alpha_1 = \sqrt{\left(\frac{W}{L}\right)_1} \quad ; \quad \alpha_2 = \sqrt{\left(\frac{W}{L}\right)_2}$$

It results a voltage division of V_{DD} plus an offset.

Body effect on M2 can affect the operation ($V_{TH1} \neq V_{TH2}$)

Supply voltage divider

Diode-connected PMOS transistors



- Body of M2 connected to source of M2 to avoid threshold voltage mismatches due to body effect

  Assuming $V_{TH1} = V_{TH2} \equiv V_{TH}$

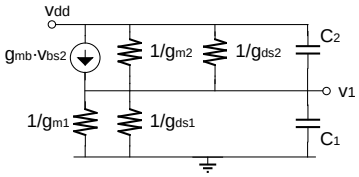
$$V_{REF} = V_{DS2} = \frac{\alpha}{1 + \alpha} \cdot V_{DD} + \frac{1 - \alpha}{1 + \alpha} |V_{TH}|$$

- Several diode-connected transistors can be connected in series, if allowed by the supply voltage ("diode chain") to reduce current level for a given V_{TH}

MOS Supply voltage divider

Disturbs on the supply

If a signal v_{dd} (usually undesired and so a disturb) is superposed to V_{DD}, the small signal equivalent circuit must be considered.



$$C_2 = C_{gs2}$$

$$C_1 = C_{gs1} + C_{db1} + C_{sb2}$$

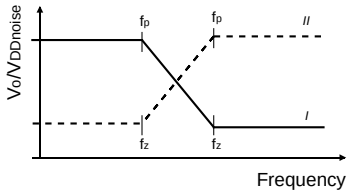
$$f_p = \frac{1}{2 \cdot \pi} \cdot \frac{g_{m1} + g_{m2}}{C_1 + C_2} \qquad f_z = \frac{1}{2 \cdot \pi} \cdot \frac{g_{m2}}{C_2}$$

At low frequency (assuming $g_{m2} >> g_{ds2}$ and $g_{m1} >> g_{ds1}$) there is a resistive partition (no capacitance effect):

$$v_{1lf} = v_{dd} \cdot \frac{1/g_{m1} + \frac{g_{mb}}{g_{m1} \cdot g_{m2}}}{1/g_{m1} + 1/g_{m2} + g_{mb}/(g_{m1} \cdot g_{m2})}$$

At high frequency there is a capacitive partition (no resistance effect)

$$v_{1hf} = v_{dd} \cdot \frac{C_2}{C_1 + C_2}$$



One of the two lines is valid depending if

$v_{1lf} > v_{1hf}$ (line I)

or

$v_{1lf} < v_{1hf}$ (line II)

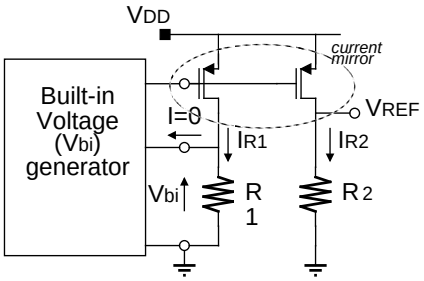
It results a noise injection from the power supply (V_{DD})

Voltage references based on a built-in voltage

Basic principle

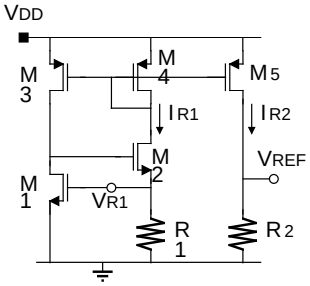
- Extraction of the chosen built-in voltage V_{bi}
- Generation of a current $I_{R1} = V_{bi}/R_1$
- Generation of a mirrored current $I_{R2} = kI_{R1}$
- Generation of the reference voltage V_{REF} forcing I_{R2} across a resistor R_2, matched with R_1

$$V_{REF} = R_2 \cdot I_{R2} = R_2 \cdot k \cdot I_{R1} = k \cdot \frac{R_2}{R_1} \cdot V_{bi}$$



- Extraction of the bult-in voltage as in current references based on a built-in voltage
- Temperature dependence of V_{REF}: it is a function of the temperature dependence of V_{bi}

$(V_{TH}+\Delta V_{ov})$-based voltage reference



- Built-in voltage: $V_{th} + V_{ov}$
- M1 to M5 in saturation region

$$(W/L)_3 = (W/L)_4 \rightarrow I_3 = I_4 = I_1 = I_2 = I_{R1}$$

$$(W/L)_5 = k\,(W/L)_4 \rightarrow I_{R2} = k\,I_{R1}$$

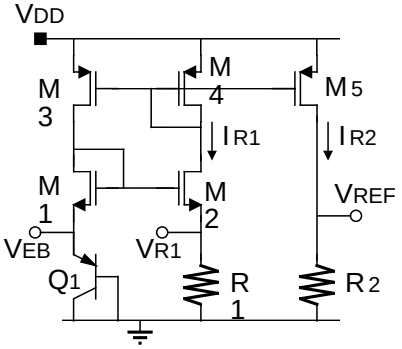
$$V_{REF} = k\frac{R_2}{R_1}V_{R1} = k\frac{R_2}{R_1}(V_{TH} + V_{ov})$$

- Generally V_{ov} is made much smaller than V_{TH}

Temperature dependence:
- V_{TH}: negative TC
- V_{ov}: positive TC ($|(V_{TH}) + |V_{ov}|$: negative TC)

Start-up circuitry needed
Complementary structure available

V_{BE}-based voltage reference



Built-in voltage: V_{BE}

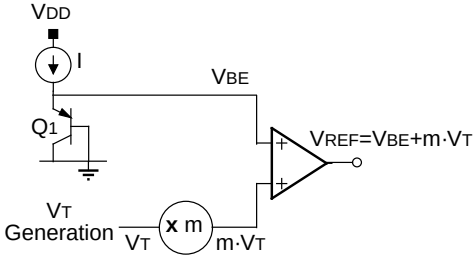
M1 to M5 in saturation region

$$(W/L)_3 = (W/L)_4 \Rightarrow I_3 = I_4 = I_{R1}$$
$$(W/L)_1 = (W/L)_2 \Rightarrow V_{R1} = V_{EB}$$
$$(W/L)_5 = k\,(W/L)_4 \Rightarrow I_{R2} = k \cdot I_{R1}$$
$$V_{REF} = k \cdot \frac{R_2}{R_1} \cdot V_{R1} = k \cdot \frac{R_2}{R_1} \cdot V_{EB}$$

Temperature dependence:
- V_{BE}: negative TC.

- Start-up circuitry needed.
- Complementary structure for p-well processes.

Voltage references based on the band-gap voltage



Basic principle

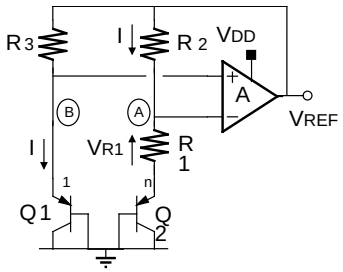
$$V_{REF} = V_{BE} + m \cdot V_T$$

where $V_T = kT/q$ is the thermal voltage.

- Suitable choice of m to have zero TC at the desired operating temperature.
- At room temperature (T = 300 K):
  V_{BE}: temperature dependence = ~–2.2 mV/°C
  V_T: temperature dependence = ~+0.086 mV/°C.
- If m = ~25.6 we have zero TC for V_{REF}
- At T = 300 K we have:

$$V_{REF} = V_{BE} + 25.6V_T = \sim 1.26\ V$$
(silicon band-gap)

Band-gap voltage reference



- Q1, Q2: substrate BJT with different emitter areas

$A_{Q2}=n\cdot A_{Q1}$
$n > 1$

$$V_A = V_B$$

$$R_2 = R_3 \Rightarrow I_{R2} = I_{R3} = I = I_{Q1} = I_{Q2}$$

$$V_{R1} = V_{EB1} - V_{EB2} = V_T \cdot \ln(n)$$

$$I = \frac{V_{R1}}{R_1} = V_T \cdot \frac{\ln(n)}{R_1}$$

$$V_{REF} = V_{EB1} + \frac{R_2}{R_1} \cdot V_T \cdot \ln(n)$$

$$V_{REF} = V_{EB1} + m \cdot V_T$$

where

$$m = \frac{R_2}{R_1} \cdot \ln(n) = \frac{R_2}{R_1} \cdot \ln\left(\frac{A_{Q2}}{A_{Q1}}\right)$$

For ambient temperature:

$$m = \sim 25.6.$$

Example:

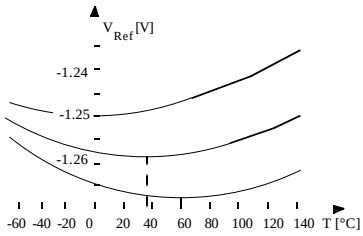
$n = 8 \Rightarrow A_{Q2} = 8A_{Q1}$ *(easy to obtain in layout)*

$$R_2 = R_3 = \sim 12.3\ R_1$$

Band-gap voltage reference

Compensation of temperature dependence

- first-order
- small temperature range.



- For better compensation, more complex schemes are used.
- Scheme sensitive to offset v_{off} of the operational amplifier:

$$V_{REF} = V_{EB1} + \left(1 + \frac{R_2}{R_1}\right) v_{off} + \frac{R_2}{R_1} V_T \ln\left[n\left(1 + \frac{v_{off}}{I_2 R_2}\right)\right]$$

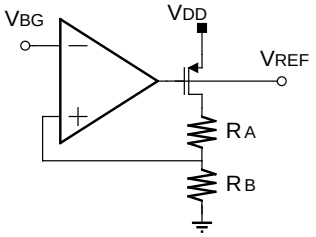
- Different (but matched) resistors R_2 and R_3 can also be used:

$$m = \frac{R_2}{R_1} \cdot \ln\left(\frac{R_3}{R_2} \cdot \frac{A_{Q2}}{A_{Q1}}\right)$$

- Generally, start-up circuitry is required.
- Similar configuration for p-well processes

Band-gap voltage reference

Band-gap voltage multiplier

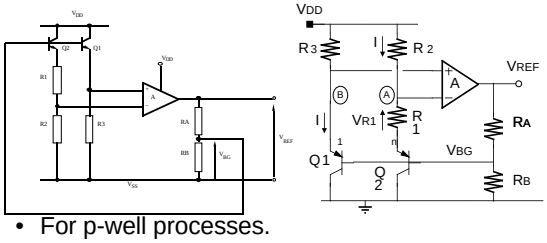


- To be used when $V_{REF} > 1.26$ V is required

$$V_{REF} = V_{BG}\left(1 + \frac{R_A}{R_B}\right)$$

where V_{BG} is the band-gap voltage.

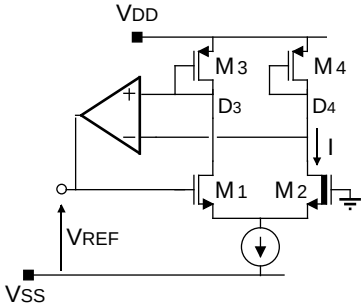
- The multiplier can be included in the feedback loop.



- For p-well processes.

$$V_{REF} = V_{BG}\left(1 + \frac{R_A}{R_B}\right)$$

Voltage references based on MOS threshold voltage difference



- M1 and M2: transistors with equal k' and different threshold voltages, e. g.:
  - both enhancement transistors with different V_{TH}
  - one enhancement and the other depletion transistor
- M1 to M4 in saturation region

$V_{D3} = V_{D4}$ $(W/L)_3 = (W/L)_4$ $k'_3 = k'_4$

It follows that: $I_3 = I_4 = I_1 = I_2 \equiv I$

$$(W/L)_1 = (W/L)_2 \rightarrow V_{ov1} = V_{ov2}$$

$$V_{REF} = -V_{GS2} + V_{GS1} = -V_{TH2} - V_{ov2} + V_{TH1} + V_{ov1}$$

$$V_{REF} = V_{TH1} - V_{TH2} \equiv \Delta V_{TH}$$

- ΔV_{TH} is generally small. A voltage multiplier is required.
- Spread in threshold voltages, hence in ΔV_{TH}
- Offset of the operational amplifier affects V_{REF}