A Novel Method of Diode Clamped Multi-Level Inverter using PWM Technique

N. Mohan Teja, R S Ravi Sankar, P. Harsha, V. Uma Shankar

Abstract— This Paper presents a novel method of Diode clamped Multi Level Inverter, which works without series association the clamping diodes. The conventional diode clamping inverter suffers from such problems as dc link unbalance, indirect clamping of the inner devices, turn-on snubbing of the inner dc rails as well as series association of the clamping diodes etc. It is due largely to these problems that the application of the conventional diode clamping inverter in practice has been deterred, in spite of the growing discussion in the literature. An auxiliary resistive clamping network solving the indirect clamping problem of the inner devices is also discussed for both the new and conventional diode clamping inverter. Operation principle, clamping mechanism, auxiliary clamping as well as experimentation are presented.

Index Terms – Clamping Diodes, DC Link Unbalance, Multi Level Inverter ,Pulse Width Modulation

I. INTRODUCTION

The concept of multilevel converters has been introduced since 1975. The term multilevel began with the three-level converter. Subsequently, several multilevel converter topologies have been developed. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output. However, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected. A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM). The attractive features of a multilevel converter can be briefly summarized as follows. Staircase waveform quality: Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) problems can be reduced. Multilevel converters produce smaller Common-mode (CM) voltage. Therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Switching frequency: Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM.

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It should be noted that lower switching frequency usually means lower switching loss and higher efficiency. Response to the growing demand for high power inverter units, multilevel inverters have been attracting growing attention from academia as well as industry in the recent decade. Among the best known topologies are the H-bridge cascade inverter, the capacitor clamping inverter (imbricated cells), and the diode clamping inverter.

II. DIODE CLAMPED MULTI-LEVEL INVERTER

An m-level diode-clamp converter typically consists of m - 1 capacitors on the dc bus and produces m levels of the phase voltage. The above figure shows a single-phase full bridge five level diode-clamp converter in which the dc bus consists of four capacitors C_1, C_2, C_3, C_4. For a dc bus voltage V_{dc} the voltage across each capacitor is $V_{dc}/4$, and each device voltage stress will be limited to one capacitor voltage level, $V_{dc}/4$, through clamping diodes. If the inverter runs under pulse width modulation (PWM), the diode reverse recovery of these clamping diodes becomes the major design challenge. The basic five level diode clamped inverter is as shown in the Fig 1.

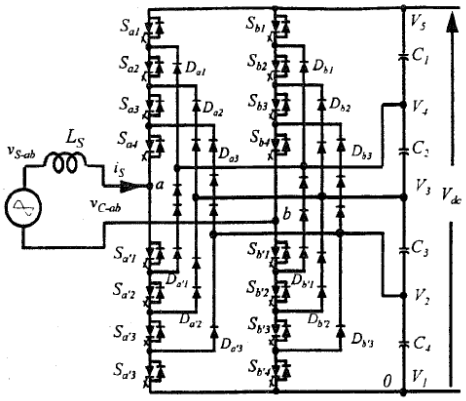

Fig. 1 Five Level Diode Clamped Inverter

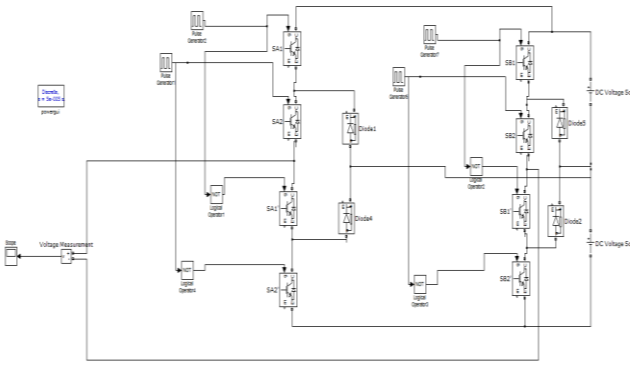

Fig. 2 Simulink of Five Level Inverter

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II. NEW DIODE CLAMPED MULTI LEVEL INVERTER

The new diode clamping inverter is shown in Fig. 2. For the five-level case, a total of eight switches and twelve diodes of equal voltage rating are used, which are the same with the conventional diode clamping inverter with diodes in series. This pyramid architecture is extensible to any level unless otherwise practically limited. A M-level inverter leg requires (M-1) storage capacitors, 2(M-1) switches and (M-1) clamping diodes

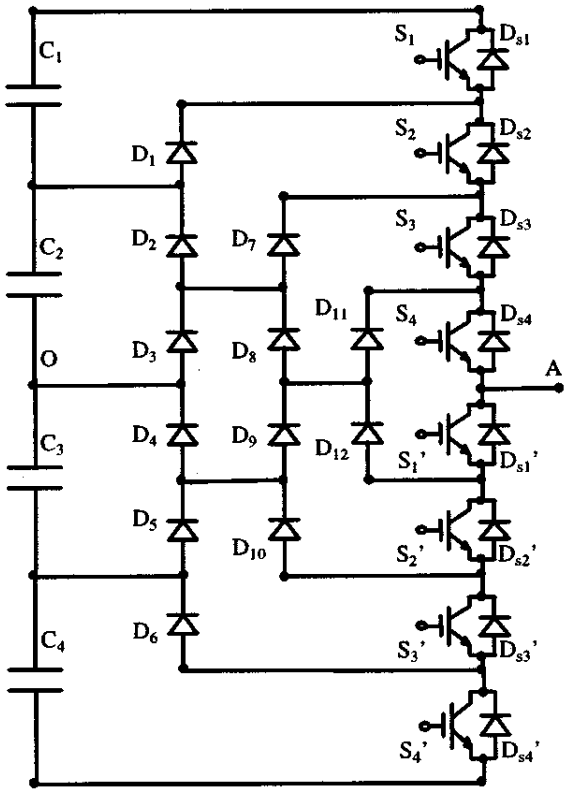

Fig. 3 Circuit Diagram of Five Level New Diode Clamped Inverter

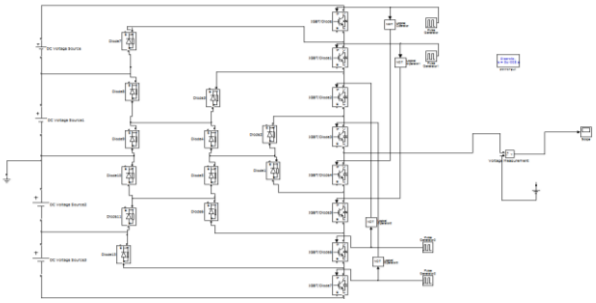

Fig. 4 Simulink of New Diode Five Level Inverter

III. SINUSOIDAL PULSE WIDTH MODULATION TECHNIQUE

For an m-level inverter, m-1 carriers with the same frequency fc and same peak-to-peak amplitude A_c are disposed such that the bands they occupy are continuous. The reference, or modulation, waveform has peak-to-peak amplitude A_m and frequency f_m, and it is centered in the middle of the carrier set. The reference is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the active device corresponding to that carrier is switched on and if the reference is less than a carrier signal, then the active device corresponding to that carrier is switched off. In multilevel inverters, the amplitude modulation index, m_a and the frequency ratio m_f are defined as

$$m_a = \frac{A_m}{(m-1)A_c} \qquad \textit{Equation – 1}$$

$$m_f = \frac{f_c}{f_m} \qquad \textit{Equation – 2}$$

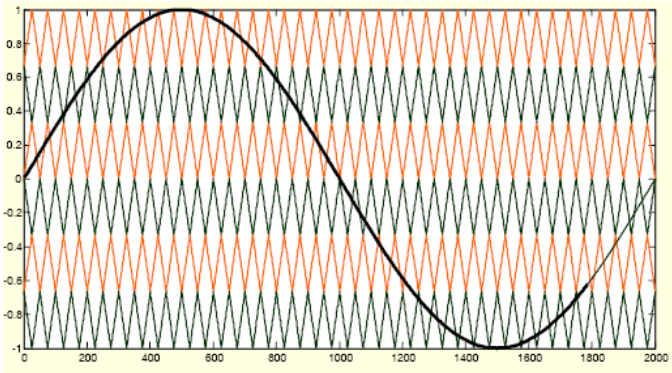

Fig. 5 Sinusoidal Pulse Width Modulation Technique

V. SIMULINK MODELS OF MULTILEVEL INVERTERS WITH PWM TECHNIQUE

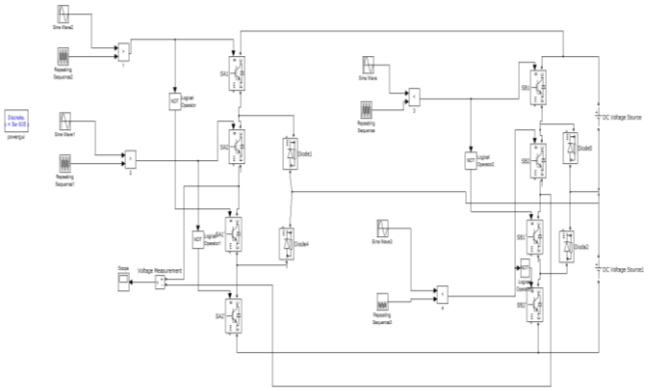

Fig. 6 Simulink of PWM based Five Level Diode Clamped Inverter

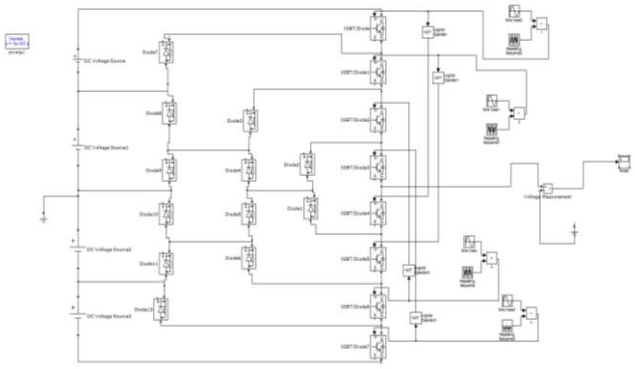

Fig. 7 Simulink of PWM based Five Level New Diode Clamped Inverter

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IV. SIMULATION RESULTS FOR DIODE CLAMPED INVERTER

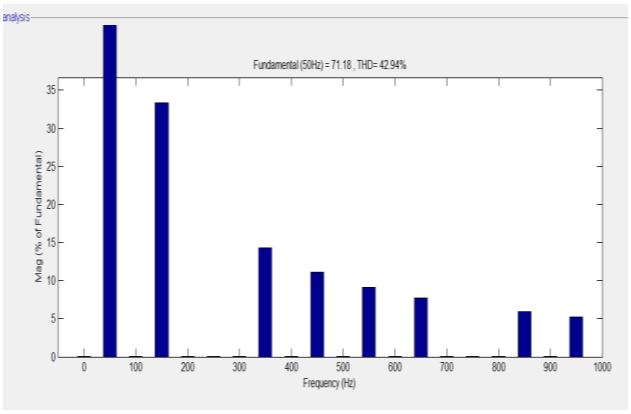

Fig. 8 THD of Five level Diode clamped inverter

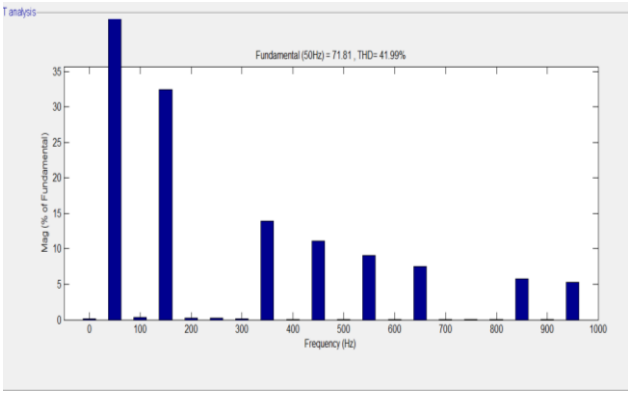

Fig. 9 THD of Five Level New Diode Clamped Inverter

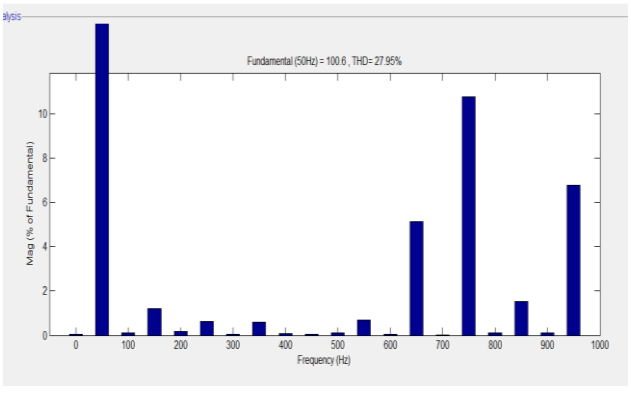

Fig. 10 THD of Five Level Diode Clamped Inverter with PWM Technique

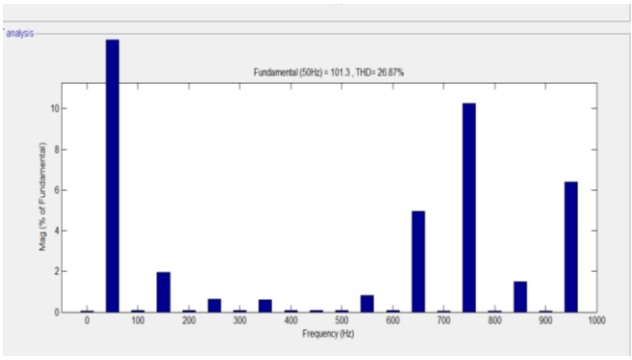

Fig. 11 THD of Five Level New Diode Clamped Inverter with PWM Technique

VI. WAVEFORMS OF DIODE CLAMPED AND NEW DIODE CLAMPED INVERTERS (FIVE LEVEL)

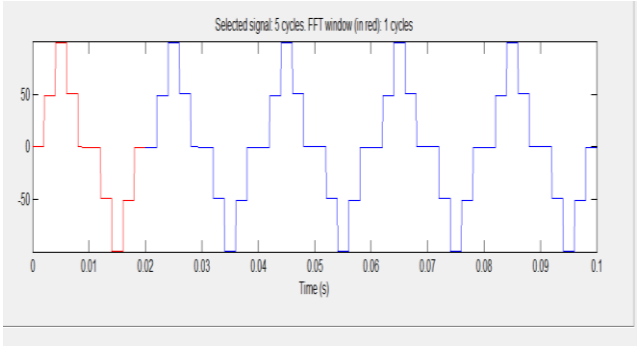

Fig. 12 Simulation Result for Line voltages of Five Level Diode Clamped Inverter

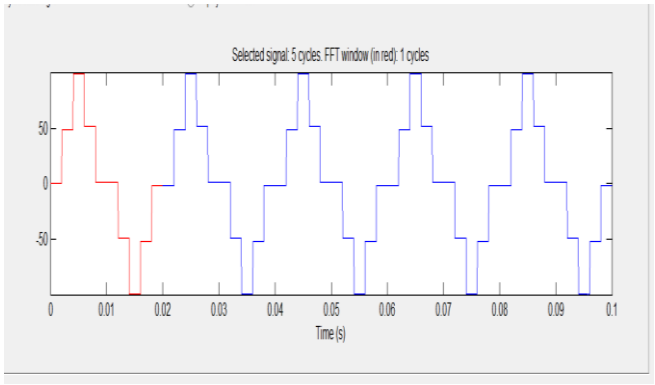

Fig. 13 Simulation Result for Line Voltages of Five Level New Diode Clamped Inverter

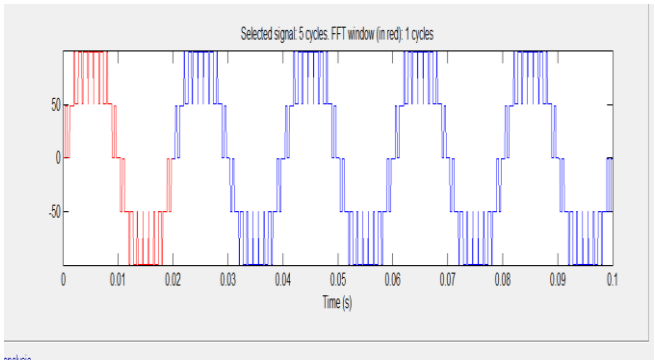

Fig. 14 Simulation Result for Line Voltages generated using PWM Technique of Five Level Diode Clamped Inverter

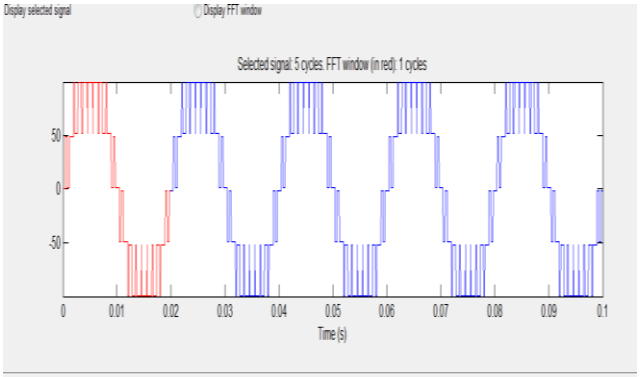

Fig. 18 Simulation Result for Line Voltages generated using PWM technique of Five Level New Diode Clamped Inverter

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VII. PERCENTAGE TOTAL HARMONIC DISTORTION ANALYSIS OF DIODE CLAMPED MULTILEVEL INVERTER WITH DIFFERENT LEVELS USING PWM

Diode clamped inverter (Levels)	%THD Without using PWM technique	%THD Using PWM technique
3 level	79.89	35.06
5 level	42.94	27.95
7 level	31.5	17.93
9 level	26.19	13.52

VIII. PERCENTAGE TOTAL HARMONIC DISTORTION ANALYSIS OF NEW DIODE CLAMPED MULTILEVEL INVERTER WITH DIFFERENT LEVELS USING PWM

Diode clamped inverter (Levels)	%THD Without using PWM technique	%THD Using PWM technique
3 level	79.43	33.98
5 level	41.99	26.87
7 level	30.25	16.93
9 level	24.62	12.45

IX. CONCLUSION

In this paper Pulse width modulation technique is applied on diode clamped and new diode clamped multilevel inverters and percentage of total harmonic distortions of several levels of inverter are simulated and compared. The simulated results are presented in this paper and it is concluded that PWM technique has given good fundamental spectrum (101.7%) and Total Harmonic Distortion (12.45%). As the number of levels increases the harmonic distortion also decreases. Comparing with the diode clamped multilevel inverter new diode clamped inverter has less Total Harmonic Distortion.

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