ARCHIVES OF ELECTRICAL ENGINEERING VOL. 65(3), pp. 481-493 (2016)

DOI 10.1515/aee-2016-0035

Common mode behavior in grid connected DC and AC decoupled PV Inverter topologies

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(Received: 08.10.2015, revised: 17.03.2016)

Abstract: The transformer-less grid connected inverters are gaining more popularity due to their high efficiency, very low ground leakage current and economic feasibility especially in photovoltaic systems. The major issue which surfaces these systems is that of common mode leakage current which arises due to the absence of an electrical transformer connected between the inverter and the utility grid. Several topologies have evolved to reduce the impact of common mode leakage current and a majority of them have succeeded in eliminating the impacts and have well kept them within the limits of grid standards. This paper compares and analyses the impact of the common mode leakage current for four popular inverter configurations through simulation of the topologies such as H5, H6, HERIC and FBZVR inverters.

Key words: distributed generation, common mode leakage current, solar PV systems, transformerless PV inverters

1. Introduction

The major highlight of Distributed Generation (DG) in recent years is attributed to Photovoltaic (PV) systems and its advancements due to the high demand for energy at affordable costs. Particularly photovoltaic inverters are becoming more popular in private and commercial circles since they convert the available PV array power to ac and supply to the utility grid. The rise in demand for PV integrated grid connected systems has also introduced several operational irregularities such as power quality issues due to high penetration levels of PV. Grid connected PV systems can be classified based on the transformer used between the inverter and the utility grid. The transformer can be a high frequency type in the DC side or low

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frequency at the AC side. The transformer provides galvanic isolation and eliminates the leakage current and thus avoiding the DC current injection into the grid. The main drawback of using the transformer is that it reduces the efficiency significantly. This has paved the way for transformer-less interconnection which is cost efficient, consumes less space and has higher energy efficiency. Since the galvanic isolation is retrieved in transformer-less interconnection the leakage current becomes higher and the PWM strategies and topologies adopted to reduce this current also becomes complex. Although transformer-less interconnection has some drawbacks its minimal operational costs overwhelm its drawbacks. The stray capacitance formed due to transformer less connection charges and discharges developing Common Mode Voltage (CMV) which is fluctuating in nature. This stray capacitance introduces high leakage currents, grid current ripples and the increased EMI losses [1].

The conventional bridge type inverters use bipolar modulation techniques in transformer-less PV systems to generate constant CMV which reduces the leakage current. Also the inductor size required is large to withstand the voltage stresses and hence the system cost and size increases. Several research papers have identified alternate methods to reduce CMV namely the topologies based on galvanic isolation such as H5, H6, HERIC and FBZVR which incorporate DC and AC decoupling to disconnect PV from the utility grid in which the AC decoupling is more efficient due to reduction of losses in the conduction path [1]. Due to the influence of junction capacitances of the semiconductor switches used and parasitic parameters, the elimination of leakage current and CMV by galvanic isolation proves ineffective in most cases. Due to these drawbacks the CMV clamping topologies were developed which uses primarily capacitances and diodes for voltage clamping [2].

In this paper four popular transformer-less topology are analyzed based on their ability to reduce the impact of ground leakage current or CMV. In section II the behavior of common mode leakage current is discussed using the fundamental and governing equations acceptable for a majority of inverters. Section III enunciates the circuit description and operation such as firing scheme and leakage current estimation using the MATLAB/Simulink environment. Section IV presents the comparison of these topologies with respect to performance indicators and section V deals with the conclusion and future scope.

2. Common mode behaviour

In the absence of the transformer connected at the AC side of the inverter a circuit is formed as shown in the detailed model in Fig. 1. The nature of this circuit formed is resonant which includes stray capacitance (C_{PV}), and leakage current (I_L), the filter inductors (L_1 and L_2). The capacitance appearing between the transformerless PV structures and the earth can vary greatly, depending on the PV panel construction and weather conditions. For the general representation of the several converter topologies, the converter is represented by a four terminal block. In the detailed model the power converter can be modeled as two voltage sources V_{AN} and V_{BN} regardless of the structure of the converter.

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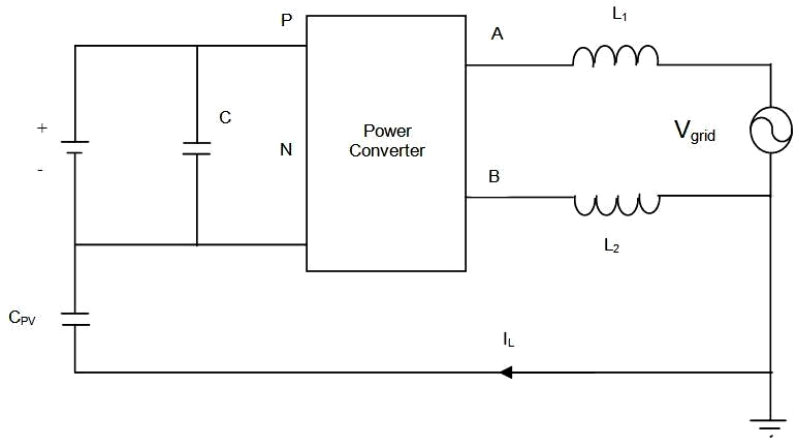

Fig. 1. Full model of common mode model of single phase grid connected inverter

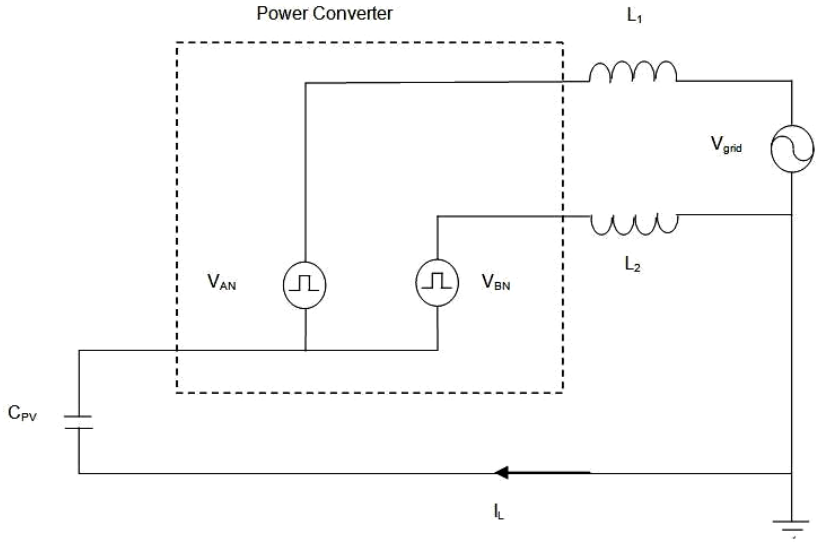

Fig. 2. Simplified model of common mode model of single phase grid connected inverter

In Fig. 3 the leakage current I_L is dependent on the voltages V_{AN}, $V_{BN,}$ V_{grid}, L_1, L_2 and stray capacitance.

The common mode voltage, V_{CM} and the differential-mode voltage V_{DM} can be expressed as [3, 4].

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2}, \tag{1}$$

$$V_{DM} = V_{AN} - V_{BN}. \tag{2}$$

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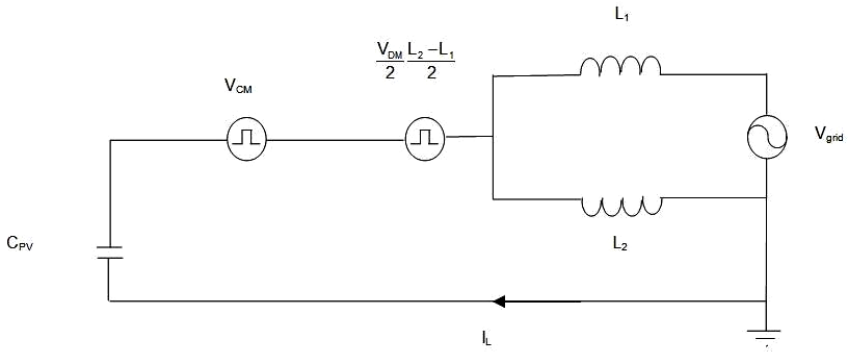

Fig. 3. Simplified common mode model

From Equations (1) and (2), expressing the output voltages in terms of V_{CM} and V_{DM} as

$$V_{AN} = V_{CM} + \frac{V_{DM}}{2}, \tag{3}$$

$$V_{BN} = V_{CM} - \frac{V_{DM}}{2}. \tag{4}$$

Using Equations (3)-(4) the voltages expressed in the left hand side are modeled as a voltage source in a simplified common-mode model as shown in Fig. 3. The equivalent C_{MV} (V_{ECM}) is defined as

$$V_{ECM} = V_{CM} + \frac{V_{DM}}{2}\frac{L_2 - L_1}{L_1 + L_2}. \tag{5}$$

If the filter inductors are identical ($L_1 = L_2$) then $V_{ECM} = V_{CM}$

$$V_{ECM} = V_{CM} = \frac{V_{AN} + V_{BN}}{2}. \tag{6}$$

The power converter topology and the modulation technique should be chosen such that the common mode voltage is eliminated since the leakage currents are highly dependent on CMV. Fig. 2 is generally used to represent common mode behavior in the topologies which are to be discussed in the following sections. The values of V_{AN} and V_{BN} will however be different for the various topologies discussed and hence the V_{CM} and V_{DM} will be different.

The effect of parasitic capacitance between the PV array and the Utility grid in the transformer-less PV inverters allows the leakage current to flow through the system and hence galvanic isolation is necessary to reduce the effect of this hazard. Galvanic isolation can be broadly classified into two categories such as dc-decoupling and ac-decoupling methods. During the freewheeling period the PV array and the utility grid are disconnected by the action of bypass switches added on the dc side. In certain topologies the output current may flow through these bypass switches, being the predominant conduction path, leading to increase in

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conduction losses. In order to limit these shortcomings the bypass branch may be suitably provisioned on the ac side of the inverter, also known as the ac-decoupling method. Due to this inherent property of ac-decoupling methods it is found that these methods are more efficient than dc-decoupling methods. CMV cannot be controlled by the PWM technique employed during the freewheeling period since during this period the voltages V_{AN} and V_{BN} are floating with respect to the input capacitor and the CMV oscillates corresponding to the values of parasitic parameters, junction capacitance of switches and the topology employed and hence the leakage current still flows. A clamping branch is introduced in the FBZVR topology for the reduction of CMV during a freewheeling period. The effect of the clamping branch is discussed in the operation and performance analysis of this topology in the successive sections of this paper [13].

3. Operating principle of PV inverters

3.1. H5 topology

The H5 inverter topology invented by SMA Technologies was developed exclusively as a grid tied inverter for Distributed Generation systems without galvanic isolation. High efficiency, reduced size and minimal leakage current are some of the features of this topology. The input to the inverter can be from a PV array source or a DC/DC converter with the MPPT algorithm employing change in voltage levels. Fig. 4 illustrates the example of a PV array fed H5 inverter topology.

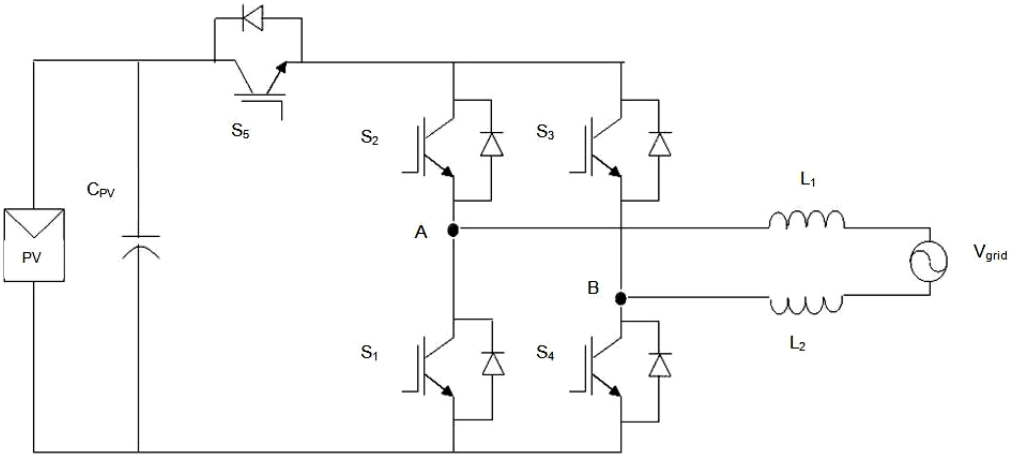

Fig. 4. Circuit diagram of H5 inverter

This topology is the modified form of the conventional full bridge topology with an extra switch S_5 which serves as the dc decoupling agent. The switches S_1 and S_3 are operated at fundamental grid frequency and the switches S_2 and S_4 are operated at high switching frequency. The H5 inverter has four operating modes namely, Mode 1: Active Conduction mode

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in positive half period, Mode 2: Freewheeling mode in positive half period, Mode 3: Active Conduction mode in negative half period, Mode 4: Freewheeling mode in negative half period. The active power is delivered to the utility grid from the dc bus during the positive and negative half periods by the action of switch S_5 which is in the ON state in modes 1 and 3. During mode 2 and 4 the inverter free wheels the current to provide continuity of supply to the utility grid since the switch S_5 is now in the OFF state.

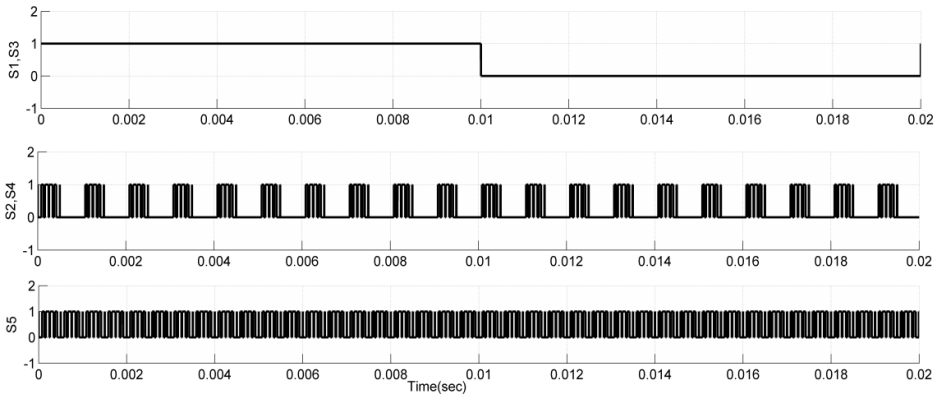

Fig. 5. PWM firing scheme for the switches $S_1 - S_5$ for H5 topology

Due to the presence of parasitic capacitance in the PV array the ground leakage current is reduced during the freewheeling operation which avoids high frequency voltage variations at the DC bus terminal [7]. An appropriate PWM strategy is necessary to control the injected current into the utility grid. Many literatures have highlighted the features of a ramp comparison method or sinusoidal PWM (SPWM) since the filter design with this technique can be easily realized. However according to the nature of the load the system stability and dynamic response is largely deteriorated which leads to rise in phase error and amplitude [7]. Fig. 5 illustrates the firing scheme adopted for the topology for the switches S_1 to S_5. Fig. 6 illustrates the common mode leakage current prevalent in this topology.

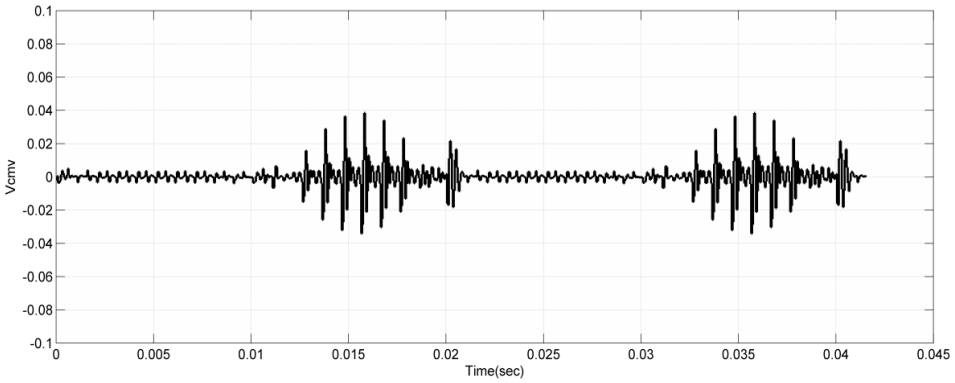

Fig. 6. Common mode leakage current in H5 topology

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3.2. H6 topology

The H6 topology is derived by introducing a switch in the dc side of the inverter as shown in Fig. 7. This switch S_6 is connected between the positive terminal of the PV array and the node B as shown in the H5 inverter topology to form a new current path.

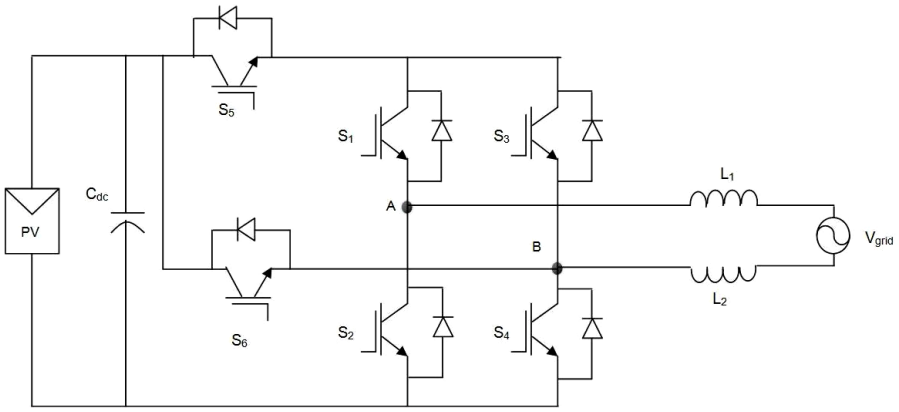

Fig. 7. Circuit diagram of H6 topology

Similar to the previous H5 topology, H6 also has four operating modes which are briefed below. In the Active Conduction mode in the positive half period of operation, the switch S_1 is turned ON at the grid frequency and switches S_4 and S_5 are switched at a higher frequency [8, 9]. As a result the power is delivered to the utility grid through the current path thus formed by the switching action of the above mentioned switches. In the freewheeling mode of the positive half period the switch S_1 is turned ON and current freewheels through the anti-parallel diode of the switch S_3 and S_1. In the Active Conduction mode in the negative half period of operation, the switch S_3 is turned ON at the grid frequency and switches S_2 and S_6 are switched at a higher frequency. As a result the power is delivered to the utility grid through the current path thus formed by the switching action of the above mentioned switches.

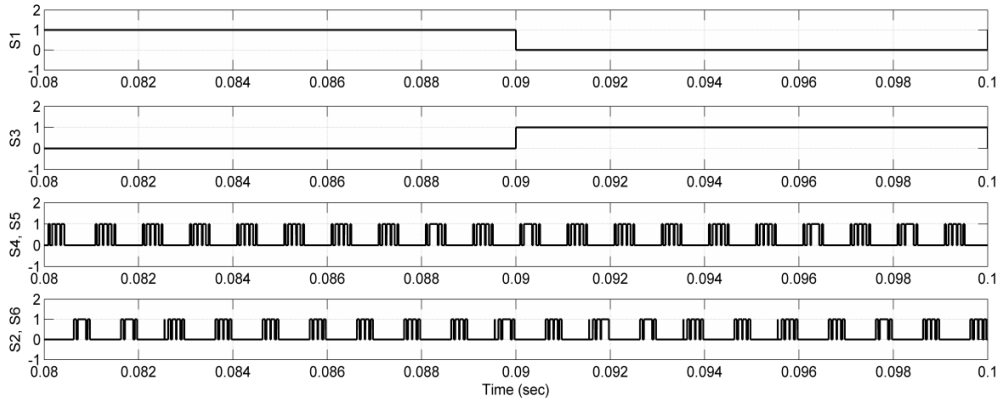

Fig. 8. PWM firing scheme for the switches $S_1 - S_6$ for H6 topology

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Although the switch S_3 is turned ON, it does not conduct and hence there is a reduction in the conduction losses in this mode compared with the H5 topology. In the freewheeling mode in the negative half period of S_3 operation and the anti-parallel diode of S_1 conduct to freewheel the current flowing through the utility grid.

The PV array is temporarily disconnected from the utility grid at the instant when the output voltage is at zero voltage level and hence the leakage current path is cut-off for that particular period. The H6 topology can achieve a unity power factor and also can control the phase shifts between current and voltage waveforms with the uni-polar SPWM firing scheme. The conduction loss of the H6 topology is higher than HERIC topology and less than H5 topology.

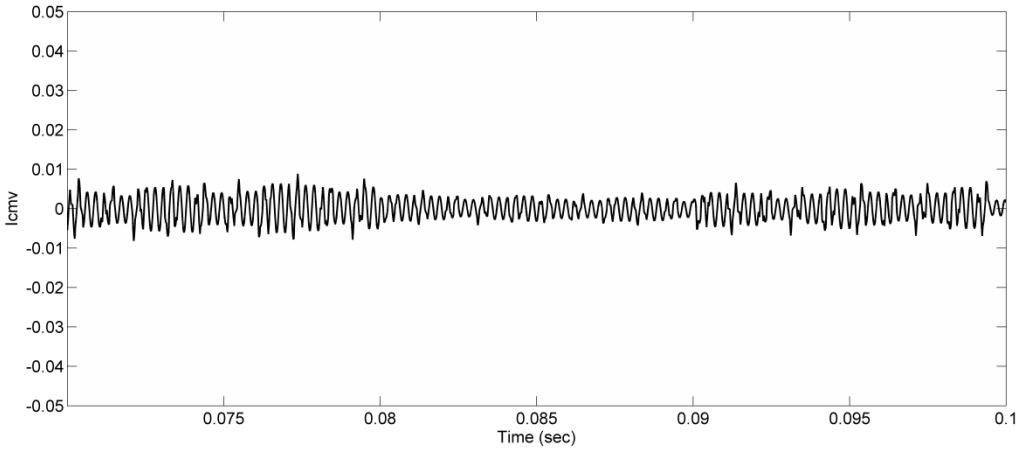

Fig. 9. Common mode leakage current in H6 topology

3.3. HERIC topology

A Highly Efficient and Reliable Inverter Concept (HERIC) is designed by adding two extra switches connected across the AC output side in a full bridge inverter. Each pair of the diagonal switches is operated at high switching frequency during one half of the grid voltage [10]. Fig. 10 shows the circuit diagram of the HERIC topology. Similar to the H5 topology there are four operating modes available for the HERIC topology. They are Mode 1: Active Conduction mode in positive half period, Mode 2: Freewheeling mode in positive half period, Mode 3: Active Conduction mode in negative half period, Mode 4: Freewheeling mode in negative half period.

In the Active Conduction modes by the switching pair action of semiconductor devices S_1 to S_4, the power is supplied to the utility grid. In the freewheeling mode, the switch S_5 is turned ON during the positive half period and hence the current freewheels through the switch S_5 and the anti-parallel diode of the switch S_6. Similarly in the negative half period of the freewheeling mode, the switch S_6 is turned ON and the output current freewheels through the anti-parallel diode of the switch S_5 and the switch S_6.

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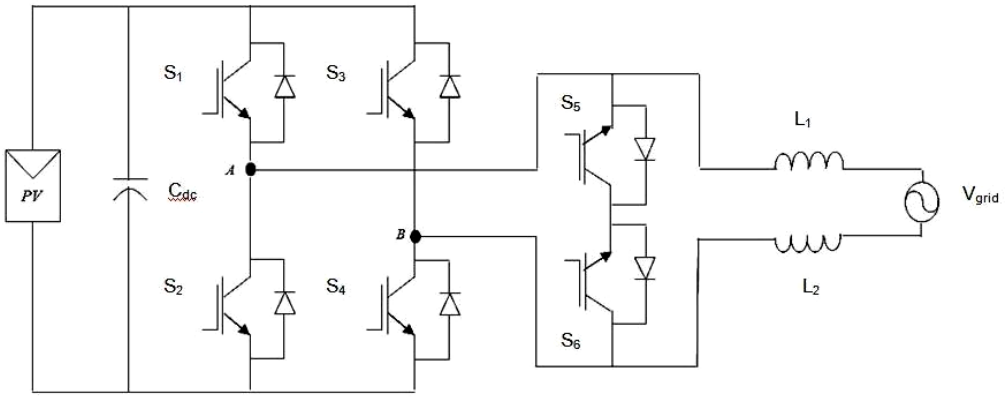

Fig. 10. Circuit diagram of HERIC topology

Thus AC voltage decoupling is accomplished by shorting the AC side of the inverter during zero voltage states. Fig. 11 illustrates the PWM firing schemes for the HERIC topology for switches S_1 to S_6. The effect of this decoupling has a major advantage that this prevents the output current to flow through the diodes of the full H-bridge. This topology maintains the voltage across the PV panel to be floating in nature and hence achieve a constant common mode voltage.

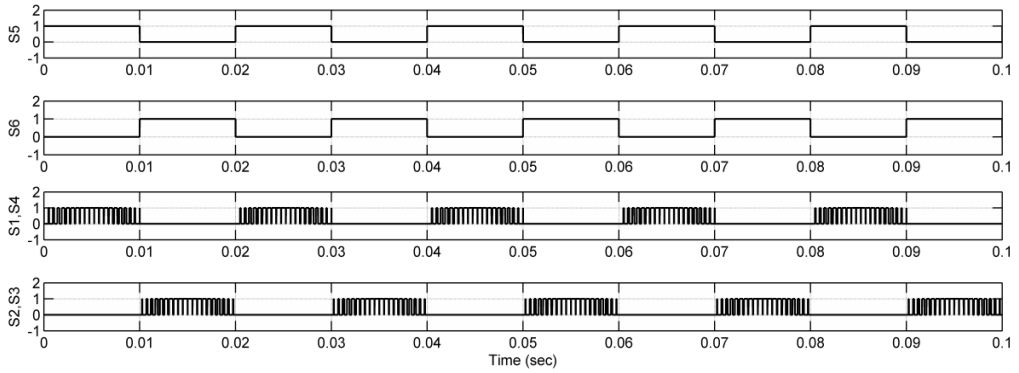

Fig. 11. PWM firing scheme for switches $S_1 - S_6$ for HERIC topology

The efficiency of the inverter is substantially increased, without affecting the common-mode behavior of the whole system. Since there is no common mode voltage generated, the leakage current through the parasitic capacitance would be very small. Fig. 12 illustrates the common mode leakage current for HERIC topology [10, 11].

The HERIC topology has been developed to exhibit inherently very high conversion efficiency over a wide working range compared to other topologies. The operation of the bidirectional switch with the grid frequency reduces switching losses than other topologies.

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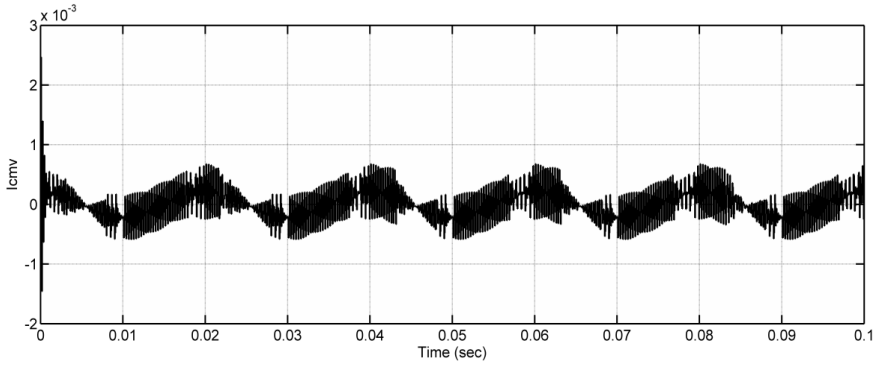

Fig. 12. Common mode leakage current for HERIC topology

3.4. FBZVR topology

Designed by Kerekes et al. [7], this modified topology that is suitable for the transformer-less PV system design is the Full Bridge Zero Voltage Rectifier (FBZVR) topology as shown in Fig. 13. A bi-directional short circuiting switch is implemented using a diode bridge rectifier, a semiconductor switch (S_5) and a clamping diode. The diode is clamped to the mid-point of the split source capacitance. Alternatively switching the diode bridge rectifier and the switch S_5, zero voltage state is achieved. During the Active Conduction mode in the positive half period the switches S_1 and S_4 supply the power to the utility grid. By turning ON the switch S_5 the zero voltage state is achieved.

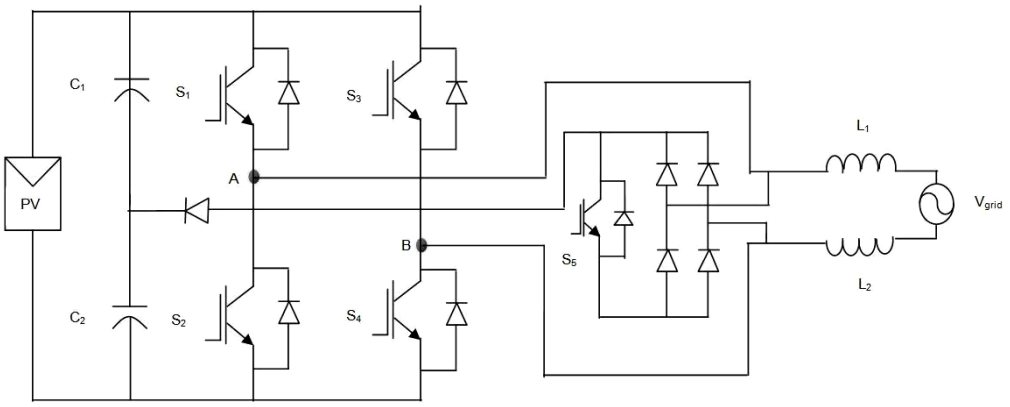

Fig. 13. Circuit diagram of FB-ZVR topology

The firing scheme for the switch pairs S_1, S_4 and S_5 are complementary allowing a small dead time to avoid shorting of the input capacitor. Similarly in the Active Conduction mode in negative half period the switches S_2 and S_3 deliver the power to the load. By switching ON S_5 using the complimentary gating signals of S_2 and S_3 the zero voltage state is achieved. The output of the inverter is clamped to the midpoint of the dc link.

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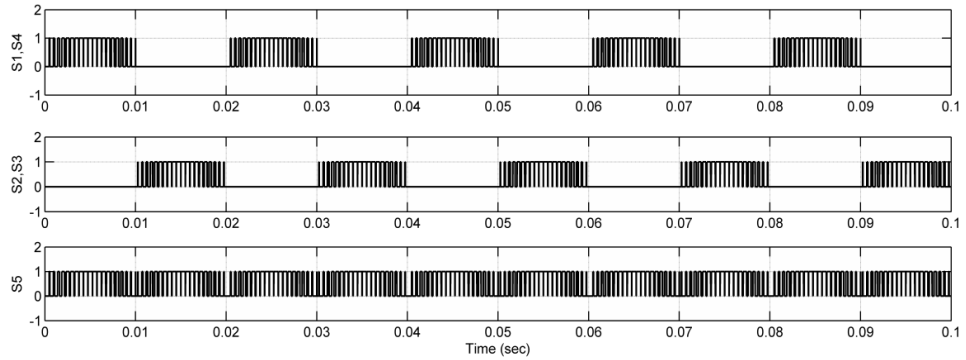

Fig. 14. PWM firing scheme for switches $S_1 – S_5$ for FBZVR topology

During the freewheeling period all the full bridge switches are turned OFF and the current freewheels through the anti-parallel diodes to reach the input capacitors. The load current ripple is less and the frequency of the current is equal to the switching frequency.

Fig. 14 shows the PWM firing scheme for switches S_1 to S_5 in case of the FBZVR topology. The common mode leakage current of the FBZVR topology is illustrated in Fig. 15. Since the firing scheme is uni-polar in nature the loss incurred in the filter circuit is less. Also the reactive power exchange between the filter passive elements and the dc link capacitance is almost zero during the zero voltage state. The main demerit of this topology is that it has an additional switch and four diodes for the operating modes.

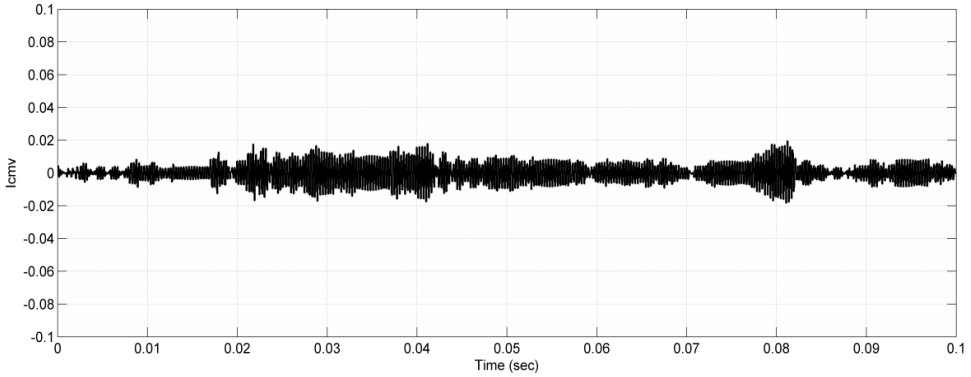

Fig. 15. Common mode leakage current for FBZVR topology

4. Results and discussions

For a common input DC voltage of $V_{dc} = 100$ V, $C_{dc} = 10$ μF, $L_1 = L_2 = 0.6$ H the maximum value of common mode leakage current was found from the above discussed topologies.

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Also the various differences between the topologies are highlighted in Table 1 as shown below. It is to be noted that for the same circuit configuration and power levels the AC decoupling topologies show efficient reduction in the value of common mode leakage current.

Harmonic currents, maximum current THD and DC current injection into the utility grid are some of the potential threats which are bound by standard put forth by leading organizations to reduce the impact of high penetration into the utility grid and thereby improve the power quality of the system.

Table 1. Comparison of various parameters between topologies

Parameters	Topology			
	H5	H6	HERIC	FBZVR
No. of switches	5	6	6	5
No. of diodes	0	2	0	5
Freewheeling witches	1	2	1	1
Switches in current path	3	4	2	2
Maximum efficiency(%)	95.2	93.6	97.3	96.1
Maximum leakage current	51 mA	26 mA	10 mA	40 mA

Table 2. Standards for grid connected Inverters

ISSUE	IEC61727	IEEE1547
Harmonic currents	(3-9) 4%	(2-10) 4%
	(11-15) 2%	(11-16) 2%
	(17-21) 1.5%	(17-22) 1.5%
	(23-33) 0.6%	(23-34) 0.6%
	–	(>35) 0.3%
Maximum current THD	5%	
DC current injection	Less than 1% of rated output current	Less than 0.5% of rated output current

5. Conclusion and future scope

This paper primarily focusses on the differences between the common mode behaviour prevalent in transformerless AC and DC decoupled photovoltaic inverters. The outcome of the results obtained from the simulation of the topologies suggest that the HERIC topology has the best efficiency with lowest leakage current values compared to the other counterparts followed by the FBZVR and H5 topologies. Even though the number of switches in the HERIC topology is higher compared to other topologies the AC decoupling ensures lower conduction losses by mitigating the effect of common mode behaviour. Although there has been a vast research carried out in the area of photovoltaic inverters in recent years, the nuances in the operation and the common mode behaviour in the AC and DC decoupled topologies has not been substantiated widely. In general the AC decoupled the PV inverter topologies fair better than their DC decoupled counterparts in many respects apart from the common mode behaviour.

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PV inverters are designed in such a way that their efficiencies are very high to balance the high cost incurred for the PV system design and erection. The above discussed topologies based on the DC and AC decoupling exhibit high efficiencies although this paper is restricted only to the common mode leakage current levels [13]. The evolution of the reduction of the common mode leakage current is either done by devising a proper switching scheme supplied to the switches or by designing a novel topology. The designing of newer inverter topologies with high efficiency even at irradiation level intermittencies is a challenge for the future grid connected PV inverter domain.

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