

International Journal on Electrical Engineering and Informatics - Volume 3, Number 1, 2011

Comparative Study on Carrier Overlapping PWM Strategies for Five Level Diode Clamped Inverter

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Abstract: This paper presents the comparison of Carrier Overlapping Pulse Width Modulation (COPWM) techniques for the Diode clamped Multi Level Inverter (DCMLI). Due to switch combination redundancies, there are certain degrees of freedom to generate the five level AC output voltage. This paper presents the use of Control Freedom Degree (CFD) combination. The effectiveness of the Pulse Width Modulation (PWM) strategies developed using CFD are demonstrated by simulation and experimentation. The results indicate that the multilevel inverter triggered by the developed COPWM-A strategy exhibits reduced harmonics. PWM strategies developed are implemented in real time using dSPACE/Real Time Interface (RTI). The simulation and experimental results closely match with each other validating the strategies presented.

Keywords: dSPACE, DCMLI, PWM, COPWM, CFD.

1. Introduction

Multilevel inverter has drawn tremendous interest in high power applications because it has many advantages: it can realize high voltage and high power output through the use of semiconductor switches without use of transformer and without dynamic voltage balance circuits. When the number of output levels increases, harmonics of the output voltage and current as well as Electro Magnetic Interference (EMI) decrease. Behera et al [1] described the harmonic analysis of the stepped output of the three level inverter based on number of triangular carriers and a sinusoidal modulating signal. The use of multilevel approach is believed to be a promising alternative in very high power conversion processing [2, 8]. Chaturvedi et al [3] presented simulation studies on different control techniques for three and five level DCMLI. The performance of each technique has been investigated based upon reduction in THD. Many investigators [4,10,13] have proposed carrier based multilevel sine triangle PWM schemes for control of a DCMLI used in a motor drive and in a static VAR compensator. Multilevel converters are rapidly emerging as viable alternatives for high power drives. A generalized circuit topology of multilevel voltage source inverter is proposed in [5]. Aquila et al [6] presented a digital implementation of DCMLI employing a fast microprocessor and logic circuits. Multilevel voltage source inverters have recently become very popular in applications using renewable energy sources such as fuel cell, photovoltaic cell and biomass etc [7]. The idea of control degrees of freedom combination and the validity of the PWM strategies are demonstrated by simulation and experimentation of three and five level inverters by Hongyan Wang et al [9]. This is based on a direct extension of three level inverter to higher level. Newton et al [11] discussed the control requirements for three and five level inverters.

Received: July 23rd, 2010. Accepted: March 8th, 2011

Samir Kouro et al [12] introduced multicarrier PWM with DC-link ripple feed-forward compensation for MLI. Sule Ozdemir et al [14] discussed the elimination of harmonics in a five level diode clamped multilevel inverter using fundamental modulation. Tolbert and Habetler [15] proposed novel carrier based PWM methods for multilevel inverter. Three kinds of novel PWM methods for multilevel inverter are analysed by Yang Deng et al [16]. This paper discusses a comparative study carried out on unipolar PWM strategies for chosen five level DCMLI both by simulation and real time implementation.

2. Diode Clamped Multilevel Inverter

Multilevel inverters are being considered for an increasing number of applications due to their high power capability associated with lower output harmonics and lower commutation losses. Multilevel inverters have become an effective and practical solution for increasing power and reducing harmonics of AC load. Diode clamped multilevel inverter is a very general and widely used topology. DCMLI works on the concept of using diodes to limit voltage stress on power devices. A DCMLI typically consists of (m-1) capacitors on the DC bus where m is the total number of positive, negative and zero levels in the output voltage. Figure1 shows a single phase half-bridge five level diode clamped inverter. The order of numbering of the switches is S1, S2, S3, S4, S1', S2', S3' and S4'. The DC bus consists of four capacitors C1, C2, C3 and C4 acting as voltage divider. For a DC bus voltage V_{dc} , the voltage across each capacitor is $V_{dc}/4$ and voltage stress on each device is limited to $V_{dc}/4$ through clamping diode. The middle point of the four capacitors 'n' can be defined as the neutral point.

The principle of diode clamping to DC-link voltages can be extended to any number of voltage levels. Since the voltages across the semiconductor switches are limited by conduction of the diodes connected to the various DC levels, this class of multilevel inverter is termed diode clamped MLI. Table 1 shows the output voltage levels and the corresponding switch states for the chosen five level DCMLI. The switches are arranged into 4 pairs (S1,S1'), (S2,S2'), (S3,S3'), (S4,S4'). If one switch of the pair is turned on, the complementary switch of the same pair must be off. Four switches are triggered at any point of time to select the desired level in the five level DCMLI.



Figure 1. Five level DCMLI

The steps to synthesis the five level output voltage in this work are as follows:

- 1. For an output voltage of $V_{an}=0$, two upper switches S3, S4 and two lower switches S1' and S2' are turned on.
- For an output voltage of V_{an}=V_{dc}/4, three upper switches S2, S3, S4 and one lower switch S1' are turned on.
- 3. For an output voltage of $V_{an}=V_{dc}/2$, all upper switches S1 through S4 are turned on.
- To obtain the output voltage of V_{an}= -V_{dc}/4, upper switch S4 and three lower switches S1', S2' and S3' are turned on.
- 5. For an output voltage of $V_{an} = -V_{dc}/2$, all lower switches S1' through S4' are turned on.

S1	S2	S 3	S4	S1'	S2'	S3'	S4'	V _{an}
1	1	1	1	0	0	0	0	$+V_{dc}/2$
0	1	1	1	1	0	0	0	$+V_{dc}/4$
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	-V _{dc} /4
0	0	0	0	1	1	1	1	-V _{dc} /2

Table 1. Switching scheme for single phase five level diode clamped inverter.

The output voltage V_{an} has five states: $V_{dc}/2$, $V_{dc}/4$, 0, - $V_{dc}/4$ and - $V_{dc}/2$. The gate signals for the chosen five level DCMLI are developed using MATLAB-SIMULINK. The gate signal generator model developed is tested for various values of modulation index. The results of the simulation study are presented in this work in the form of the PWM outputs of the chosen multilevel inverter. The PWM strategies developed are also implemented in real time using dSPACE/RTI system. The simulation and experimental results are compared and evaluated.

3. Carrier Based PWM Methods Based on CFD Combination

This paper focuses on carrier based PWM techniques which have been extended for use in multilevel inverter topologies by using multiple carriers. Multilevel carrier based PWM methods have more than one carrier that can be triangular waves or sawtooth waves and so on. As far as the particular carrier signals are concerned, there are multiple CFD including frequency, amplitude, phase of each carrier and offsets between carriers. The modulating / reference wave of multilevel carrier based PWM method can be sinusoidal or trapezoidal. As far as the particular reference wave is concerned, there is also multiple CFD including frequency, amplitude, phase angle of the reference wave and as in three phase circuits, the injected zero sequence signal to the reference wave. Therefore, multilevel carrier based PWM methods can offer multiple CFD. These CFD combinations combined with the basic topology of multilevel inverters can produce many multilevel carrier based PWM methods. This paper presents three COPWM methods that utilize the CFD of vertical offsets among carriers. They are: COPWM-A, COPWM-B and COPWM-C. The above three methods are simulated and implemented in this work.

For an m-level inverter using carrier overlapping technique, m-1 carriers with the same frequency f_c and same peak-to-peak amplitude A_c are disposed such that the bands they occupy overlap each other; the overlapping vertical distance between each carrier is $A_c/2$. The reference waveform has amplitude of A_m and frequency of f_m and it is centered in the middle of the carrier signals. The reference wave is continuously compared with each of the carrier

signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched on. Otherwise, the devices switch off. The amplitude modulation index m_a and the frequency ratio m_f are defined in the carrier overlapping method as follows:

$$m_a = A_m / ((m/4)^* A_c)$$

$$m_f = f_c / f_m$$

In this paper, $m_f = 21$, $A_c = 1.6$ and m_a is varied from 0.5 to 1. m_f is chosen as 21 as a trade off in view of the following reasons:(i) to reduce switching losses (which may be high at large m_f). (ii) to reduce the size of the filter needed for the closed loop control, the filter size being moderate at moderate frequencies. (iii) to effectively utilise the available dSPACE system for hardware implementation.

A. COPWM-A strategy

The vertical offset of carriers for five level inverter with COPWM-A method is illustrated in Figure 2. It can be seen that the four carriers are overlapped with other and the reference sine wave is placed at the middle of the four carriers.



Figure 2. Carrier arrangement for COPWM-A strategy

B. COPWM-B strategy

Carriers for five level inverter with COPWM-B method are shown in Figure3. It can be seen that they are divided equally into two groups according to the positive/negative average levels. In this strategy the two groups are opposite in phase with each other while keeping in phase within the group.



Figure 3. Carrier arrangement for COPWM-B strategy

C. COPWM-C strategy

Carriers for five level inverter with COPWM-C method are shown in Figure4. In this strategy, carriers invert their phase in turns from the previous one. It may be identified as PWM with amplitude-overlapped and neighbouring-phase-interleaved carriers. Actually, COPWM-B and COPWM-C can be looked on as a second control freedom degree change besides offsets in vertical: the carriers' have horizontal phase shift from COPWM-A.



Figure 4. Carrier arrangement for COPWM-C strategy

4. Simulation Results

The diode clamped five level inverter is modelled in SIMULINK using power system block set. Switching signals for diode clamped multilevel inverter using COPWM techniques are simulated.

Simulations are performed for different values of m_a ranging from 0.5 to 1 and the corresponding %THD are measured using the FFT block and their values are shown in Table II. Figs.5 – 10 show the simulated output voltage of DCMLI and their harmonic spectrum with above strategies but for only one sample value of $m_a = 0.8$.

Figure 5 displays the five level output voltage generated by COPWM-A switching strategy and its FFT plot is shown in Figure 6. Figure 7 shows the five level output voltage generated by COPWM-B switching strategy and its FFT plot is shown in Figure 8. Figure 9 shows the five level output voltage generated by COPWM-C switching strategy and its FFT plot is shown in Figure 10. Figure 11 shows a graphical comparison of %THD in various strategies for different modulation indices. Tables III and IV show the Distortion Factor (DF) and Crest Factor (CF) of the output voltage of chosen MLI. The following parameter values are used for simulation: V_{DC} =200V, R(load) = 100 ohms, f_c=1050Hz, and f_m=50Hz.





Figure 6. FFT plot of COPWM-A strategy

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Figure 7. Output voltage generated by COPWM-B strategy





Figure 10. FFT plot of COPWM-C strategy



Figure 11. % THD vs modulation index (m_a)

Table 2. % THD for different modulation indices (by simulation)				
m _a	COPWM-A	COPWM-B	COPWM-C	
1	12.91	19.14	14.23	
0.9	10.39	21.66	16.08	
0.8	7.84	24.93	18.28	
0.7	5.68	28.55	20.35	
0.6	4.18	33.79	20.36	
0.5	3.75	42.61	18.8	

Table 2. %THD for different modulation indices (by simulation)

m _a	COPWM-A	COPWM-B	COPWM-C
1	0.84	0.84	0.8
0.9	0.74	0.74	0.7
0.8	0.55	0.56	0.5
0.7	0.3	0.3	0.3
0.6	0.04	0.09	0.09
0.5	0.03	0.11	0.1

Table 3. % DF for different modulation indices (by simulation)

Table 4. CF for different modulation indices (by simulation)

m _a	COPWM-A	COPWM-B	COPWM-C
1	1.31	1.29	1.31
0.9	1.41	1.38	1.39
0.8	1.52	1.48	1.5
0.7	1.67	1.61	1.64
0.6	1.88	1.79	1.86
0.5	2.26	2.08	2.25

It is observed (from Table II & Figure11) the harmonic output voltage is least with COPWM-A strategy. The %DF is relatively equal for all the three strategies. CF is least with COPWM-B strategy. The following are observed from the FFT plots (Figure 6, Figure8 and Figure10) : (i) 3rd order harmonic is dominant in all the three strategies, (ii) among the three overlapping strategies COPWM-A provides minimum harmonic contents, (iii) dominant lower sideband harmonic (20th order) is present in COPWM-B and COPWM-C strategies. (iv) COPWM-A strategy has the harmonic amplitude below 6%. (v) All the three strategies provide high DC bus utilisation. (vi) harmonic energy above 3% is present in 3rd and 19th orders in COPWM-A strategy, 3rd, 18th and 20th orders in COPWM-B strategy and 3rd, 14th, 16th, 18th and 20th orders in COPWM-A has less number of dominant harmonics.

5. Experimental Results

This section presents the results of experimental work carried out on chosen DCMLI using dSPACE DS1104 controller board which is based on the Texas Instruments TMS320F240 floating-point DSP. Real time implementation of these strategies using dSPACE/RTI requires less time for development as it can be expanded from the simulation blocks developed using MATLAB- SIMULINK.

The dSPACE system is an embedded or self contained system. The dSPACE system combines a data acquisition system with an independent processing system to implement digital control. It is specifically designed for the development of high-speed multivariable digital controllers. It is a real time control system based on a 603 power PC floating-point processor with four multiplexed inputs to 16-bit Analog to Digital Converter (ADC), four inputs with independent 12-bit ADCs and an 8 - output digital to analog converter running at 250 MHz. For advanced I/O purposes, the board includes a slave-DSP subsystem based on the

TMS320F240 DSP. The dSPACE system can be plugged into a PCI slot of a PC. The gate signal generation block using different PWM strategies listed above is designed and developed using SIMULINK and downloaded to dSPACE / RTI. The results of the experimental study are shown in the form of the PWM outputs of chosen DCMLI. Optocoupler circuit provides isolation between the control circuit and the power converter circuit. The optocoupler used is 6N137, which is an optically coupled gate that combines a GaAsP light emitting diode and an integrated high gain photo detector. An enable input allows the detector to be strobed. The output of the detector IC is inversion of the applied input. The PWM signals from the dSPACE are not capable of driving the MOSFETs. In order to strengthen the pulses a driver circuit is provided.

The results of the experimental study are shown in the form of the oscillograms of PWM outputs and harmonic spectrum of chosen MLI. Figs.12-14 show the experimental output voltage and corresponding harmonic spectra of chosen DCMLI obtained using dSPACE/RTI with COPWM-A, COPWM-B and COPWM-C strategies respectively. After suitably scaling down the simulation values, in view of laboratory constraints, the peak-to-peak output voltage obtained experimentally is 20V.

Table V and Figure15 show the comparison of %THD of output voltage with different carrier overlapping strategies for various values of modulation index. Figure 16 shows the entire hardware setup. Tables VI and VII show the % DF and CF of the output voltage of chosen MLI.



Figure 12. Output voltage of DCMLI using COPWM-A strategy



Figure 13. Output voltage of DCMLI using COPWM-B strategy



Figure 14. Output voltage of DCMLI using COPWM-C strategy



Figure 15. Hardware setup



Figure 16. % THD vs modulation index (by experiment)

m _a	COPWM-A	COPWM-B	COPWM-C
1	12.5	13.5	15.9
0.9	10.8	14.9	17.4
0.8	9.4	18.3	18.1
0.7	6.2	22.6	20.9
0.6	5.7	25.8	16.2
0.5	5.0	28.7	20.3

Table 5. % THD for different modulation indices (by experiment)

Table 6. %DF for different modulation indices (by experiment)

ma	COPWM-A	COPWM-B	COPWM-C
1	0.60	0.98	0.66
0.9	0.60	0.69	0.38
0.8	0.39	0.75	0.09
0.7	0.04	0.06	0.06
0.6	0.10	0.07	0.20
0.5	0.02	0.08	0.07

Table 7. CF for different modulation indices (by experiment)

m _a	COPWM-A	COPWM-B	COPWM-C
1	1.4	1.4	1.4
0.9	1.5	1.5	1.5
0.8	1.6	1.6	1.6
0.7	1.7	1.7	1.7
0.6	1.9	1.8	1.9
0.5	2.2	2.2	2.2

6. Conclusion

In this paper, CFD based PWM strategies for chosen DCMLI have been presented. Various performance factors like % THD, % DF and CF which is a measure of the stress on the device have been evaluated, presented and analysed. It is observed that the COPWM-A strategy provides lower %THD and less number of dominant harmonics than the other strategies. The simulation and experimental results closely match with each other validating the strategies presented. The results presented also closely agree with those in literature [9,16].

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