Phase Noise and Jitter in CMOS Ring Oscillators

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***Abstract*—A simple, physically based analysis illustrate the noise processes in CMOS inverter-based and differential ring oscillators. A time-domain jitter calculation method is used to analyze the effects of white noise, while random VCO modulation most straightforwardly accounts for flicker ($1/f$) noise. Analysis shows that in differential ring oscillators, white noise in the differential pairs dominates the jitter and phase noise, whereas the phase noise due to flicker noise arises mainly from the tail current control circuit. This is validated by simulation and measurement. Straightforward expressions for period jitter and phase noise enable manual design of a ring oscillator to specifications, and guide the choice between ring and *LC* oscillator.**

I. Introduction

THE ring oscillator is the most widely manufactured integrated circuit of all. Foundries use ring oscillators on every semiconductor wafer to monitor the gate delay and speed-power product of fabricated MOS inverters. Automated measurements of oscillation frequency determine which wafers are acceptable, and which fall outside an acceptable window and must be discarded. Ring oscillators have occupied this role since the earliest days of MOS IC technology because they are easy to build, always oscillate, and are readily measured. The ring oscillator is a closed loop comprising an odd number of identical inverters, which forms an unstable negative feedback circuit. Its period of oscillation is twice the sum of the gate delays in the ring.

Because these oscillators are so well-known to digital and analog circuit designers alike, they have found use beyond the monitoring of the semiconductor process in communications circuits and clock generation. A voltage-controlled ring CMOS inverter-based oscillator was first used for clock recovery in an Ethernet controller [1]. Since then, the ring oscillator has become a widely used component in the communications IC toolbox. On today's mixed-signal ICs, almost all ring oscillators use differential delay stages [2], [3] because of their greater immunity to supply disturbances. In this role, the ring oscillator is still the most widely fabricated of *all* oscillators.

Why is this? First, compared to alternatives such as the *LC* resonator-based oscillator, the ring oscillator is exceptionally compact. A large number of ring oscillators take up the same chip area as a small spiral inductor. Second, it can oscillate at very high frequencies, that is, at very short periods limited only by the sum of a few gate delays. The maximum oscillation frequency is always much higher than relaxation or *RC* phase shift oscillators—although not as fast as *LC* oscillators that can tune a transistor to oscillate at its $f_{\max}$. Third, as the ring oscillator is tuned in frequency by a current, its tuning range can span orders of magnitude. Only the relaxation oscillator, which is also tuned by a current, offers a similar tuning range.

In spite of its widespread use in communication circuits and on microprocessors, the ring oscillator is designed empirically. Based on delay data given by the foundry, the right number of stages is chosen to oscillate at the desired frequency. This is refined by simulation. Today the time jitter or phase noise in the oscillation can also be simulated. Before the advent of phase noise simulation, there was little recourse but to build the circuit and find out. This has not escaped researchers. There has been a stream of publications since the early 1980s on analytical estimation of delay in chains of CMOS inverters, and since the mid–1990s on estimation of jitter in ring oscillators. However, the analysis for gate delay becomes increasingly nonintuitive as it gets more accurate, and the latest editions of textbooks on VLSI design [4], [5] hold that it is better to use the simplest possible analysis for a first-order estimate of gate delay and then refine it with simulation. Similarly, the available analyses for jitter offer "upper limits" or estimates within orders of magnitude, but no crisp, simple expression that is validated by measurements and that gives enough design insight to enable a ring oscillator to be designed first time right without guesswork and lengthy simulations.

Section II briefly reviews the prior literature on this subject.

II. Summary of Literature

A. CMOS Gate Delay

An accurate estimate of the delay through a CMOS inverter loaded by the capacitance of a similar inverter is important not only for our purposes here, but is at the very center of the enterprise of VLSI design. The delay through a gate with fanout of one sets the absolute upper limit on clock frequency for a logic block. *Propagation delay* (t_d) is defined as the time between when the input crosses the switching threshold [4] or toggle point (V_M) of the inverter to when its output crosses the toggle point of the next inverter in a chain (Fig. 1). The first publications on the subject estimated delay by the time for the output voltage of an nMOS or CMOS inverter driving the capacitance of the next stage to cross the trip point in response to an input step [Fig. 2(a)]. However, the input waveforms in a practical logic chain are not ideal steps but have a finite slope, which in the case of a chain of identical stages is the same at every other stage [6], and in the case of balanced CMOS inverters with equal pullup and pulldown is the same at the input and output of each inverter with opposite sign. This led to a refinement of the calculation based on step response delay to one which takes into account the finite slope of the input ramp [7] [Fig. 2(b)]. In general, for large fanouts this calculates a longer propagation delay

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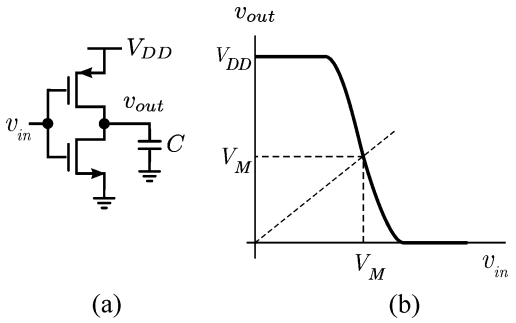

Fig. 1. (a) CMOS inverter driving a capacitor load, as in a ring oscillator. (b) Static input-output characteristic.

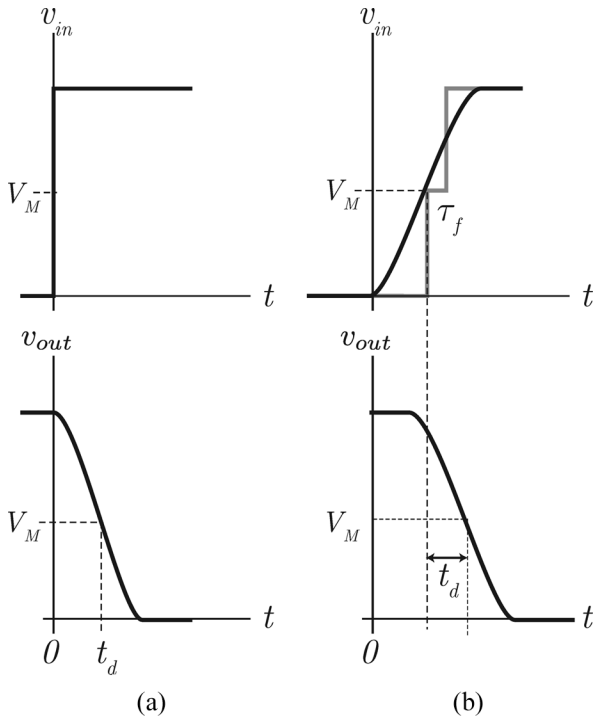

Fig. 2. (a) Propagation delay defined in response to a step voltage input. (b) Realistic ramp input, which can be approximated by a two-step input for any fanout.

than an input step. Yet better estimates of propagation delay continue to be published; for example, [8] gives a surprisingly complicated but complete analytical expression for delay, given that the circuit in question contains only an NFET, a PFET, and a capacitor. The complexity of these analyses forces designers to continue to use simple estimates based on *RC* delay for hand calculation, which are refined on timing simulators [4], [5].

When the fanout is one as in a ring oscillator, simple but reasonably accurate models of dynamics can suffice. In [9] it is shown that delay can be estimated within 10% by approximating a ramp with a delayed two-level step input [Fig. 1(b)]. The delay in the first step is the time it takes the ramp to reach the inverter toggle point, and the delay in the second step depends on the load capacitance and the ramp rate at the input. Ring oscillators are subject to what they call moderate inputs [9, p. 1181], where the input and output ramp rates in each CMOS inverter delay stage are comparable. This delay between the first and second steps, τ_f, is roughly half the remaining time for the input ramp to reach its final value. If we let $\tau_f \to 0$, then we are back to estimating the delay with a step input [Fig. 2(b)]. The input step is correctly located in time, because t_d is measured from the time that the input crosses the toggle point. We will use this simplification in subsequent analysis.

B. Jitter in Ring Oscillators

The first paper to estimate jitter caused by FET noise in CMOS differential ring oscillators [10] cast the problem correctly in the time domain, by finding fluctuations in the instants when the output ramp in a delay element crosses the toggle point. This is similar to the analysis used to find jitter in relaxation oscillators [11]. However, it concluded that jitter and phase noise depend on the voltage gain of the delay circuit. Intuition tells us that voltage gain of the delay element should not matter as long as it is large; indeed, it can be infinite, because delay, and therefore jitter, depends mainly on charge/discharge current and capacitance. It also gave the correct expression (without proof in the paper) that links period jitter, which we will define below, with phase noise; subsequent analyses, including our own, show that this relationship holds for white noise sources. The paper does not address $1/f$, or flicker, noise.

The second paper to analyze jitter focused on ring oscillators using ECL-like BJT delay stages [12]. The analysis as well as the results were in the time-domain, again defining jitter by fluctuations in instants of threshold crossings at each delay stage in a closed chain. There was no attempt to link jitter to phase noise. This paper's expressions for jitter are consistent with ours.

Both papers take into account the time-varying nature of the circuit by first analyzing the steady-state RMS noise at equilibrium, with the load *RC* setting the noise bandwidth; and then modeling exponential decay or build up with this time constant to capture the time-varying aspect of the large-signal switching.

The next publication in the series [13] applies the concept of the impulse sensitivity function to the waveforms of a ring oscillator, and from the relation between the impulse sensitivity function and phase noise, deduces an approximate expression for phase noise. Although the results look similar to ours, they are quantitatively different. An abstract formulation also runs the risk that it might lead to incorrect physical interpretations.

The latest analysis of ring oscillator phase noise [14] explores details of the noise processes at the toggle point of the delay element, but at the end offers no analytical expressions, simple or otherwise, for the phase noise or jitter.

With this as background, this paper presents a comprehensive analysis of jitter and phase noise in both CMOS inverter-based and differential ring oscillators, pinpointing the most important mechanisms whereby white and flicker noise manifest themselves. The physically based approach and simple resulting expressions should make it easy to design ring oscillators for a given jitter. In fact, these simple expressions predict jitter and phase noise much more accurately than oscillation frequency; this is similar to what is seen in amplifier design, where input-referred noise is predicted much more accurately than gain.

III. Analytical Tools

This section covers the analytical methods and results which are used in several places in the body of the paper. It will aid

understanding of the physical processes if these methods are dealt with as a prelude.

A. Windowed Integrals of Noise

1) Lossless Integral: The definite integral of white noise over a time window is of interest. Suppose i_n is a noise current that integrates on a capacitor C over an interval t_d. The resulting voltage v_n is given by

$$v_n = \frac{1}{C}\int_0^{t_d} i_n dt. \tag{1}$$

We would like to know the spectral density and RMS value of the samples of integrated voltage $\{v_n\}$ if this process is repeated many times. The most intuitive way to find this is to convert the definite integral into a convolution, by multiplying i_n by a rectangular unit window $w_{t_d}(t)$ of width t_d and integrating

$$v_n(t) = \frac{1}{C}\int_0^{\infty} i_n(x) \times w_{t_d}(t-x)dx. \tag{2}$$

In the frequency domain, this can be thought of as passing the input noise through a linear block whose transfer function is the Laplace transform $W_{t_d}(s)$ of the rectangular window $w_{t_d}(t)$ [15]. In terms of power spectral density (PSD)

$$S_{v_n}(f) = \frac{1}{C^2}\left|W_{t_d}(f)\right|^2 \times S_{i_n}(f). \tag{3}$$

The Laplace transform of a rectangular window is well known:

$$W_{t_d}(s) = \frac{1-e^{-st_d}}{s} = \frac{\sin(\omega t_d/2)}{\omega t_d/2}e^{-j\omega t_d/2}. \tag{4}$$

Its frequency response in magnitude is

$$\left|W_{t_d}(f)\right| = t_d \times \mathrm{sinc}(ft_d) \equiv t_d\frac{\sin(\pi f t_d)}{\pi f t_d}. \tag{5}$$

This is a low-pass filter with a -3 dB cutoff frequency of roughly $f \sim 1/2t_d$ and a series of nulls in its transfer function at $f = 1/t_d, 2/t_d, \ldots$ It passes the low frequencies in the noise spectrum, but attenuates the high frequencies. With white Gaussian noise at the input, the output spectrum is no longer white although its distribution remains Gaussian. Fig. 3 illustrates the integration of several trials of white noise waveforms with $\sigma = 1$. It can be seen that as the integration period t_d increases, the rate of change of the dominant noise wander slows down, indicating that progressively lower frequencies are being accentuated, while the standard deviation widens, indicating a diffusion process [15].

Given the spectral density of the integrated voltage noise, the mean-square value at the end of the integration window is found using the Wiener–Khinchine theorem [15]:

$$\left\langle v_n^2\right\rangle = \int_0^{\infty} S_{v_n}(f)df = \frac{1}{C^2}\int_0^{\infty} S_{i_n}(f)\left|W_{t_d}(f)\right|^2 df. \tag{6}$$

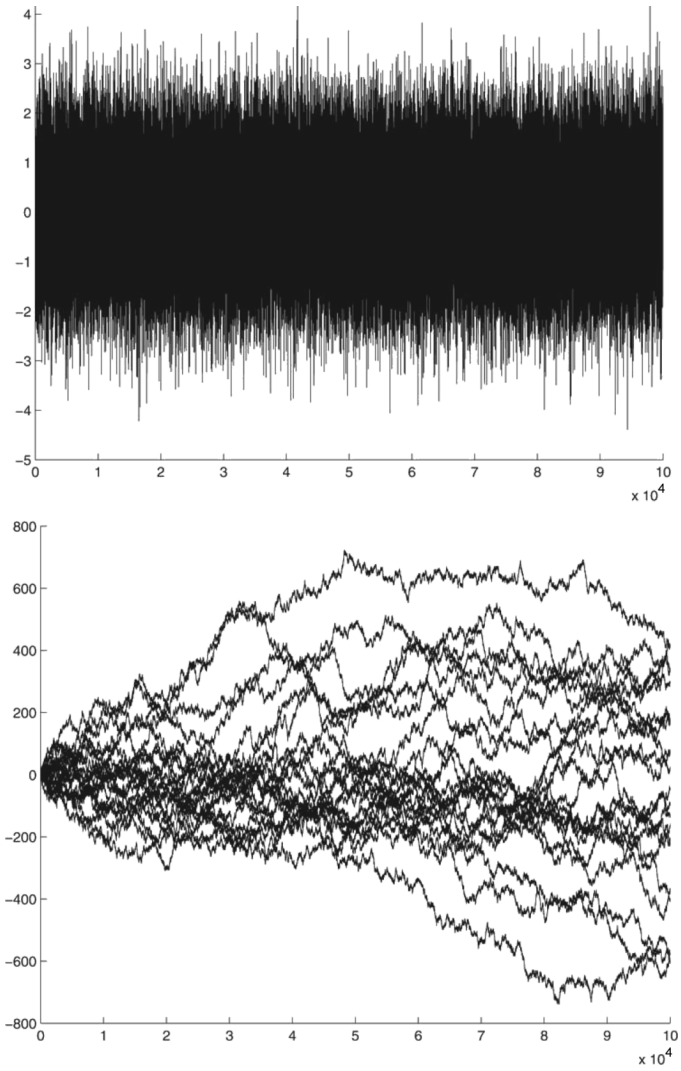

Fig. 3. White noise of unit standard deviation, and its integration over an increasingly wide window with multiple trials.

Now if $S_{i_n}(f)$ is constant because it is white, it can be pulled out and the remaining integral is evaluated as follows:

$$\begin{aligned}\int_0^{\infty}\left|W_{t_d}(f)\right|^2 df &= t_d^2\int_0^{\infty}\frac{\sin^2(\pi f t_d)}{(\pi f t_d)^2}df \\ &= \frac{t_d}{\pi}\int_0^{\infty}\frac{\sin^2 x}{x^2}dx = \frac{t_d}{\pi}\frac{\pi}{2} = \frac{t_d}{2}.\end{aligned} \tag{7}$$

Therefore, from (5), (6), and (7),

$$\left\langle v_n^2\right\rangle = \frac{S_{i_n}}{2C^2}t_d \propto t_d. \tag{8}$$

This expression clearly shows that integrated white noise resembles a random walk with steps of t_d, and as expected, the longer the walk, the wider the spread.

2) Lossy Integral: Lossy integration refers to the process when a noise current i_n integrates onto a capacitor C which is shunted by a finite loss resistance R. We denote by θ the window of integration normalized to the time constant, that is,

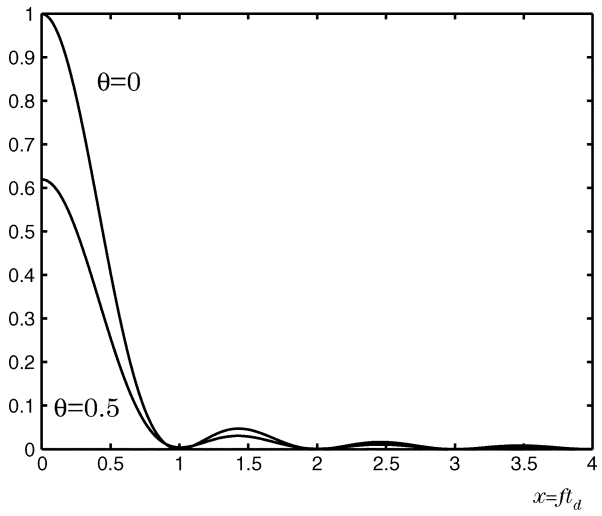

Fig. 4. Plots of the square of transfer functions of lossless ($\theta = 0$) and lossy ($\theta = 0.5$) windowed integrators, on normalized horizontal axis.

$\theta = t_d/RC$. It can be shown that the transfer function associated with the windowed integration $\tilde{W}_{t_d}$ is

$$\tilde{W}_{t_d}(s) = t_d \frac{1 - e^{-(st_d+\theta)}}{st_d + \theta} \tag{9}$$

and

$$\int_0^\infty \left|\tilde{W}_{t_d}(f)\right|^2 df = \frac{t_d}{2}\frac{1-e^{-2\theta}}{2\theta} = \frac{1-e^{-2\theta}}{2\theta}\int_0^\infty |W_{t_d}(f)|^2\, df. \tag{10}$$

The functions $|W_{t_d}(f)|^2$ and $|\tilde{W}_{t_d}(f)|^2$ for $\theta = 0.5$ are plotted in Fig. 4.

B. Relation Between Jitter and Phase Noise

The search for a link between jitter and phase noise is motivated by the problem that baseband communication systems specify clock purity in the time domain, either as the jitter in a single period of the clock, that is, *period jitter*, or by *accumulated jitter* over N cycles of the clock [16]–[20], but oscillators are specified by *phase noise*. The two are fundamentally different, and the relationship is not obvious.

Phase noise is a continuous stochastic process indicating random accelerations and decelerations in phase (ϕ) as an oscillator orbits at a nominally constant frequency (f_0) in steady-state (Fig. 5). Jitter arises from sampling the orbit at certain points. For example, for a noisy oscillatory waveform that is nominally free of DC the period (τ) may be defined as the interval between successive zero crossings of the waveform with, say, positive slope. In the presence of phase noise, $\{\tau\}$ is a set of *discrete* random variables. *Period jitter* is defined as the standard deviation σ_τ of this discrete sequence around its mean value [15]. By contrast, the underlying phase noise is a continuous random variable that is specified by its PSD $S_\phi(f)$. So what is the link between the two?

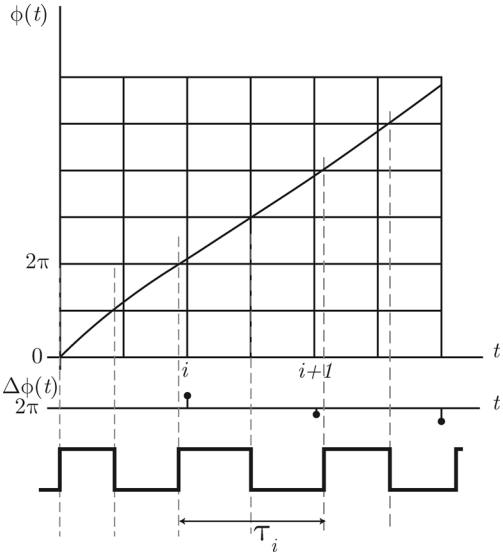

Fig. 5. Connection between phase of an oscillation, phase noise, and period jitter.

Appendix 1 in [13] derives a general link which does not assume a particular spectral density of phase noise. The same analysis has since appeared in other publications [16], [21], [22]. Expressed most simply, the derivation goes as follows:

$$\tau_i = \frac{1}{2\pi f_0}\left(\phi(t_{i+1}) - \phi(t_i)\right) = \frac{1}{2\pi f_0}\Delta\phi_i. \tag{11}$$

As ϕ is a continuously evolving variable, $\Delta\phi$ is found by the first-difference operation, that is, by subtracting it after a delay equal to the nominal period $1/f_0$. Thus, the spectral density $S_{\Delta\phi}(f)$ is given by

$$S_{\Delta\phi}(f) = S_\phi(f)\left|1 - e^{-j2\pi f/f_0}\right|^2 = 4S_\phi(f)\sin^2(\pi f/f_0). \tag{12}$$

From this and (11) follows the **spectral density of jitter**:

$$S_\tau(f) = S_\phi(f)\frac{\sin^2(\pi f/f_0)}{(\pi f_0)^2}. \tag{13}$$

This is the spectrum of the quantity τ sampled at f_0, and is therefore defined only over the frequency range (0, $f_0/2$). In practice, more important than the spectral density of jitter is its mean-square value σ_τ^2, as would be measured on a time-domain instrument such as a digital oscilloscope [12], [20]. Once again, we use the Wiener–Khinchine theorem to calculate this from the spectral density:

$$\sigma_\tau^2 = \int_0^\infty S_\tau(f)df = \int_0^\infty S_\phi(f)\frac{\sin^2(\pi f/f_0)}{(\pi f_0)^2}df. \tag{14}$$

This then is the general form of the **link between jitter and phase noise**, two directly measurable quantities.

Let us see how the link simplifies under the special case when all phase noise arises from white noise sources. Ref. [23]—and the earlier, but to our readers the less accessible, [24]—shows that in an oscillator with white noise sources alone, the SSB

phase noise PSD $\mathcal{L}(f)$ at moderate frequency offsets f is given by

$$\mathcal{L}(f) = \frac{S_\phi(f)}{2} = \frac{S_w}{f^2} \tag{15}$$

where S_w is a coefficient specific to an oscillator and its noise sources. In this case, the expression in (14) can be evaluated exactly:

$$\sigma_\tau^2 = \frac{2}{\pi f_0^3} S_w \int_0^\infty \frac{\sin^2 x}{x^2} dx = \frac{S_w}{f_0^3}. \tag{16}$$

Thus

$$\mathcal{L}(f) = \sigma_\tau^2 \frac{f_0^3}{f^2}. \tag{17}$$

Using heuristic reasoning, others [10], [25], [26] also have found this relationship for white noise.

We will now apply these analytical tools to commonly used ring oscillators. As these circuits are most naturally analyzed in the time domain, we will first analyze the jitter, and then deduce the phase noise. The predictions of phase noise will be validated against measurements.

IV. Inverter-Based Ring Oscillator

A. Inverter Jitter Due to White Noise

Based on the summary in Section II-A, we model a CMOS inverter in a ring oscillator as producing a voltage ramp at its output in response to a correctly positioned step input. Consider a positive input step (Fig. 6). The input shuts off the PFET and biases the NFET in the saturation region. The NFET pulls down the voltage on C from $V_{\rm DD}$ to 0. We define the propagation delay t_d as the time from the input step to when the output ramp crosses the next (identical) inverter's toggle point, which we will suppose is located at $(1/2)V_{\rm DD}$. We note that an inverter with symmetrical toggle point results in unequal rise and fall times, but the analysis takes this into account.

The NFET enters triode region when $v_{\rm out}$ crosses $(V_{\rm DD} - V_{tN})$. If $(V_{\rm DD} - V_{tN}) > (1/2)V_{\rm DD}$, the NFET will enter triode region during the propagation delay, otherwise not. While in saturation the discharge current is

$$I_N = I_{DNsat} = (1/2)\mu C'_{ox}(W/L)(V_{\rm DD} - V_{tN})^2 \tag{18}$$

and this current will fall gradually in the triode region. For simplicity we assume that even if the NFET enters triode during t_{dN}, its drain current will not change appreciably. Thus, the output voltage crosses the toggle point with a slope

$$dv_{\rm out}/dt = I_{DNsat}/C. \tag{19}$$

This current is accompanied by noise i_n from the NFET (Fig. 6). The spectral density of the noise is [27]

$$S_{i_nN} = 4{\rm kT}\gamma_N g_{DS0} = 4{\rm kT}\gamma_N g_m = 8{\rm kT}\gamma_N \frac{I_{DNsat}}{V_{\rm DD} - V_{tN}}.$$

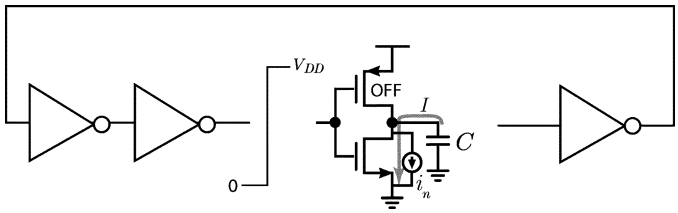

Fig. 6. Inverter switching in ring oscillator, showing signal and noise currents.

(20)

The capacitor C integrates noise into voltage over the window t_{dN}. This voltage wavers randomly at a rate that is inversely proportional to t_{dN}, advancing or delaying the instant of threshold crossing. It is unlikely that on a macroscopic time scale this noisy ramp will cross the threshold more than once (Fig. 7) (whereas [14] discusses multiple crossings). The dynamics of the threshold crossing are described by

$$\int_0^{t_{dN}} \frac{I_N + i_{nN}}{C} dt = \frac{V_{\rm DD}}{2} \tag{21}$$

where t_{dN} is a random variable that arises from noise current. The statistics of t_{dN} follow:

$$t_{dN} \equiv \langle t_{dN} \rangle = \frac{CV_{\rm DD}}{2I_N} \tag{22}$$

and

$$\sigma_{t_{dN}}^2 = \frac{1}{I_N^2} \left\langle \left(\int_0^{t_{dN}} i_{nN} dt \right)^2 \right\rangle. \tag{23}$$

Section III-A examines this very situation. As shown there, it is most straightforward to first calculate the spectral density of t_{dN}, that is,

$$S_{t_{dN}} = \frac{t_{dN}^2}{I_n^2} {\rm sinc}^2(f t_{dN}) S_{i_nN} \tag{24}$$

and then use the Wiener–Khinchine theorem to find the mean-square value

$$\sigma_{t_{dN}}^2 = \int_0^\infty S_{t_{dN}} df = \frac{t_{dN}}{\pi I_N^2} S_{i_nN} \int_0^\infty \frac{\sin^2 x}{x^2} dx \tag{25}$$

Using (20) this simplifies to

$$\sigma_{t_{dN}}^2 = \frac{4{\rm kT}\gamma_N t_{dN}}{I_N(V_{\rm DD} - V_{tN})}. \tag{26}$$

This is a compact expression for **uncertainty in propagation delay** caused by current noise integrating on the capacitor C. The expression could be refined to take into account integrator leak caused by nonzero g_{ds} when the pulldown FET enters

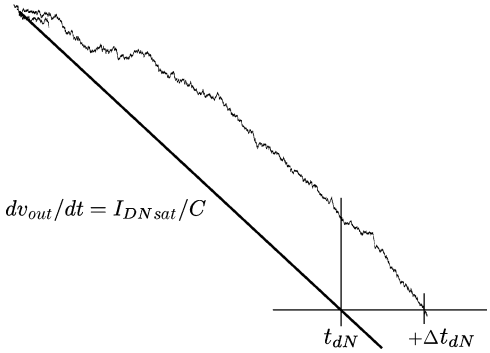

Fig. 7. Illustrating zero crossing of a ramp with integrated noise.

triode, but even in the worst case when $V_{tN} \ll V_{\rm DD}/2$, neglecting the leak causes only a 2 dB error.

Prior to the switching event the channel resistance of the PFET pullup deposits an initial noise on the capacitor. The mean square noise and the associated jitter are

$$\langle v_n^2 \rangle = {\rm kT}/C \tag{27}$$

$$\sigma_{t_{dN}}^2 = \frac{\langle v_n^2 \rangle}{(I_N/C)^2} = \frac{{\rm kT}C}{I_N^2}. \tag{28}$$

Thus, the total jitter due to these two uncorrelated white noise sources is

$$\sigma_{t_{dN}}^2 = \frac{4{\rm kT}\gamma_N t_{dN}}{I_N(V_{\rm DD} - V_{tN})} + \frac{{\rm kT}C}{I_N^2}. \tag{29}$$

B. Ring Oscillator Jitter and Phase Noise Due to White Noise

The *period of oscillation* τ of a ring oscillator is defined by the time it takes for a transition to propagate *twice* around the ring. In a ring oscillator comprising M inverter delay stages, this involves M pulldowns by NFETs and M pullups by PFETs. Thus, the nominal frequency of oscillation f_0 is

$$f_0 = \frac{1}{M(t_{dN} + t_{dP})} \simeq \frac{2}{MCV_{\rm DD}} \left(\frac{1}{I_N} + \frac{1}{I_P} \right)^{-1} \simeq \frac{I/C}{MV_{\rm DD}}. \tag{30}$$

In light of the discussion in Section II-A, we should state the approximations that underlie this expression. The first approximation is in the expression for propagation delay. Second, we assume that the pullup and pulldown currents are equal, whereas when the toggle point is symmetric at $(1/2)V_{\rm DD}$, they are actually different.

Every propagation delay is jittered by noise in the pullup or pulldown process. These noise events are uncorrelated and add in the mean-square. Therefore, the **variance of period jitter** is

$$\sigma_\tau^2 = M \left(\sigma_{t_{dN}}^2 + \sigma_{t_{dP}}^2 \right). \tag{31}$$

Using (29) and (30), and to simplify analysis assuming that $V_{tN} = V_{tP} = V_t$, this can be written as

$$\sigma_\tau^2 = \frac{\rm kT}{If_0} \left(\frac{2}{V_{\rm DD} - V_t}(\gamma_N + \gamma_P) + \frac{2}{V_{\rm DD}} \right). \tag{32}$$

Using (17), the **SSB phase noise due to white noise** is now found from the jitter

$$\mathcal{L}(f) = \frac{2{\rm kT}}{I} \left(\frac{1}{V_{\rm DD} - V_t}(\gamma_N + \gamma_P) + \frac{1}{V_{\rm DD}} \right) \left(\frac{f_0}{f} \right)^2. \tag{33}$$

Inverters toggle in sequence, alternating in pullup and pulldown. The pullup current I charges an inverter's load C to $V_{\rm DD}$, then the next inverter discharges its pre-charged C to ground. Thus, the average current that flows from the supply to ground in the circuit is I. In the terminology of power amplifiers, this amounts to Class B push-pull operation [27].

We draw the following conclusions from this compact expression for phase noise.

1) The phase noise is independent of the number of delay stages, and only depends on the frequency of oscillation f_0. Thus, the phase noise is equal in two rings which oscillate at the same frequency, where one ring comprises a few stages loaded heavily while the other ring comprises more lightly loaded stages.
2) The only technology-dependent parameters are V_t and γ.

The main design guideline is that to lower phase noise, we should use as high a supply voltage as possible, and burn as much current as the budget allows. The desired oscillation frequency determines the number of stages.

C. Phase Noise Due to VCO Control Noise

Noise on the frequency tuning voltage or current is an inescapable source of phase noise in every oscillator. If, say, in a current-starved inverter chain the control voltage V_C imposes a sensitivity κ_V on the nominal frequency f_0, then using the narrowband FM expression [28, p. 1036, (18)] it is straightforward to deduce the resulting phase noise

$$\frac{\partial f_0}{\partial V_C} = \kappa_V \;\Rightarrow\; S_{f_0}(f) = \kappa_V^2 S_{V_C}(f) \;\Rightarrow\; \mathcal{L}(f) = \frac{\kappa_V^2}{4f^2} S_{V_C}(f). \tag{34}$$

The supply voltage $V_{\rm DD}$ often exerts a strong control on inverter delay. On mixed-signal ICs, the switching of nearby circuits to an oscillator causes perturbations and glitches on an imperfectly filtered supply that far exceed all thermodynamic noise. This modulates the delay in all the inverters connected to the perturbed supply. The delay modulation is *correlated* between the inverters. Even if the supply to the oscillator is well-regulated and filtered, flicker noise will likely be present at the regulator output. Its effect can be estimated by finding the κ_V and applying (34).

In the expression for ring oscillator frequency (30) I depends on $V_{\rm DD}$, and this dependence can be made explicit assuming that C is only due to the gate capacitance:

$$f_0 = \frac{\mu}{2L^2M}\frac{(V_{\rm DD}-V_t)^2}{V_{\rm DD}} \tag{35}$$

so that

$$\kappa_{V_{\rm DD}} = \frac{\partial f_0}{\partial V_{\rm DD}} = \frac{\mu}{2L^2M}\left(1-\frac{V_t^2}{V_{\rm DD}^2}\right) \simeq \frac{\mu}{2L^2M} \tag{36}$$

Clearly, aside from using FETs with as long a channel length as is possible, not much else will desensitize the inverter-based voltage-controlled oscillator (VCO) against supply noise. At high frequencies, FET capacitances will further raise the supply sensitivity. This is the CMOS inverter's main weakness: that although with enough noise margin [5] it is a reliable *logic* element on mixed-signal ICs, it cannot usually be a precise *delay*.

D. Ring Oscillator Phase Noise Due to Flicker Noise

Flicker $(1/f)$ noise is qualitatively different, and invokes different mechanisms of jitter and phase noise, so it should be analyzed from first principles. Pullup and pulldown currents contain flicker noise which may not fluctuate over a single transition, but varies slowly over many transitions. The noise arising in every FET is, of course, uncorrelated.

Suppose I_{Nk} and I_{Pk} are the pulldown and pullup currents supplied, respectively, by the NFET and PFET in the kth stage of an M-stage ring oscillator. Then the period of oscillation τ and frequency f_0 are

$$\tau = \frac{CV_{\rm DD}}{2}\left(\frac{1}{I_{N1}}+\frac{1}{I_{P2}}+\ldots+\frac{1}{I_{PM}} +\frac{1}{I_{P1}}+\frac{1}{I_{N2}}+\ldots+\frac{1}{I_{NM}}\right) \tag{37}$$

$$f_0 = \frac{2}{CV_{\rm DD}}\left(\sum_{j=1}^{M}\frac{1}{I_{Nj}}+\frac{1}{I_{Pj}}\right)^{-1} \tag{38}$$

In a symmetrically designed inverter where the pullup and pulldown currents are equal to I, the expression for frequency is identical to (30).

The sensitivity of f_0 to, say, the pulldown current in the kth inverter is

$$\frac{\partial f_0}{\partial I_{Nk}} = \frac{2}{CV_{\rm DD}}\left(\sum_{j=1}^{M}\frac{1}{I_{Nj}}+\frac{1}{I_{Pj}}\right)^{-2}\frac{1}{I_{Nk}^2} = \frac{CV_{\rm DD}f_0^2}{2I_{Nk}^2} = \frac{f_0}{2MI}. \tag{39}$$

This is a VCO gain, as discussed in the section above. Thus, using (34), the SSB phase noise resulting from flicker noise of spectral density $S_{i_{Nk}}^{1/f}$ in the kth pulldown current is

$$\mathcal{L}(f) = \frac{1}{4f^2}\left(\frac{f_0}{2MI}\right)^2 S_{i_{Nk}}^{1/f}(f) \tag{40}$$

and due to the uncorrelated contributions of the M NFETs and PFETs in the oscillator it is

$$\mathcal{L}(f) = \frac{1}{4f^2}\left(\frac{f_0}{2MI}\right)^2 \times M\left(S_{i_{Nk}}^{1/f}+S_{i_{Pk}}^{1/f}\right) = \frac{1}{16MI^2}\left(S_{i_N}^{1/f}+S_{i_P}^{1/f}\right)\left(\frac{f_0}{f}\right)^2. \tag{41}$$

To gain design insight from this expression, we must specify the spectral density of flicker noise in terms of FET geometry and bias. For many years, we have used a measurement-based model of flicker noise [29] in amplifiers, mixers, and oscillators that has proved itself to be a reliable predictor. According to this model the flicker noise PSD in nMOS *referred to the FET gate* as a voltage $v_n^{1/f}$ is given by the expression

$$S_{v_n}^{1/f} = \frac{K_{fN}}{WLC'_{ox}f} \tag{42}$$

where the empirical coefficient $K_{fN} \approx 10^{-24}$ is essentially independent of bias, fabricator and technology. The same expression holds for PMOS, but here K_{fP} is lower and depends on bias. One can estimate an upper limit on the effects of flicker noise by setting $K_{fP} = K_{fN}$. To find the noise in the drain current we use (18)

$$S_{i_n}^{1/f} = g_m^2 S_{v_n}^{1/f} = \left(\frac{2I}{V_{\rm DD}-V_t}\right)^2\frac{K_f}{WLC'_{ox}f}. \tag{43}$$

The final expression for SSB **phase noise induced by flicker noise** is

$$\mathcal{L}(f) = \frac{1}{4M(V_{\rm DD}-V_t)^2}\left(\frac{K_{fN}}{W_NL_N}+\frac{K_{fP}}{W_PL_P}\right) \times\left(\frac{f_0^2}{f^3}\right) \tag{44}$$

$$= \frac{C'_{ox}}{8MI}\left(\frac{\mu_NK_{fN}}{L_N^2}+\frac{\mu_PK_{fP}}{L_P^2}\right)\left(\frac{f_0^2}{f^3}\right). \tag{45}$$

This last expression gives design insight. To lower flicker noise upconversion into phase noise, choose large W/L to burn as much current in the oscillator as the budget allows, and use FETs with the longest practical channel L. As the ring oscillator's average bias current does not depend on the number of stages M, use the largest number of stages. It is satisfying to see that these guidelines will also lower phase noise due to white noise (see end of Section IV-B).

E. Jitter Due to Flicker Noise

It is not easy to solve the integral in (14) analytically to establish a link between flicker-induced phase noise and jitter. However, [30] gives an approximate solution. They prove that with flicker noise the mean-square jitter grows with the *square* of elapsed time, unlike the case of white noise where, as we have also shown, it grows proportionally to elapsed time.

V. Differential Ring Oscillator

The differential delay stage's strength is that, ideally, noise on the supply appears as common-mode on both outputs, and is

rejected by the next delay stage in a chain. Of course, a small sensitivity to supply voltage remains through the voltage-dependent junction capacitances in the stage [26], which is worse at high frequencies when the load capacitance couples the delay stage output directly to the supply. In a chain of differential delay stages, the actual differential voltage waveforms are identical ramps of positive and negative slope. Here, too, we calculate the propagation delay, approximately, by the circuit's step response.

For the purpose of jitter analysis, we assume that the differential delay stage consists of a MOS differential pair, a MOS tail current source (I), and resistor loads (R) on each side. In an actual circuit, the R is realized with a single or compound MOSFET in triode region, embedded in an amplitude control loop. As the tail current tunes the delay per stage, and thereby the oscillation frequency, this control loop holds the amplitude constant; otherwise tunability will be lost. The input capacitance C of the next stage loads each output node.

A. Analysis of Delay per Stage

All analysis is on differential voltages. To keep analysis simple, the propagation delay is defined as the time t_d between an input step and the zero crossing of the output differential waveform. The differential peak output voltage swing is

$$\hat{V}_{od} = V_{op} = IR. \tag{46}$$

As the loads are *RC* circuits, the propagation delay and frequency of oscillation are determined by decaying exponentials:

$$t_d = \frac{CV_{op}\ln 2}{I} = RC\ln 2 \tag{47}$$

$$f_0 = \frac{1}{2Mt_d}. \tag{48}$$

To understand noise, we must look more closely at the switching process. A differential pair (Fig. 8) has an *input* transition range of $\hat{V}_{id} = \pm\sqrt{2}V_{effd}$ over which it steers the tail current, where V_{id} is the differential input voltage, and V_{effd} is the effective gate voltage on the differential pair at balance [27]. For the output of one delay stage to steer the current fully in the next stage, it is necessary that

$$V_{op} \gg \sqrt{2}V_{effd}. \tag{49}$$

In reality the differential input voltage ramps from, say, $-V_{op}$ to $+V_{op}$, and *vice versa*. A ramp rising from the negative extreme starts the steering action of the differential pair on crossing $-\sqrt{2}V_{effd}$. This initiates the output transition. We call the time it takes the input to rise from $-\sqrt{2}V_{effd}$ to $+\sqrt{2}V_{effd}$ the input transition time, t_T; this is different from the propagation delay t_d, which is the time between the differential zero crossings of the input and output.

B. Phase Noise due to White Noise

We analyze the jitter at the moment of zero crossing by looking at the fluctuations in voltage of the zero crossing waveform. As before, jitter is found by dividing the noise voltage by the slope of the differential switching voltage at zero crossing. In the *RC*-loaded differential pair, this slope is:

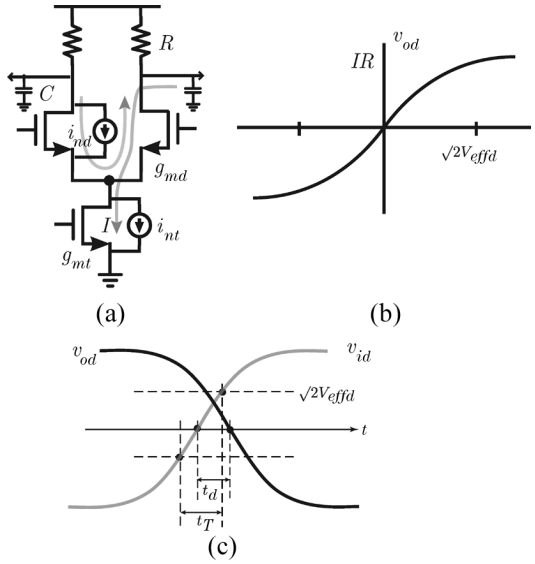

Fig. 8. (a) Differential pair delay stage, showing signal and noise currents. (b) Input–output characteristic of differential pair. (c) Illustrating transition time and propagation delay.

$$\frac{dV_{od}}{dt} = \frac{I}{C}. \tag{50}$$

Let us start by analyzing noise due to the load resistors. This noise is continuously coupled into the load capacitors, and at all times its differential mean square fluctuation is

$$\langle v_{nR}^2 \rangle = \frac{2\mathrm{kT}}{C}. \tag{51}$$

Suppose a transition steers current from left to right. Let us assume that the time between successive transitions, that is the half period of oscillation $MRC\ln 2$, is long enough that due to tail current noise i_{nt} (Fig. 8), the voltage across the *RC* load at the left output is in steady state:

$$\langle v_{nt}^2 \rangle = \int_0^\infty S_{i_{nt}} \frac{R^2}{1+(2\pi fRC)^2} df = 4kT\gamma g_{mt}R^2\left(\frac{1}{4RC}\right) = \frac{kT}{C}\gamma g_{mt}R = \frac{kT}{C}\frac{2\gamma V_{op}}{V_{efft}}. \tag{52}$$

When the current is steered to the other side, the noise voltage held on C leaks with time. After a delay t_d, the mean square value of the residue is

$$\langle v_n^2 \rangle (\text{left}) = \frac{kT}{C}\gamma g_{mt}R(e^{-t_d/RC})^2 = \frac{kT}{C}\frac{2\gamma V_{op}}{V_{efft}}e^{-2t_d/RC}. \tag{53}$$

After switching, the tail current integrates noise on the right load capacitor. This is a lossy integration. To simplify analysis, we assume that the tail current is steered to the right *all at once*.

Using the results from Section III-A-2, the mean-square voltage after period t_d is

$$\begin{aligned}\left\langle v_n^2\right\rangle(\text{right}) &= \frac{4kT}{C^2}\gamma g_{mt}\frac{1-e^{-2t_d/RC}}{(2t_d/RC)}\frac{t_d}{2}\\ &= \frac{kT}{C}\gamma g_{mt}R(1-e^{-2t_d/RC}).\end{aligned} \tag{54}$$

We can check this result by noting that as $t_d \to \infty$, this assumes the steady-state value of (52). The mean-square value of the *differential* noise voltage is *independent* of t_d:

$$\left\langle v_n^2\right\rangle(\text{left}) + \left\langle v_n^2\right\rangle(\text{right}) = \frac{kT}{C}\gamma g_{mt}R. \tag{55}$$

This is because the differential noise arises from the periodic commutation of a noise current into a differential *RC* load. Commutation of bandlimited white noise does not change its mean-square value in steady state.

During the transition time, noise from the differential pair FETs (Fig. 8) modulates the fraction of tail current being steered to the left and right branches. This describes the effect of the differential pair's current noise i_{ndiff}, which flows as a *differential current* on to the two load capacitors. To simplify analysis, we assume that *this noise integrates over* t_d, although strictly it is over some fraction of t_T, and also that over this duration the noise PSD remains the same as in the balanced condition. The magnitude of the differential current is

$$S_{i_{ndiff}} = (1/4+1/4)S_{i_{nd}} = S_{i_{nd}}/2 \tag{56}$$

where at balance $S_{i_{nd}}$ is defined as

$$S_{i_{nd}} = 4\text{kT}\gamma\frac{I}{V_{effd}}. \tag{57}$$

The differential noise current integrates on a differential load of $C/2$ in parallel with $2R$. Using the result for leaky integration (10), (57), the mean-square differential voltage after time t_d is

$$\begin{aligned}\left\langle v_{ndiff}^2\right\rangle &= \frac{1}{(C/2)^2}S_{indiff}\frac{t_d}{2}\frac{1-e^{-2t_d/RC}}{(2t_d/RC)}\\ &= \frac{3}{8C}4kT\gamma\frac{IR}{V_{effd}}.\end{aligned} \tag{58}$$

Next we sum the uncorrelated noise voltages in (58), (55), and (51) and use (50) to calculate the period jitter:

$$\begin{aligned}\sigma_\tau^2 &= 2M\sigma_{t_d}^2 = 2M\frac{\left\langle v_n^2\right\rangle}{(I/C)^2}\\ &= \frac{2\text{kT}}{If_0\ln 2}\left[\gamma\left(\frac{3}{4V_{effd}}+\frac{1}{V_{efft}}\right)+\frac{1}{V_{op}}\right].\end{aligned} \tag{59}$$

From (17) an expression follows for **SSB phase noise due to white noise** in the differential oscillator:

$$\mathcal{L}(f) = \frac{2\text{kT}}{I\ln 2}\left[\gamma\left(\frac{\frac{3}{4}}{V_{effd}}+\frac{1}{V_{efft}}\right)+\frac{1}{V_{op}}\right]\left(\frac{f_0}{f}\right)^2. \tag{60}$$

If it is believed that because of short-channel effects the FETs do not obey the square law, the phase noise expression should be recast in terms of the FET transconductance by substituting

$$g_{mt} = \frac{2I}{V_{efft}}; \quad g_{md} = \frac{I}{V_{effd}}$$

and using simulated values of these g_m's. The FET noise factor γ may also be larger for short channels.

Whereas the inverter-based delay cell operates in Class B, that is, there is no static standing current, the differential delay cell operates in Class A and consumes a steady current I per cell. Therefore, the oscillator as a whole consumes MI.

This development largely parallels an earlier analysis for BJT differential ring oscillators [12], we hope in simpler terms.

C. Phase Noise Due to Flicker Noise

Once again, flicker noise should be thought of differently than white noise, because it fluctuates at a rate much lower than the oscillation frequency. First we show that flicker noise in the differential pairs does not cause phase noise. Next we show that flicker noise in the tail currents modulates the VCO with random FM.

Let us associate flicker noise with only one differential pair in the ring oscillator, and assume all other FETs are noiseless (Fig. 9). The noise can be modeled as an input offset voltage that varies slowly. In response to a transition in the differential input, the offset either advances or retards the rising edge, and *vice-versa* the falling edge. When the input offset is constant over one period, it changes the duty cycle or mark-space ratio of the output *without* affecting the period. Duty cycle variations create second harmonic. Therefore, we conclude that flicker noise in the differential pairs upconverts to $2f_0$, but does not appear around f_0.

Flicker noise in the *tail current* modulates the delay directly. While fluctuations originating in each tail current are uncorrelated, the delay variations in all cells will add in phase due to noise on the common gate voltage driving the tail FETs (Fig. 10) and cause a large phase deviation and phase noise. The mean square jitter due to correlated noise is proportional to M^2, instead of M as, for instance, in (41). This noise originates, for example, from noise in the diode-connected FET that mirrors into the tail currents. Mirrored white noise from this FET also raises the white noise in each tail current, but because of the rapid fluctuations its effect is uncorrelated between the switching of one delay stage and the next. Flicker noise, on the other hand, slows down or speeds up *every* delay stage in a concerted manner over many cycles of oscillation, accumulating into a large variance in phase.

We analyze this by deriving an effective VCO gain. In general, the width of the diode-connected FET is $1/A$ of the width of the tail FETs in the delay stages. Further we assume that the control current is noiseless. Using the expression (48) for oscillation frequency, we find the sensitivity κ_I to tail current. Phase noise follows from (34).

$$f_0 = \frac{I}{2MCV_{op}\ln 2} \quad \Rightarrow \quad \kappa_I = \frac{f_0}{I} \tag{61}$$

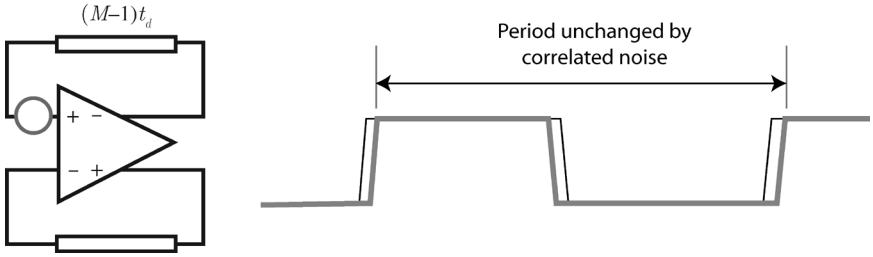

Fig. 9. Differential pair flicker noise modeled as a slowly changing input-referred voltage in a single delay stage of a ring oscillator, and the resulting effect on the oscillation waveform.

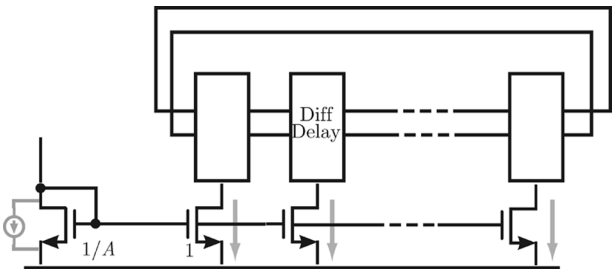

Fig. 10. Noise originating in the tail current control FET is amplified in all the tail currents $(\mathrm{A} > 1)$ and modulates the delay of all stages in the oscillator.

$$\Rightarrow \quad \mathcal{L}(f) = \frac{\kappa_I^2}{4f^2} S_I(f) = \frac{1}{4I^2} \left(\frac{f_0}{f}\right)^2 S_I(f) \qquad (62)$$

Using the expression given previously for input-referred flicker noise (42) and applying straightforward circuit analysis [27], the noise current arising from the diode-connected FET at the output of a current mirror with ratio $(1/A)$:1 is

$$S_I(f) = A \left(\frac{2I}{V_{efft}}\right)^2 \frac{K_f}{WLC'_{ox}f}. \qquad (63)$$

The resulting **SSB phase noise due to flicker noise** is

$$\mathcal{L}(f) = A \frac{K_f}{WLC'_{ox}f} \left(\frac{1}{V_{efft}^2}\right) \frac{f_0^2}{f^3}. \qquad (64)$$

Again, this is the phase noise that results only from noise in the FET that drives the common gate line for all the currents in the delay cells. As measurements will show, this is the dominant source of flicker noise.

VI. Experimental Validation

It can be difficult to measure the phase noise of ring oscillators accurately. Inverter-based oscillators are very sensitive to noise on the supply, so for accurate measurement they should be powered by heavily filtered batteries. In general, the VCO gain, or sensitivity, of a ring oscillator is much greater than of a varactor-tuned *LC* oscillator. Thus, noise on the control line can overwhelm internally generated phase noise in voltage-controlled ring oscillators.

With one exception, we have drawn upon published data on ring oscillator phase noise to validate the analysis. To also match analysis with SPECTRE-RF simulations, we obtained netlists and technology files from the designers of the original circuits. Most of our effort was directed to a careful validation of the differential ring oscillator, because for the reasons given previously, this is the circuit of choice for low-noise applications.

A. Inverter-Based Ring Oscillators

1) White Noise: [13] reports measured phase noise data on inverter-based ring oscillators in several generations of CMOS technology. A recent paper [31] uses that data to validate an expression for the minimum achievable phase noise in an idealized inverter-based ring oscillator. Our analysis, which is by comparison more direct and intuitive, under the same conditions as in [31] leads to the identical result (33). Therefore, the same measurements also validate our analysis.

2) Flicker Noise: Our analysis of the effects of flicker noise in inverter-based ring oscillators is the same as that of [32]. The two differ only in the expression for flicker noise in MOSFETs. Cast in the same terms, the two predict identical phase noise except for an integer factor. Ref. [32] suggests that it predicts measured phase noise exactly, but as it does not provide numerical values for the flicker noise coefficients, it is possible that the discrepancy has been absorbed into the noise coefficients. In the validations of differential ring oscillators, we show that the coefficient $K_f \approx 10^{-24}$ predicts phase noise consistently.

B. Differential Ring Oscillators

We found good measurements of phase noise in two publications on differential ring oscillators. "Good" means that our independent simulations and expressions are close in value to the reported data. The first [33] reports on a three-stage, 1.38-GHz ring oscillator in 0.5-μm CMOS that uses an NFET differential delay cell with antisymmetric PFET loads for greater immunity to supply noise [3]. The second [34] is a four-stage, 860-MHz ring oscillator in 0.18-μm CMOS that uses a PFET delay cell with a simple triode NFET load. In both cases, replica circuits stabilize amplitude.

1) White Noise: Flicker noise in ring oscillators can easily overwhelm white noise over frequency offsets as large as 1–10 MHz from the oscillation frequency. In [33] a 12-nF capacitor attached across the diode-connected FET in the frequency control line suppresses the most important source of flicker noise, so the measured phase noise is due to white noise alone (Fig. 11). As $A = 20$ in this circuit, this lowers flicker-induced phase noise by 20×, and another 3× because flicker noise is now decorrelated in all three stages. This amounts to

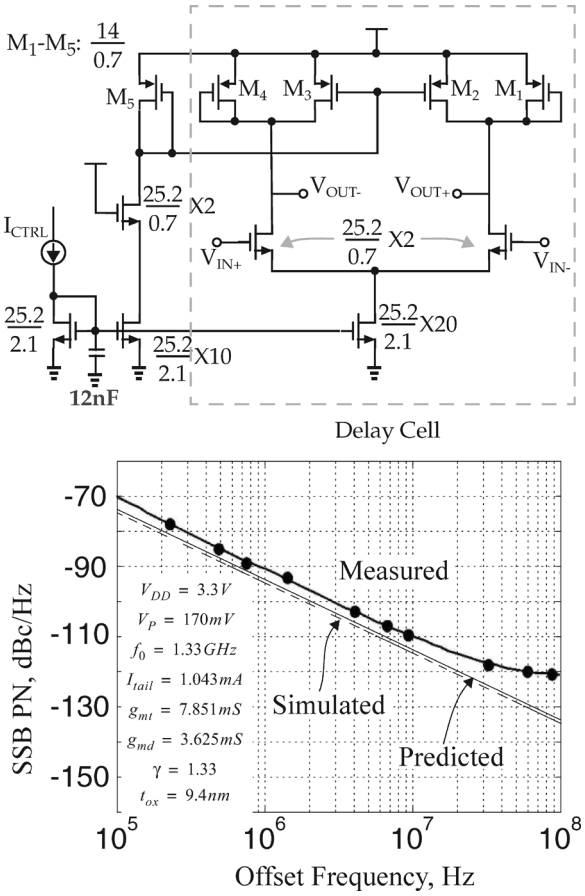

Fig. 11. Differential delay cell with decoupled tail current control FET. Measured phase noise of ring oscillator is compared with prediction due to noise in delay stages only, and simulation of complete circuit.

a 60× lower flicker noise corner frequency. This decoupling method is suitable for open-loop measurement only; it is not a practical way to suppress phase noise in oscillators that will be embedded in a phase-locked loop (PLL), because in most cases the lengthy loop settling time will be unacceptable.

Fig. 11 shows three plots superimposed: the *measured* phase noise; SPECTRE-RF *simulation* of phase noise of the entire oscillator circuit, including all auxiliary circuits, using circuit parameters shown in the inset; and *prediction* based on our equation (60). To account for departures from square law, we have substituted simulated g_{mt} and g_{md} in this expression. Simulation and prediction coincide, while measurement is about 3 dB higher. The flattening out of phase noise at 30 MHz offset is due to the white noise floor of the instruments.

In the ring oscillator in [34], the diode-connected tail control FET is not decoupled (Fig. 12). As $A = 40$ in this circuit, flicker noise dominates measurement. However, using the netlist and FET models in hand we have simulated the phase noise due to white noise only by instructing SPECTRE to turn off flicker noise. Fig. 12 shows the result: simulation (with flicker noise turned off) and prediction based on our equation (60) match exactly.

The next section contains a third validation of white noise, which shows similar agreement between full simulation and prediction.

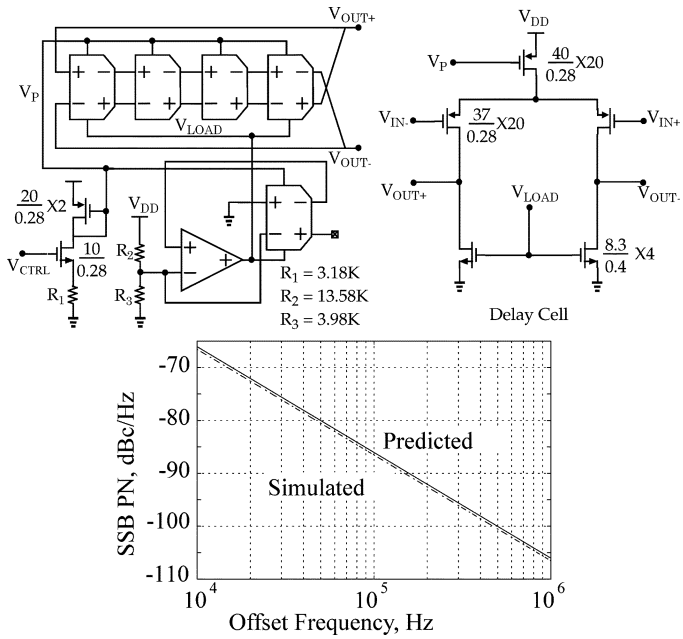

Fig. 12. Differential ring oscillator, in which white noise cannot be measured up to 1 MHz offset. Simulated phase noise, with flicker noise turned off, is compared with predictions based on noise in delay stages.

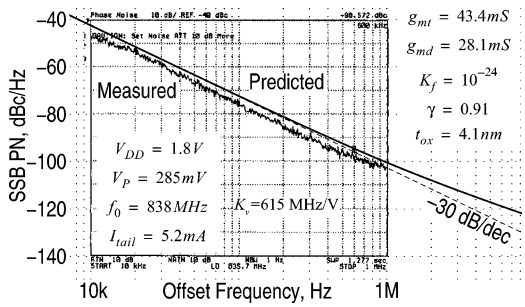

Fig. 13. Measured noise is dominated by flicker noise. This is compared with prediction, where tail current control FET noise dominates. Measurement at 1 MHz offset shows beginnings of predicted change in slope at onset of white noise.

We can draw the following conclusions.

1) The simple expression (60) predicts the total white-noise-induced phase noise in a differential ring oscillator accurately.
2) As this expression calculates only the *white noise in the delay stages*, validation proves that this is in fact the dominant source of phase noise. White noise in auxiliary support circuits such as for amplitude or frequency control is usually not important.

2) Flicker Noise: Flicker noise dominates the measured phase noise in [34] up to an offset of 1 MHz (Fig. 13). Using the simulated VCO gain κ_v and (64), we predict the phase noise caused by flicker noise due to the diode-connected PFET and the degenerated control NFET. We use the same flicker noise coefficient K_f for both. Also, we predict phase noise induced by white noise with the expression (60). The composite prediction is plotted against the measurement. Flicker noise is off only by about 4 dB, which is very acceptable. Moreover,

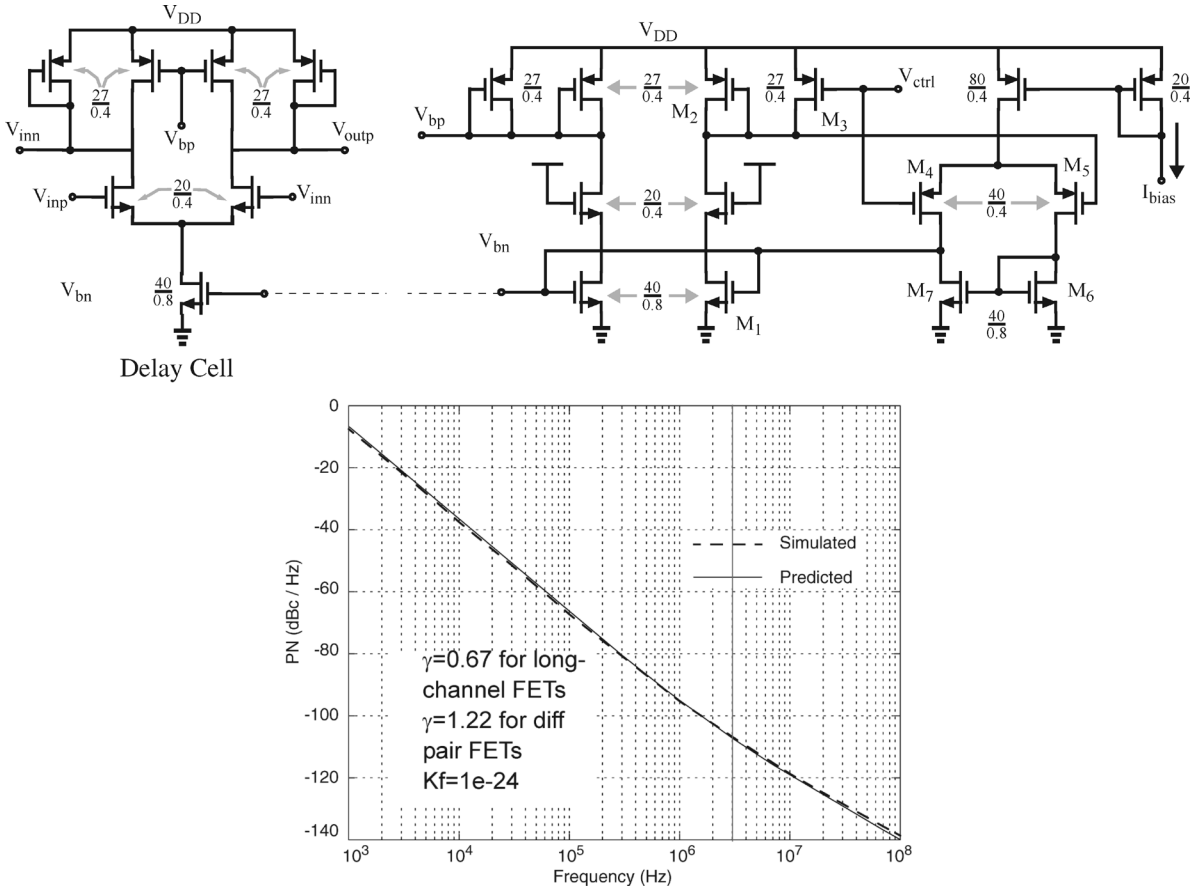

Fig. 14. Differential ring oscillator whose measured phase noise was, due to external noise sources, well above simulation. Composite prediction of flicker and white noise-induced phase noise corresponds exactly with simulation.

the analysis shows that the slight change of slope measured at 1 MHz offset is due to the onset of white noise.

We have designed a three-stage, 1-GHz ring oscillator in 0.35-μm CMOS as part of a disk drive read channel [35] (Fig. 14). It uses NFET-based delay stages and an antisymmetrical load. Although its measured jitter was low enough for the application, the phase noise was several dBs larger than simulation. We believe that we failed to take into account random FM caused by noise on the frequency control (bias) current in the transconductor driven by the PLL filter. Therefore, we use SPECTRE-RF simulation to estimate the true inherent phase noise of this circuit due to both flicker and white noise, except in the bias which is assumed noiseless. This is a worthwhile exercise because we know the circuit details fully. In this circuit $A = 1$, but tail current modulation by the large input-referred flicker noise voltage of the operational transconductance amplifier (OTA) M_4–M_7 multiplied by $g_m(M_2)$ causes phase noise. Only this source of noise is used for predictions.

The fit between our expressions for composite phase noise and simulation is striking. The phase noise simulation includes all auxiliary circuits that tune frequency and control amplitude. The inset shows the parameter values used. This serves as further validation of both white and flicker noise.

We may conclude that:

1) the simple expression (64) predicts phase noise due to flicker noise accurately enough for the purposes of first-time right design;
2) flicker noise in the controlling branch of the tail currents dominates the total close-in phase noise.

VII. Ring Oscillator or *LC* Oscillator?

Faced with the need for a high-frequency oscillator on a communications IC, the circuit designer must decide between a ring oscillator and an *LC* oscillator. The tradeoffs are broadly understood: for a given power budget, ring oscillators are compact but noisy, whereas *LC* oscillators consume considerably more chip area but are low noise. We are now in a position to explore this tradeoff quantitatively. Assume that the oscillator is inside a PLL which suppresses flicker noise, so white noise is the basis for comparison.

The mechanisms of phase noise in the commonly used differential *LC* oscillator (Fig. 15) are well understood [36]. The total phase noise due to white noise is given by

$$\mathcal{L}(f) = \frac{4kTRF}{A^2}\left(\frac{f_0}{2Qf}\right)^2 \tag{65}$$

where Q is the unloaded quality factor of the resonator at frequency f_0, and the circuit-specific noise factor F is given by

$$F = 1 + \frac{2\gamma IR}{\pi V_{op}} + \frac{\gamma IR}{2V_{efft}} = 1 + \gamma + \gamma\frac{\pi V_{op}}{4V_{efft}}. \tag{66}$$

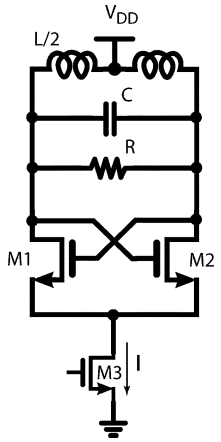

Fig. 15. Differential *LC* oscillator.

Let us assume that this oscillator is designed optimally: that is, its output swing is the largest possible, $V_{op} \simeq 2V_{\rm DD}$; and a filter [37] suppresses its tail current noise, the third and largest term in (66). Then the phase noise reduces to

$$\mathcal{L}(f) = \frac{\rm kT}{IV_{\rm DD}} \frac{\pi(1+\gamma)}{4Q^2} \left(\frac{f_0}{f}\right)^2. \tag{67}$$

We will compare the current consumptions of the two oscillators, I_{LC} and I_{RO}, for the same phase noise at the same frequency by substituting $I = I_{LC}$ in (67) and $I = I_{RO}/M$ in (60), and equating the two expressions. Then

$$I_{RO} \approx M \times 8Q^2 \frac{V_{\rm DD}}{V_{efft}||V_{effd}} I_{LC}. \tag{68}$$

Suppose the differential ring oscillator consists of the smallest practical number of stages, $M = 3$, and operates at $V_{\rm DD} = 1\,{\rm V}$. Its FETs are biased at, say, $V_{\rm eff} = V_{\rm DD}/5$. Then

$$I_{RO} \approx 50Q^2 I_{LC}.$$

If $Q \approx 3$, the ring oscillator takes $450\times$ the current of the *LC* oscillator. Admittedly, comparison with a highly refined *LC* oscillator that needs two spiral inductors is extreme, even unfair, but it does highlight the impracticality of using a ring oscillator in applications such as wireless receivers for cellular use.

VIII. Conclusion

Using a simple square-law FET model, we are able to predict phase noise in CMOS ring oscillators arising from white and flicker noise to a few dB of measurement and simulations. This is consistent with large-signal analyses of oscillators and mixers we have published previously, where we have found that simple models suffice for the purpose of hand calculations. These results yield insights into the principal mechanisms, and give a meaningful strategy for design optimization.

The main finding is that in the widely used differential ring oscillator, *white noise in the delay stages* and *flicker noise in the tuning current* are mainly responsible for jitter and phase noise. These effects are captured by simple expressions involving only a few terms. The analysis tools employed are simpler and easier to understand than in the prior literature.

With this analysis, it is possible to choose between a ring or an *LC* oscillator for given specifications, and then proceed to design the oscillator with no more effort than, say, a low-noise amplifier. The role of the simulator is mainly to verify hand calculations, not to serve as the primary tool for design.

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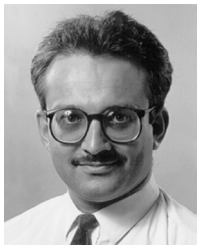

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