Introduction to Electronics

An Online Text

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Version 2.0

Dedication

Human beings are a delightful and complex amalgam of the spiritual, the emotional, the intellectual, and the physical.

This is dedicated to all of them; especially to those who honor and nurture me with their friendship and love.

Table of Contents

Preface

Philosophy of an Online Text

I think of myself as an educator rather than an engineer. And it has long seemed to me that, as educators, we should endeavor to bring to the student not only as much information as possible, but we should strive to make that information as accessible as possible, and as inexpensive as possible.

The technology of the Internet and the World Wide Web now allows us to virtually *give away* knowledge! Yet, we don't, choosing instead to write another conventional text book, and print, sell, and use it in the conventional manner. The "whys" are undoubtedly intricate and many; I offer only a few observations:

- *Any* change is difficult and resisted. This is true in the habits we form, the tasks we perform, the relationships we engage. It is simply *easier* not to change than it is to change. Though change is inevitable, it is not well-suited to the behavior of any organism.

- The proper reward structure is not in place. Faculty are supposedly rewarded for writing textbooks, thereby bringing fame and immortality to the institution of their employ.[1] The recognition and reward structure are simply not there for a text that is simply "posted on the web."

- No economic incentive exists to create and maintain a

[1] I use the word "supposedly" because, in my view, the official rewards for textbook authoring fall far short of what is appropriate and what is achievable through an equivalent research effort, despite all the administrative lip service to the contrary. These arguments, though, are more appropriately left to a different soapbox.

structure that allows *all* authors to publish in this manner; that allows students easy access to *all* such material, and that rigorously ensures the material will exceed a minimum acceptable quality.

If I were to do this the way I think it ought to be done, I would have prepared the course material in two formats. The first would be a text, identical to the textbooks with which you are familiar, but available online, and intended to be used in printed form. The second would be a slide presentation, à la Corel® Presentations™ or Microsoft® PowerPoint®, intended for use in the classroom or in an independent study.

But, alas, I am still on that journey, so what I offer you is a *hybrid* of these two concepts: an online text somewhat less verbose than a conventional text, but one that can also serve as classroom overhead transparencies.

Other compromises have been made. It would be advantageous to produce *two* online versions - one intended for use in printed form, and a second optimized for viewing on a computer screen. The two would carry identical information, but would be formatted with different page and font sizes. Also, to minimize file size, and therefore download times, font selection and variations are somewhat limited when compared to those normally encountered in a conventional textbook.

You may also note that exercise problems are not included with this text. By their very nature problems quickly can become “worn out.” I believe it is best to include problems in a separate document.

Until all of these enhancements exist, I hope you will find this a suitable and worthwhile compromise.

Enough of this; let’s get on with it...

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Generous monetary donations included with your request will be looked upon with great favor.

Review of Linear Circuit Techniques

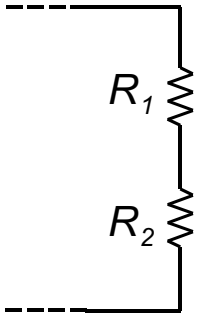

Fig. 1.
R's in series.

Resistors in Series

This is the simple one*!!!*

$$R_{total} = R_1 + R_2 + R_3 + \cdots \quad (1)$$

Resistors *must* carry the same current*!!!*

L's is series and C's in parallel have same form.

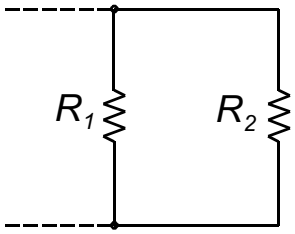

Fig. 2.
R's in parallel.

Resistors in Parallel

Resistors *must* have the same voltage*!!!*

Equation takes either of two forms:

Product Over Sum:

$$R_{total} = \frac{R_1 R_2}{R_1 + R_2} \quad (2)$$

Only valid for two resistors. Not calculator-efficient*!!!*

Inverse of Inverses:

$$R_{total} = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \cdots} \quad (3)$$

Always valid for multiple resistors. Very calculator-efficient*!!!*

L's in parallel and C's in series have same forms.

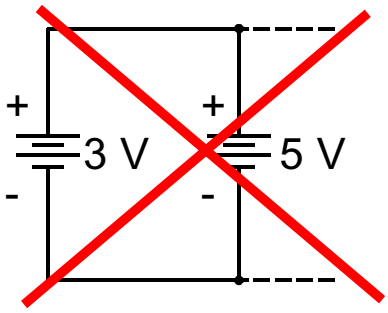

Fig. 3. Ideal voltage sources in parallel???

Ideal Voltage Sources

Cannot be connected in parallel*!!!*

Real voltage sources include a series resistance ("Thevenin equivalent"), and can be paralleled.

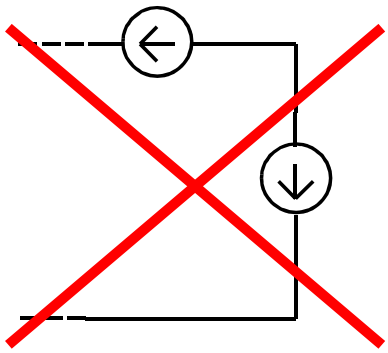

Fig. 4. Ideal current sources in series???

Ideal Current Sources

Cannot be connected in series*!!!*

Real current sources include a parallel resistance ("Norton equivalent"), and can be connected in series.

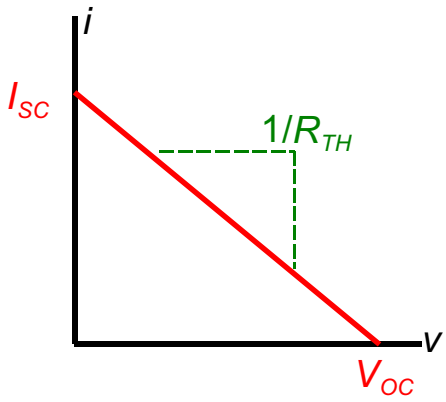

Fig. 5. Typical linear *i - v* characteristic of a real source.

Real Sources

All sources we observe in nature exhibit a decreasing voltage as they supply increasing current.

We presume that *i-v* relationship to be *linear*, so we can write the equations:

$$v = V_{OC} - i R_{TH} \quad \text{or} \quad i = I_{SC} - \frac{v}{R_{TH}} \qquad \textbf{(4)}$$

The linear equations help us *visualize* what *might* be inside of a real source:

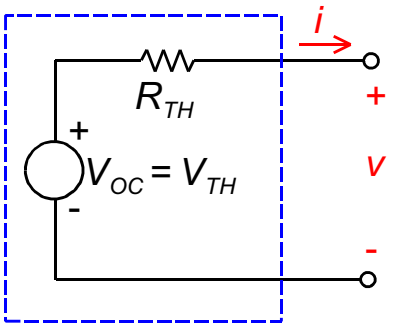

Fig. 6. Thevenin equivalent circuit.

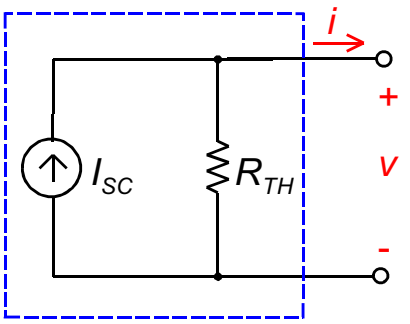

Fig. 7. Norton equivalent circuit.

Note that:

$$R_{TH} = \frac{V_{OC}}{I_{SC}} \qquad (5)$$

We can generalize this $\Rightarrow$ *any* linear resistive circuit can be represented as in Figs. 6 and 7.

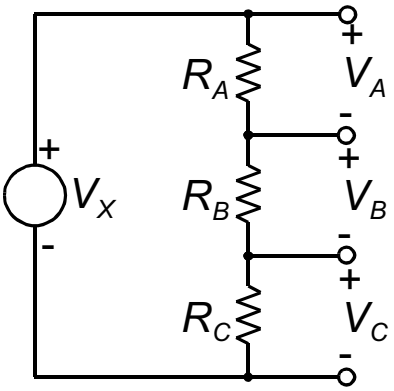

Fig. 8. Example of a voltage divider.

Voltage Dividers

Example - finding the voltage across R_B:

$$V_B = \frac{R_B}{R_A + R_B + R_C} V_X \qquad (6)$$

Resistors *must* be in series, i.e., they *must* carry the same current*!!!*

(Sometimes we cheat a little, and use the divider equation if the currents through the resistors are *almost* the same - we'll note this in class if that is the case)

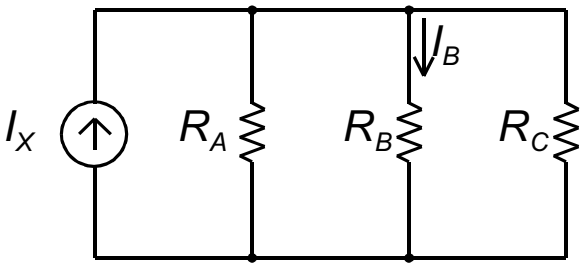

Fig. 9. Example of a current divider.

Current Dividers

$$I_B = \frac{\frac{1}{R_B}}{\frac{1}{R_A}+\frac{1}{R_B}+\frac{1}{R_C}} I_X \qquad (7)$$

Resistors must be in parallel, i.e., have the same voltage*!!!*

Superposition

Superposition applies to *any* linear circuit - in fact, *this is the definition of a linear circuit!!!*

An example of finding a response using superposition:

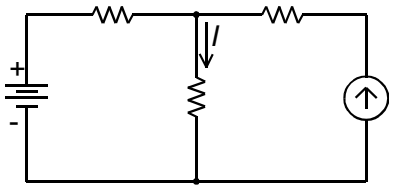

Fig. 10. The total response current I . . .

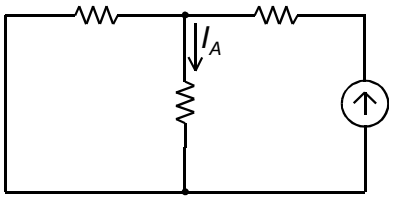

Fig. 11. . . . is the sum of the response I_A . . .

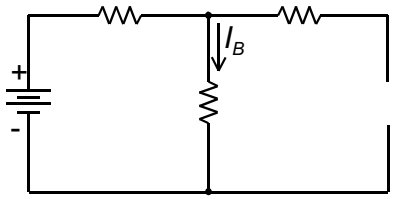

Fig. 12. . . . and the response I_B . . .

A quick exercise:

Use superposition and voltage division to show that V_X = 6 V:

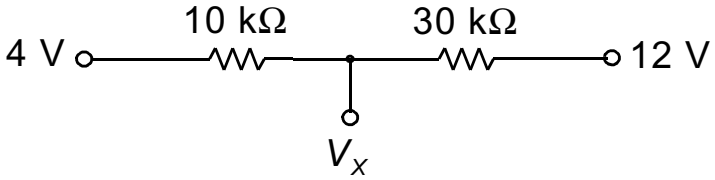

Fig. 13. A quick exercise . . .

What's missing from this review???

Node voltages / mesh currents . . .

For the kinds of problems you'll encounter in this course, I think you should *forget* about these analysis methods*!!!*

If there is any other way to solve a circuit problem, do it that other way . . . you'll arrive at the answer more efficiently, and with more insight.

You'll still need Ohm's and Kirchoff's Laws:

KVL: *Sum of voltages around a closed loop is zero.*

We'll more often use a different form:

Sum of voltages from point A to point B is the same regardless of the path taken.

KCL: *Sum of currents into a node (or area) is zero.*

I won't insult you by repeating Ohm's Law here . . .

Basic Amplifier Concepts

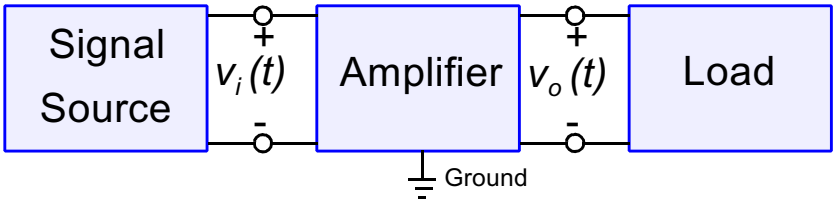

Fig. 14. Block diagram of basic amplifier.

Signal Source

A signal source is *anything* that provides the signal, e.g., . . .

. . . the carbon microphone in a telephone handset . . .

. . . the fuel-level sensor in an automobile gas tank . . .

Amplifier

An amplifier is a system that provides *gain* . . .

. . . sometimes *voltage gain* (illustrated below), sometimes *current gain*, always *power gain*.

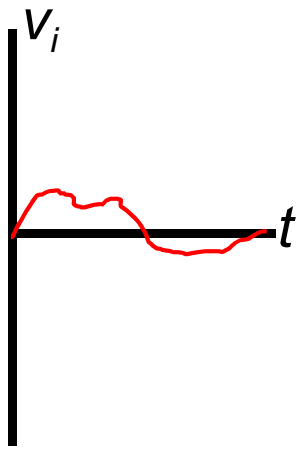

Fig. 15. Generic input signal voltage.

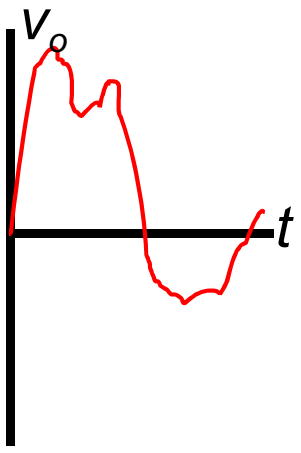

Fig. 16. Output voltage of noninverting amplifier.

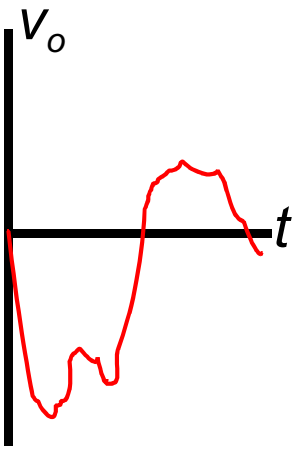

Fig. 17. Output voltage of inverting amplifier.

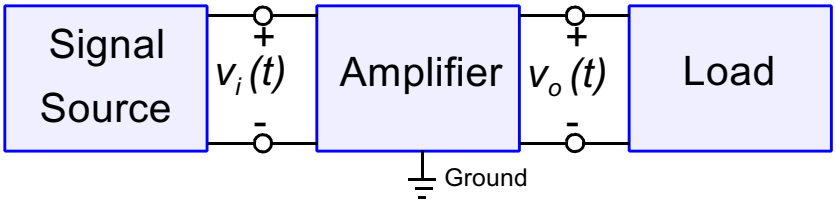

Fig. 18. Block diagram of basic amplifier (Fig. 14 repeated).

Load

The load is anything we deliver the amplified signal to, e.g., . . .

. . . loudspeaker . . .

. . . the leg of lamb in a microwave oven . . .

Ground Terminal

Usually there is a *ground* connection . . .

. . . usually common to input and output . . .

. . . maybe connected to a metal chassis . . .

. . . maybe connected to power-line ground . . .

. . . maybe connected to *both . . .*

. . . maybe connected to *neither . . . use caution!!!*

To work with (analyze and design) amplifiers

we need to *visualize* what *might* be inside all three blocks of Fig. 18, i.e., *we need models!!!*

Voltage Amplifier Model

This is usually the one we have the most intuition about . . .

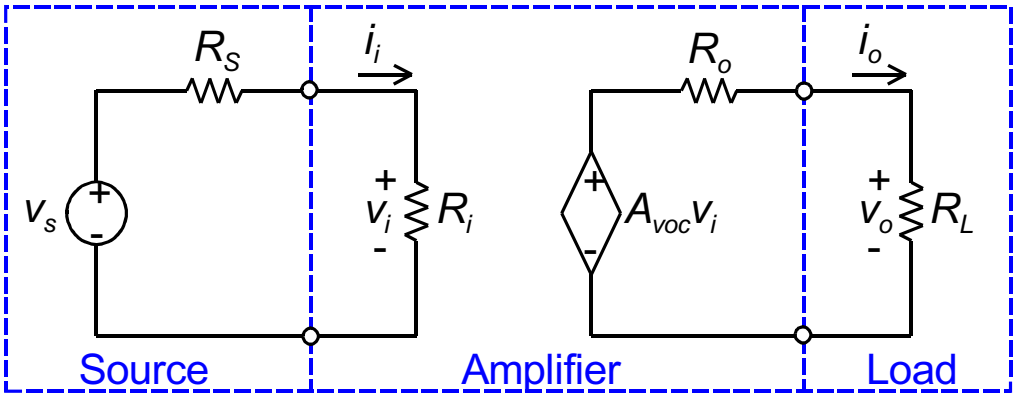

Fig. 19. Modeling the source, amplifier, and load with the emphasis on voltage.

Signal Source

Our emphasis is *voltage* . . . source voltage decreases as source current increases, as with any real source . . .

. . . so we use a *Thevenin equivalent*.

Amplifier Input

When the source is connected to the amplifier, current flows . . .

. . . the amplifier must have an *input resistance,* R_i.

Amplifier Output

Output voltage decreases as load current increases . . .

. . . again we use a *Thevenin equivalent*.

Load

Load current flows . . . the load appears as a *resistance,* R_L.

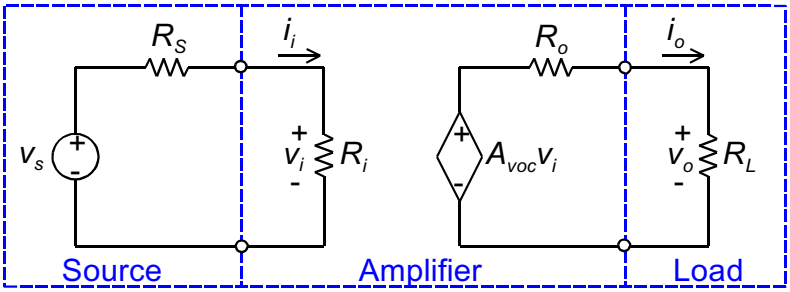

Fig. 20. Voltage amplifier model (Fig. 19 repeated).

Open-Circuit Voltage Gain

If we remove R_L (i.e., with $R_L = \infty$) the voltage of the Thevenin source in the amplifier output is the *open-circuit output voltage of the amplifier*. Thus, A_{voc} is called the *open-circuit voltage gain*:

$$A_{voc} = \left.\frac{v_o}{v_i}\right|_{R_L=\infty} \tag{8}$$

Voltage Gain

With a load in place our concept of voltage gain changes slightly:

$$A_V = \frac{v_o}{v_i} \quad \Rightarrow \quad v_o = \frac{R_L}{R_o + R_L} A_{voc} v_i \quad \Rightarrow \quad A_v = A_{voc} \frac{R_L}{R_o + R_L} \tag{9}$$

We can think of this as the amplifier voltage gain if the source were ideal:

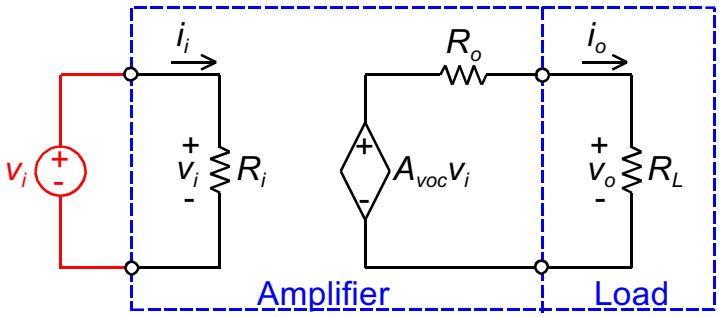

Fig. 21. $A_v = v_o/v_i$ illustrated.

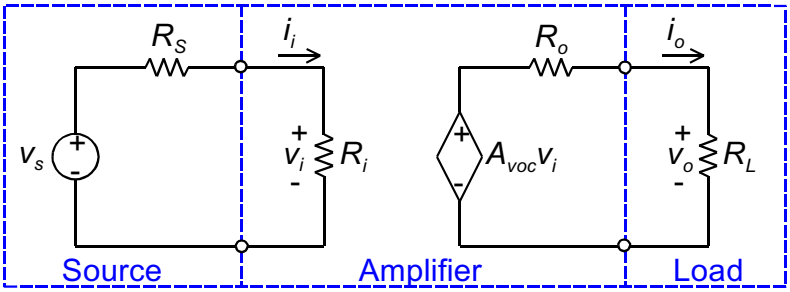

Fig. 22. Voltage amplifier model (Fig. 19 repeated).

With our "real" source model we define another useful voltage gain:

$$A_{vs} = \frac{v_o}{v_s} \quad \Rightarrow \quad v_i = \frac{R_i}{R_S + R_i} v_s \quad \Rightarrow \quad A_{vs} = A_{voc} \frac{R_i}{R_S + R_i} \frac{R_L}{R_o + R_L} \tag{10}$$

Notice that A_v and A_{vs} are both less than A_{voc}, due to *loading effects*.

Current Gain

We can also define the amplifier *current gain*:

$$A_i = \frac{i_o}{i_i} = \frac{v_o / R_L}{v_i / R_i} = \frac{v_o}{v_i} \frac{R_i}{R_L} = A_v \frac{R_i}{R_L} \tag{11}$$

Power Gain

Because the amplifier input and load are resistances, we have $P_o = V_o I_o$, and $P_i = V_i I_i$ (*rms* values). Thus:

$$G = \frac{P_o}{P_i} = \frac{V_o I_o}{V_i I_i} = A_v A_i = A_v{}^2 \frac{R_i}{R_L} = A_i{}^2 \frac{R_L}{R_i} \tag{12}$$

Power Supplies, Power Conservation, and Efficiency

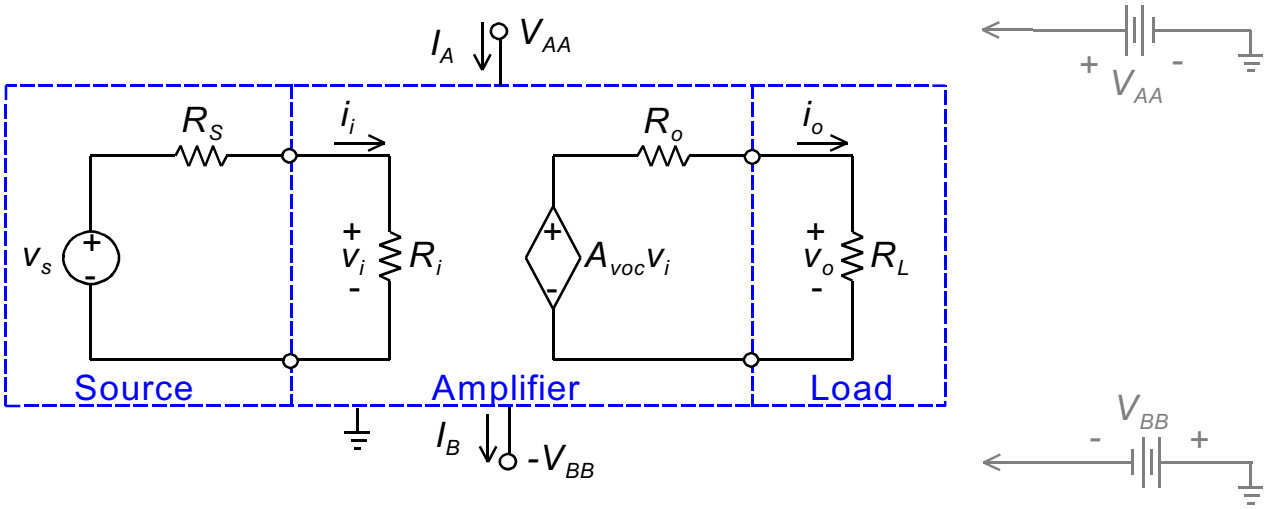

Fig. 23. Our voltage amplifier model showing power supply and ground connections.

The *signal power delivered to the load* is converted from the *dc power provided by the power supplies*.

DC Input Power

$$P_S = V_{AA}I_A + V_{BB}I_B \tag{13}$$

This is sometimes noted as P_{IN}. *Use care not to confuse this with the signal input power* P_i.

Conservation of Power

Signal power is delivered to the load $\Rightarrow P_o$

Power is dissipated within the amplifier as heat $\Rightarrow P_D$

The total input power must equal the total output power:

$$P_S + P_i = P_o + P_D \tag{14}$$

Virtually always $P_i << P_S$ and is neglected.

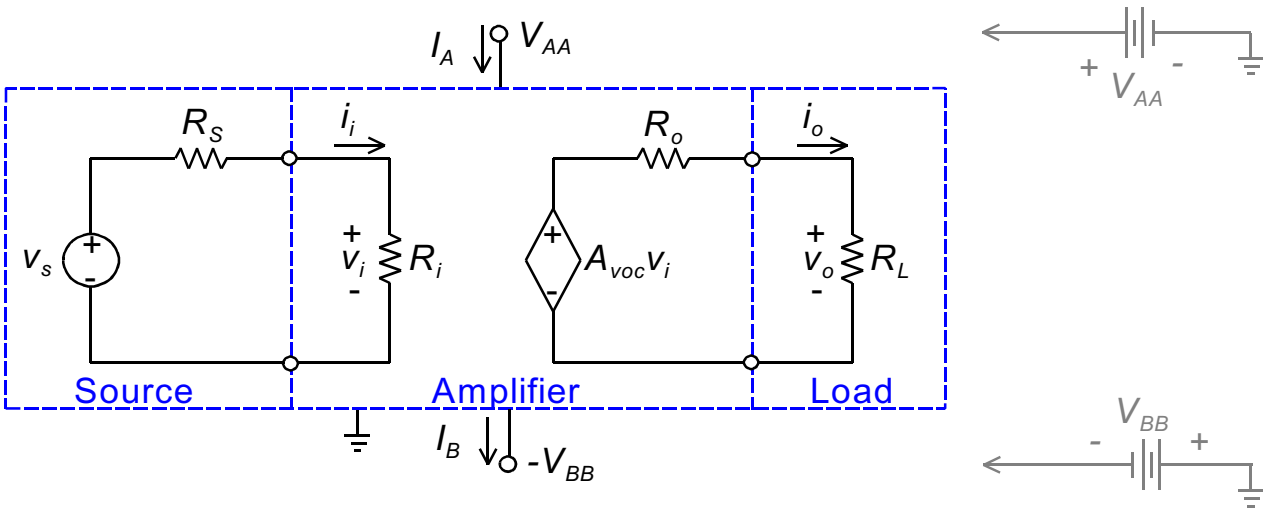

Fig. 24. Our voltage amplifier model showing power supply and ground connections (Fig. 23 repeated).

Efficiency

Efficiency is a figure of merit describing amplifier performance:

$$\eta = \frac{P_o}{P_S} \times 100\% \qquad \textbf{(15)}$$

Amplifier Cascades

Amplifier stages may be connected together (*cascaded*) :

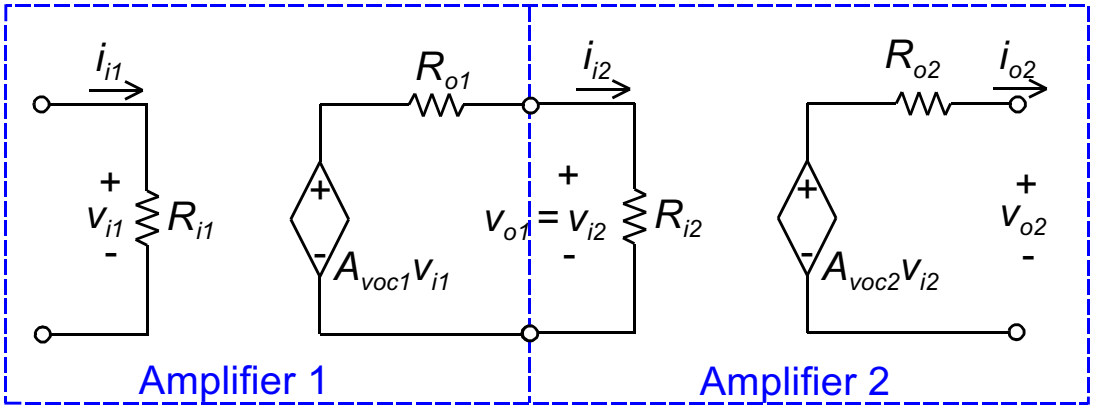

Fig. 25. A two-amplifier cascade.

Notice that stage 1 is loaded by the input resistance of stage 2.

Gain of stage 1:

$$A_{v1} = \frac{v_{o1}}{v_{i1}} \tag{16}$$

Gain of stage 2:

$$A_{v2} = \frac{v_{o2}}{v_{i2}} = \frac{v_{o2}}{v_{o1}} \tag{17}$$

Gain of cascade:

$$A_{voc} = \frac{v_{o1}}{v_{i1}}\frac{v_{o2}}{v_{o1}} = A_{v1}A_{v2} \tag{18}$$

We can replace the two models by a single model (remember, the model is just a *visualization* of what *might* be inside):

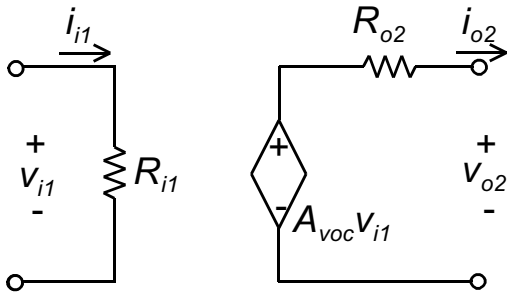

Fig. 26. Model of cascade.

Decibel Notation

Amplifier gains are often not expressed as simple ratios . . . rather they are mapped into a logarithmic scale.

The fundamental definition begins with a *power ratio*.

Power Gain

Recall that $G = P_o/P_i$, and define:

$$G_{dB} = 10\log G \tag{19}$$

G_{dB} is expressed in units of *decibels*, abbreviated *dB.*

Cascaded Amplifiers

We know that $G_{total} = G_1 G_2$. Thus:

$$G_{total,\,dB} = 10\log G_1 G_2 = 10\log G_1 + 10\log G_2 = G_{1,\,dB} + G_{2,\,dB} \tag{20}$$

Thus, the *product* of gains becomes the *sum* of gains in decibels.

Voltage Gain

To derive the expression for voltage gain in decibels, we begin by recalling from eq. (12) that $G = A_v^2(R_i/R_L)$. Thus:

$$\begin{aligned} 10\log G &= 10\log A_v^{\,2}\frac{R_i}{R_L} \\ &= 10\log A_v^{\,2} + 10\log R_i - 10\log R_L \qquad (21) \\ &= 20\log A_v + 10\log R_i - 10\log R_L \end{aligned}$$

Even though R_i may not equal R_L in most cases, we *define*:

$$A_{v\,dB} = 20 \log A_v \qquad \textbf{(22)}$$

Only when R_i does equal R_L, will the *numerical values* of G_{dB} and $A_{v\,dB}$ be the same. In all other cases they will differ.

From eq. (22) we can see that in an amplifier cascade the *product* of voltage gains becomes the *sum* of voltage gains in decibels.

Current Gain

In a manner similar to the preceding voltage-gain derivation, we can arrive at a similar definition for current gain:

$$A_{i\,dB} = 20 \log A_i \qquad \textbf{(23)}$$

Using Decibels to Indicate Specific Magnitudes

Decibels are *defined* in terms of *ratios*, but are often used to indicate a specific magnitude of voltage or power.

This is done by defining a reference and referring to it in the units notation:

Voltage levels:

dBV, decibels with respect to 1 V . . . for example,

$$3.16 \text{ V} = 20 \log \frac{3.16 \text{ V}}{1 \text{ V}} = 10 \text{ dBV} \qquad \textbf{(24)}$$

Power levels:

dBm, decibels with respect to 1 mW . . . for example

$$5\ \text{mW} = 10\log\frac{5\ \text{mW}}{1\ \text{mW}} = 6.99\ \text{dBm} \quad \textbf{(25)}$$

dBW, decibels with respect to 1 W . . . for example

$$5\ \text{mW} = 10\log\frac{5\ \text{mW}}{1\ \text{W}} = -23.0\ \text{dbW} \quad \textbf{(26)}$$

There is a 30 dB difference between the two previous examples because 1 mW = - 30 dBW and 1 W = +30 dBm.

Other Amplifier Models

Recall, our voltage amplifier model arose from our *visualization* of what *might* be inside a real amplifier:

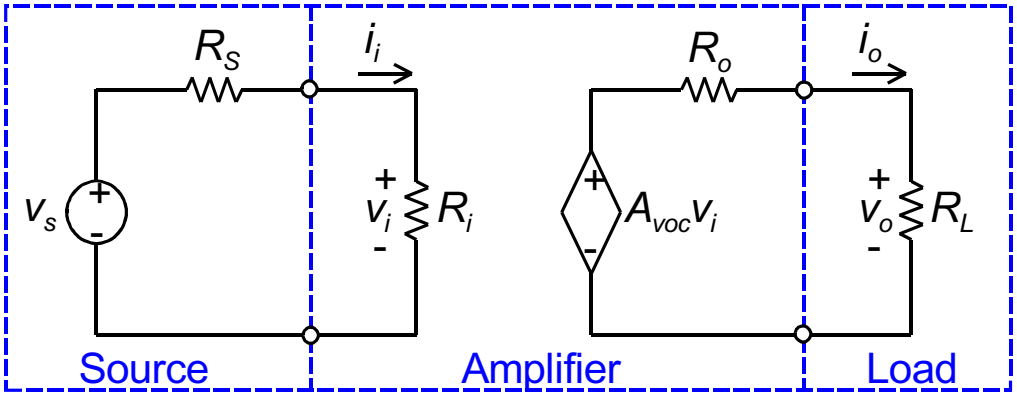

Fig. 27. Modeling the source, amplifier, and load with the emphasis on voltage (Fig. 19 repeated).

Current Amplifier Model

Suppose we choose to emphasize *current*. In this case we use Norton equivalents for the signal source and the amplifier:

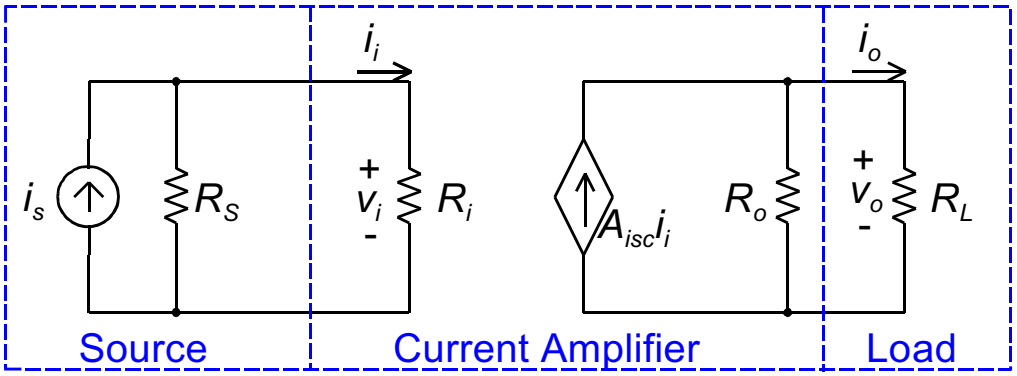

Fig. 28. Modeling the source, amplifier, and load with the emphasis on current.

The *short-circuit current gain* is given by:

$$A_{isc} = \left.\frac{i_o}{i_i}\right|_{R_L=0} \tag{27}$$

Transconductance Amplifier Model

Or, we could emphasize *input voltage* and *output current*:

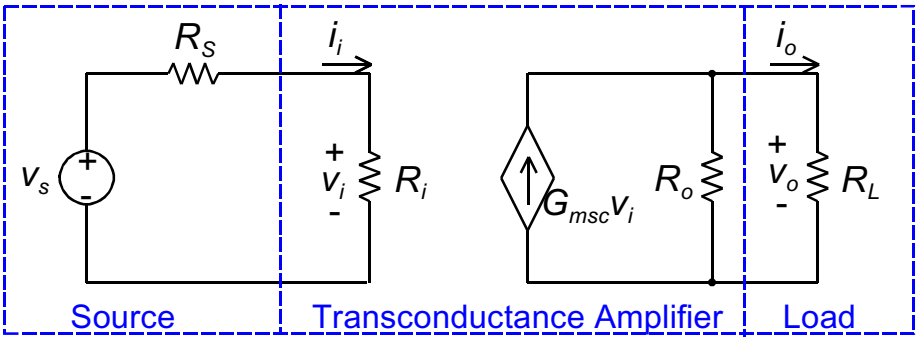

Fig. 29. The transconductance amplifier model.

The *short-circuit transconductance gain* is given by:

$$G_{msc} = \left.\frac{i_o}{v_i}\right|_{R_L=0} \quad \text{(siemens, S)} \tag{28}$$

Transresistance Amplifier Model

Our last choice emphasizes *input current* and *output voltage*:

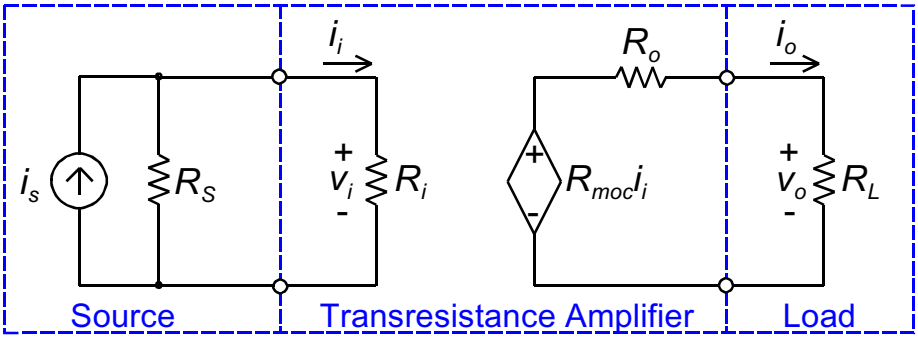

Fig. 30. The transresistance amplifier model.

The *open-circuit transresistance gain* is given by:

$$R_{moc} = \left.\frac{v_o}{i_i}\right|_{R_L=\infty} \quad \text{(ohms, } \Omega\text{)} \tag{29}$$

Any of these four models can be used to represent what *might* be inside of a real amplifier.

Any of the four can be used to model the same amplifier!!!

- Models obviously will be different *inside* the amplifier.
- If the model parameters are chosen properly, they will behave *identically at the amplifier terminals!!!*

We can change from any kind of model to any other kind:

- Change Norton equivalent to Thevenin equivalent (if necessary).
- Change the dependent source's variable of dependency with Ohm's Law $\Rightarrow$ $v_i = i_i R_i$ (if necessary).

Try it*!!!* Pick some values and practice*!!!*

Amplifier Resistances and Ideal Amplifiers

Ideal Voltage Amplifier

Let's re-visit our voltage amplifier model:

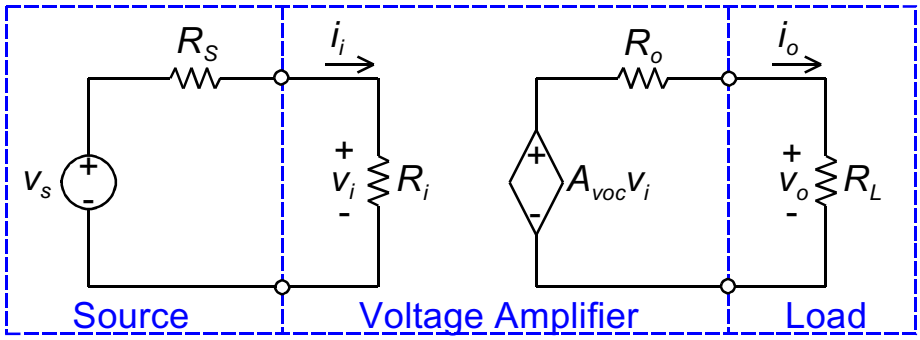

Fig. 31. Voltage amplifier model.

We're thinking *voltage*, and we're thinking *amplifier* . . . so how can we maximize the voltage that gets delivered to the load ?

- We can get the most voltage out of the signal source if $R_i >> R_S$, i.e., if the amplifier can "measure" the signal voltage with a high input resistance, like a voltmeter does.

  In fact, if $R_i \Rightarrow \infty$, *we won't have to worry about the value of* R_S *at all!!!*

- We can get the most voltage out of the amplifier if $R_o << R_L$, i.e., if the amplifier can look as much like a voltage source as possible.

  In fact, if $R_o \Rightarrow 0$, *we won't have to worry about the value of* R_L *at all!!!*

So, in an ideal world, we could have an *ideal amplifier!!!*

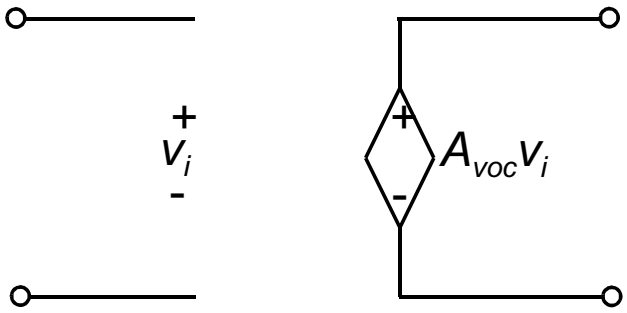

Fig. 32. Ideal voltage amplifier. Signal source and load are omitted for clarity.

An ideal amplifier is only a *concept;* we cannot build one.

But an amplifier may *approach* the ideal, and we may use the model, if only for its simplicity.

Ideal Current Amplifier

Now let's revisit our current amplifier model:

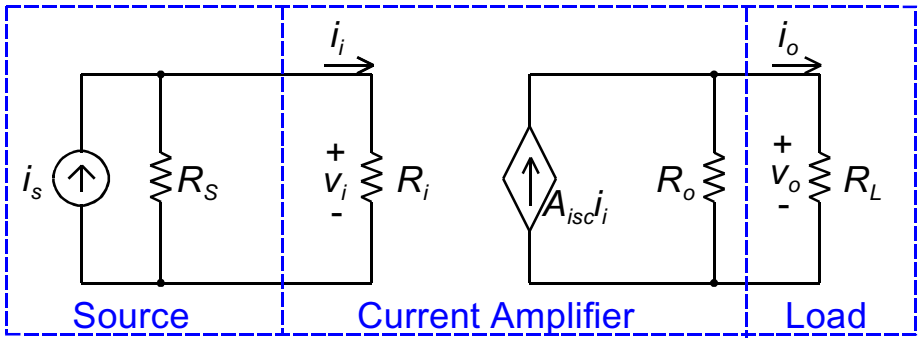

Fig. 33. Current amplifier model (Fig. 28 repeated).

How can we maximize the current that gets delivered to the load ?

- We can get the most current out of the signal source if $R_i << R_S$, i.e., if the amplifier can "measure" the signal current with a low input resistance, like an ammeter does.

  In fact, if $R_i \Rightarrow 0$, *we won't have to worry about the value of* R_S *at all!!!*

- We can get the most current out of the amplifier if $R_o >> R_L$, i.e., if the amplifier can look as much like a current source as possible.

  In fact, if $R_o \Rightarrow \infty$, we won't have to worry about the value of R_L at all!!!

This leads us to our conceptual *ideal current amplifier*:

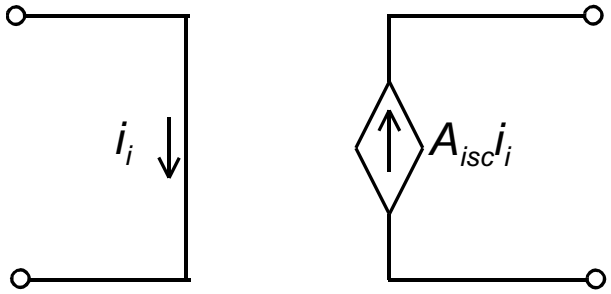

Fig. 34. Ideal current amplifier.

Ideal Transconductance Amplifier

With a mixture of the previous concepts we can conceptualize an *ideal transconductance amplifier.*

This amplifier ideally measures the *input voltage* and produces an *output current*:

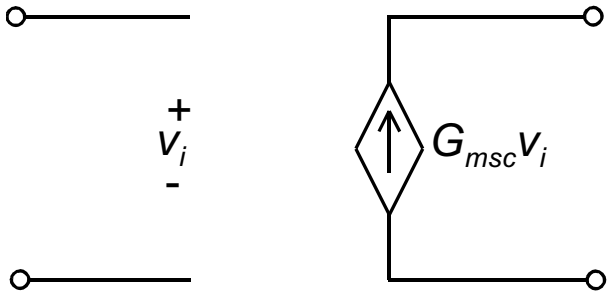

Fig. 35. Ideal transconductance amplifier.

Ideal Transresistance Amplifier

Our final ideal amplifier concept measures *input current* and produces an *output voltage*:

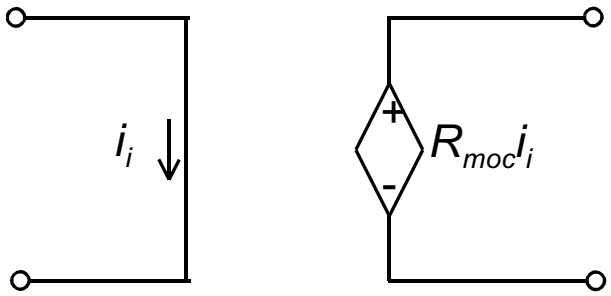

Fig. 36. Ideal transresistance amplifier.

Uniqueness of Ideal Amplifiers

Unlike our models of "real" amplifiers, ideal amplifier models cannot be converted from one type to another (try it . . .).

Frequency Response of Amplifiers

Terms and Definitions

In real amplifiers, gain changes with frequency . . .

"Frequency" implies sinusoidal excitation which, in turn, implies *phasors* . . . using voltage gain to illustrate the general case:

$$\mathbf{A_v} = \frac{\mathbf{V_o}}{\mathbf{V_i}} = \frac{|\mathbf{V_o}|\angle\mathbf{V_o}}{|\mathbf{V_i}|\angle\mathbf{V_i}} = |\mathbf{A_v}|\angle\mathbf{A_v} \qquad (30)$$

Both $|\mathbf{A_v}|$ and $\angle\,\mathbf{A_v}$ are functions of frequency and can be plotted.

Magnitude Response:

A plot of $|\mathbf{A_v}|$ vs. *f* is called the *magnitude response* of the amplifier.

Phase Response:

A plot of $\angle\,\mathbf{A_v}$ vs. *f* is called the *phase response* of the amplifier.

Frequency Response:

Taken together the two responses are called the *frequency response* . . . though often in common usage the term frequency response is used to mean only the magnitude response.

Amplifier Gain:

The *gain* of an amplifier usually refers only to the magnitudes:

$$|\mathbf{A_v}|_{dB} = 20\log|\mathbf{A_v}| \qquad (31)$$

The Magnitude Response

Much terminology and measures of amplifier performance are derived from the magnitude response . . .

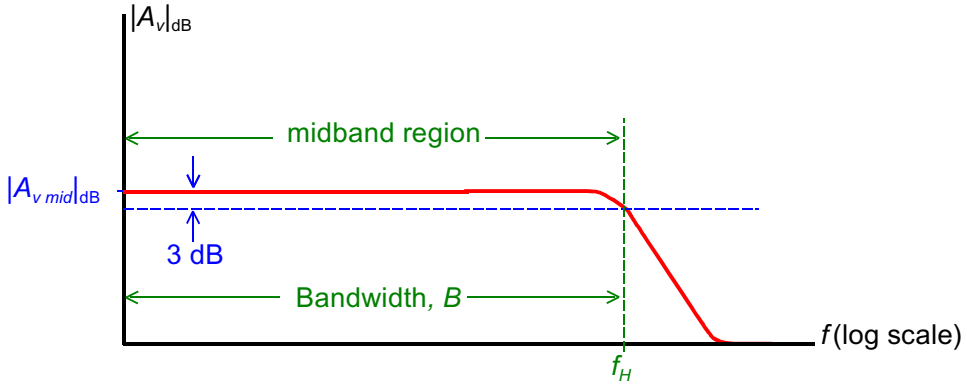

Fig. 37. Magnitude response of a *dc-coupled*, or *direct-coupled* amplifier.

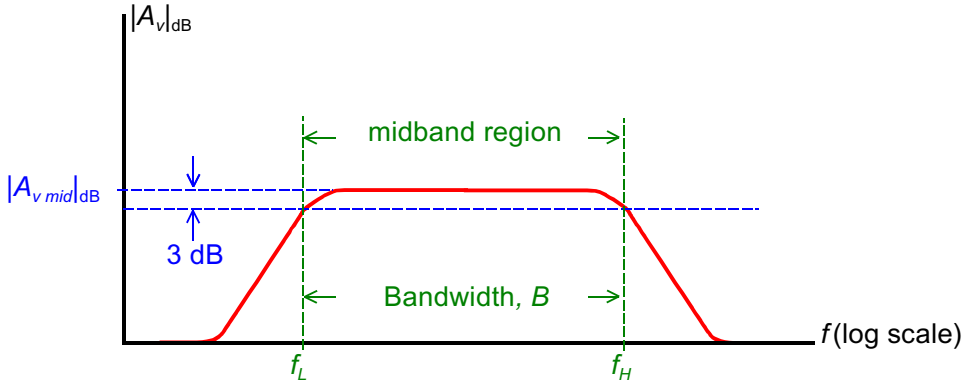

Fig. 38. Magnitude response of an *ac-coupled*, or *RC-coupled* amplifier.

$|A_{v\,mid}|_{dB}$ is called the *midband gain* . . .

f_L and f_H are the *3-dB frequencies*, the *corner frequencies*, or the *half-power frequencies* (why this last one?) . . .

B is the *3-dB bandwidth*, the *half-power bandwidth*, or simply the *bandwidth* (of the *midband region*) . . .

Causes of Reduced Gain at Higher Frequencies

Stray wiring inductances . . .

Stray capacitances . . .

Capacitances in the amplifying devices (not yet included in our amplifier models) . . .

The figure immediately below provides an example:

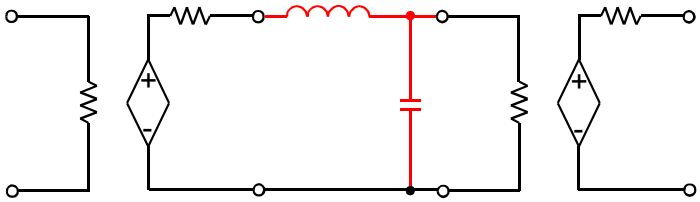

Fig. 39. Two-stage amplifier model including stray wiring inductance and stray capacitance between stages. These effects are also found within each amplifier stage.

Causes of Reduced Gain at Lower Frequencies

This decrease is due to capacitors placed between amplifier stages (in *RC-coupled* or *capacitively-coupled* amplifiers) . . .

This prevents dc voltages in one stage from affecting the next.

Signal source and load are often coupled in this manner also.

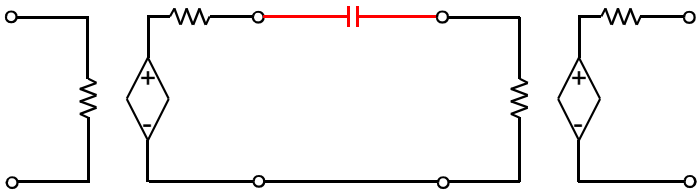

Fig. 40. Two-stage amplifier model showing capacitive coupling between stages.

Differential Amplifiers

Many desired signals are weak, *differential signals* in the presence of much stronger, *common-mode signals*.

Example:

Telephone lines, which carry the desired voice signal *between* the green and red (called *tip* and *ring*) wires.

The lines often run parallel to power lines for miles along highway right-of-ways . . . resulting in an induced 60 Hz voltage (as much as 30 V or so) from each wire to ground.

We must extract and amplify the voltage *difference* between the wires, while ignoring the large voltage *common* to the wires.

Modeling Differential and Common-Mode Signals

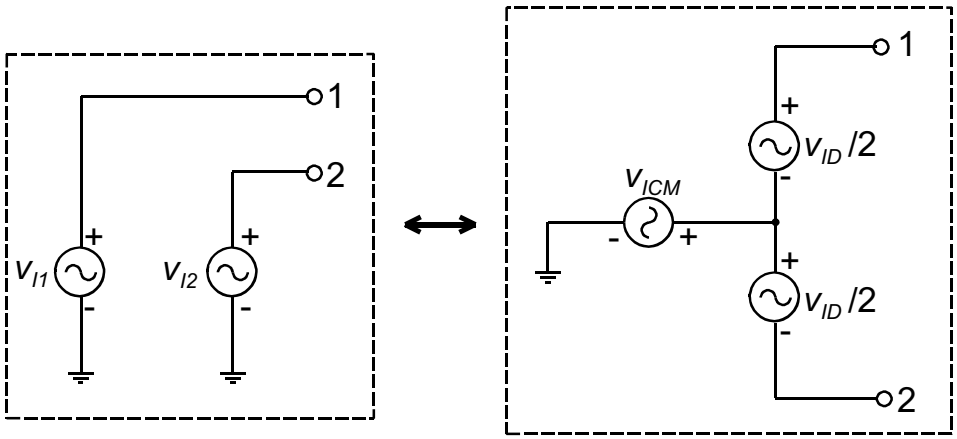

Fig. 41. Representing two sources by their *differential* and *common-mode* components.

As shown above, *any* two signals can be modeled by a *differential* component, v_{ID}, and a *common-mode* component, v_{ICM}, *if:*

$$v_{I1} = v_{ICM} + \frac{v_{ID}}{2} \quad \text{and} \quad v_{I2} = v_{ICM} - \frac{v_{ID}}{2} \tag{32}$$

Solving these simultaneous equations for v_{ID} and v_{ICM}:

$$v_{ID} = v_{I1} - v_{I2} \qquad \text{and} \qquad v_{ICM} = \frac{v_{I1} + v_{I2}}{2} \tag{33}$$

Note that the *differential* voltage v_{ID} is the *difference* between the signals v_{I1} and v_{I2}, while the *common-mode* voltage v_{ICM} is the *average* of the two (a measure of how they are similar).

Amplifying Differential and Common-Mode Signals

We can use superposition to describe the performance of an amplifier with these signals as inputs:

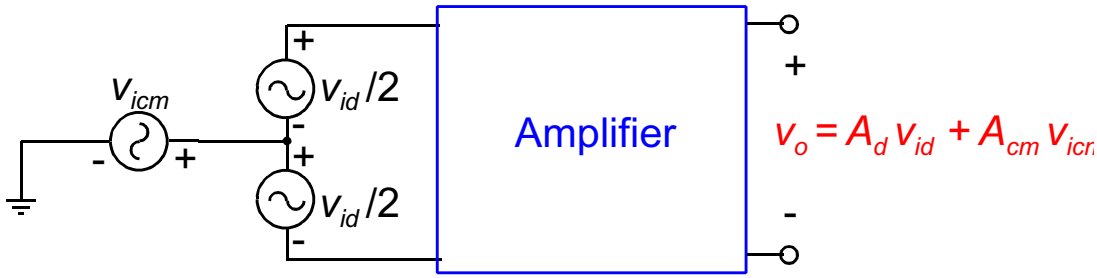

Fig. 42. Amplifier with differential and common-mode input signals.

A *differential amplifier* is designed so that A_d is very large and A_{cm} is very small, preferably zero.

Differential amplifier circuits are quite clever - they are the basic building block of all operational amplifiers

Common-Mode Rejection Ratio

A figure of merit for "diff amps," CMRR is expressed in decibels:

$$CMRR_{dB} = 20\log\frac{|A_d|}{|A_{cm}|} \tag{34}$$

Ideal Operational Amplifiers

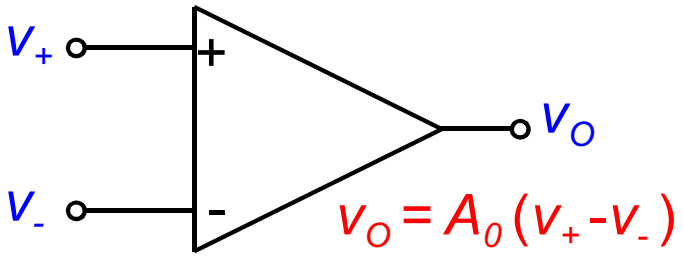

Fig. 43. The ideal operational amplifier: schematic symbol, input and output voltages, and input-output relationship.

The *ideal operational amplifier* is an ideal *differential amplifier:*

$$A_0 = A_d = \infty \qquad A_{cm} = 0$$

$$R_i = \infty \qquad R_o = 0$$

$$B = \infty$$

The input marked "+" is called the *noninverting* input . . .

The input marked "-" is called the *inverting* input . . .

The model, just a voltage-dependent voltage source with the gain $A_0 (v_+ - v_-)$, is so simple that you should get used to analyzing circuits with just the schematic symbol.

Ideal Operational Amplifier Operation

With $A_0 = \infty$, we can conceive of three rules of operation:

1. If $v_+ > v_-$ then v_o increases . . .
2. If $v_+ < v_-$ then v_o decreases . . .
3. If $v_+ = v_-$ then v_o does not change . . .

In a real op amp v_o cannot exceed the dc power supply voltages, which are not shown in Fig. 43.

In normal use as an amplifier, an operational amplifier circuit employs *negative feedback* - a fraction of the output voltage is applied to the *inverting* input.

Op Amp Operation with Negative Feedback

Consider the effect of negative feedback:

- If $v_+ > v_-$ then v_o increases . . .

  Because a fraction of v_o is applied to the inverting input, v_- increases . . .

  The "gap" between v_+ and v_- is reduced and will eventually become zero . . .

  Thus, v_o takes on the value that causes $v_+ - v_- = 0$!!!

- If $v_+ < v_-$ then v_o decreases . . .

  Because a fraction of v_o is applied to the inverting input, v_- decreases . . .

  The "gap" between v_+ and v_- is reduced and will eventually become zero . . .

  Thus, v_o takes on the value that causes $v_+ - v_- = 0$!!!

In either case, the output voltage takes on whatever value that causes $v_+ - v_- = 0$!!!

In analyzing circuits, then, we need only determine the value of v_o which will cause $v_+ - v_- = 0$.

Slew Rate

So far we have said nothing about the *rate* at which v_o increases or decreases . . . this is called the *slew rate*.

In our ideal op amp, we'll presume the slew rate is as fast as we need it to be (i.e., infinitely fast).

Op Amp Circuits - The Inverting Amplifier

Let's put our ideal op amp concepts to work in this basic circuit:

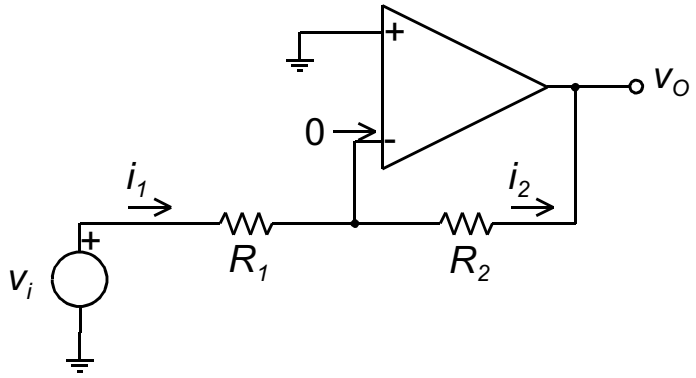

Fig. 44. Inverting amplifier circuit.

Voltage Gain

Because the ideal op amp has $R_i = \infty$, the current into the inputs will be zero.

This means $i_1 = i_2$, i.e., resistors *R_1 and R_2 form a voltage dividerIII*

Therefore, we can use *superposition* to find the voltage v_-.

(Remember the quick exercise on p. 4 *???* This is the identical problem*!!!*):

$$v_- = \frac{v_i R_2 + v_o R_1}{R_1 + R_2} \qquad \textbf{(35)}$$

Now, *because there is negative feedback*, v_o takes on whatever value that causes $v_+ - v_- = 0$, and $v_+ = 0$ *!!!*

Thus, setting eq. (35) to zero, we can solve for v_o:

$$v_i R_2 + v_o R_1 = 0 \quad \Rightarrow \quad v_o = -\frac{R_2}{R_1} v_i \quad \Rightarrow \quad A_v = -\frac{R_2}{R_1} \qquad \textbf{(36)}$$

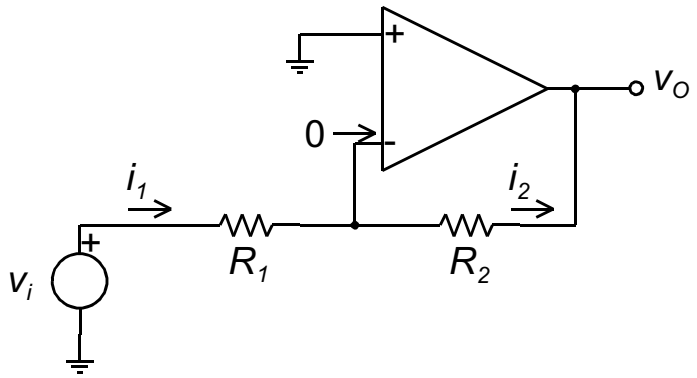

Fig. 45. Inverting amplifier circuit (Fig. 44 repeated).

Input Resistance

This means resistance "seen" by the signal source v_i, not the input resistance of the op amp, which is infinite.

Because $v_- = 0$, the voltage across R_1 is v_i. Thus:

$$i_1 = \frac{v_i}{R_1} \quad \Rightarrow \quad R_{in} = \frac{v_i}{i_1} = \frac{v_i}{\frac{v_i}{R_1}} = R_1 \tag{37}$$

Output Resistance

This is the Thevenin resistance which would be "seen" by a load looking back into the circuit (Fig. 45 does not show a load attached).

Our op amp is ideal; its Thevenin output resistance is zero:

$$R_O = 0 \tag{38}$$

Op Amp Circuits - The Noninverting Amplifier

If we switch the v_i and ground connections on the inverting amplifier, we obtain the *noninverting amplifier*:

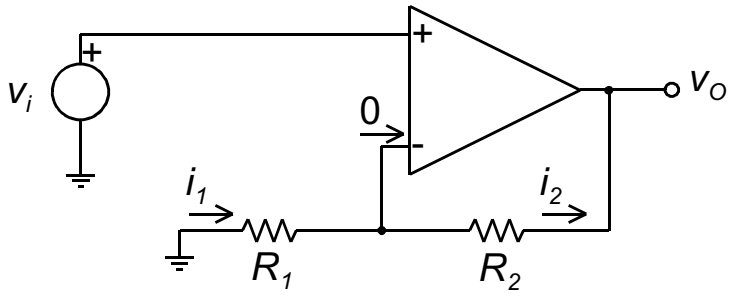

Fig. 46. Noninverting amplifier circuit.

Voltage Gain

This time our rules of operation and a voltage divider equation lead to:

$$v_i = v_+ = v_- = \frac{R_1}{R_1 + R_2} v_o \tag{39}$$

from which:

$$v_o = \frac{R_1 + R_2}{R_1} v_i = \left(1 + \frac{R_2}{R_1}\right) v_i \quad \Rightarrow \quad A_v = 1 + \frac{R_2}{R_1} \tag{40}$$

Input and Output Resistance

The source is connected directly to the ideal op amp, so:

$$R_{in} = R_i = \infty \tag{41}$$

A load "sees" the same ideal Thevenin resistance as in the inverting case:

$$R_O = 0 \tag{42}$$

Op Amp Circuits - The Voltage Follower

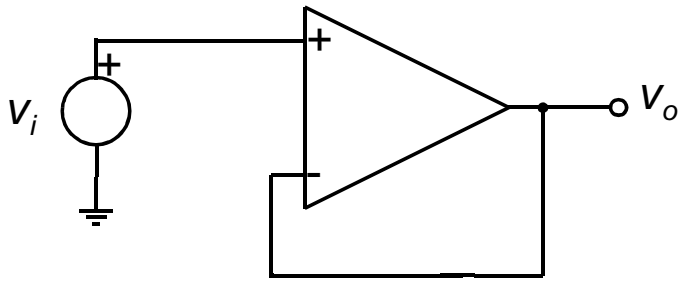

Fig. 47. The voltage follower.

Voltage Gain

This one is easy:

$$v_i = v_+ = v_- = v_o \quad \Rightarrow \quad A_v = 1 \tag{43}$$

i.e., the output voltage *follows* the input voltage.

Input and Output Resistance

By inspection, we should see that these values are the same as for the noninverting amplifier . . .

$$R_{in} = \infty \qquad \text{and} \qquad R_O = 0 \tag{44}$$

In fact, the follower is just a special case of the noninverting amplifier, with $R_1 = \infty$ and $R_2 = 0$*!!!*

Op Amp Circuits - The Inverting Summer

This is a variation of the inverting amplifier:

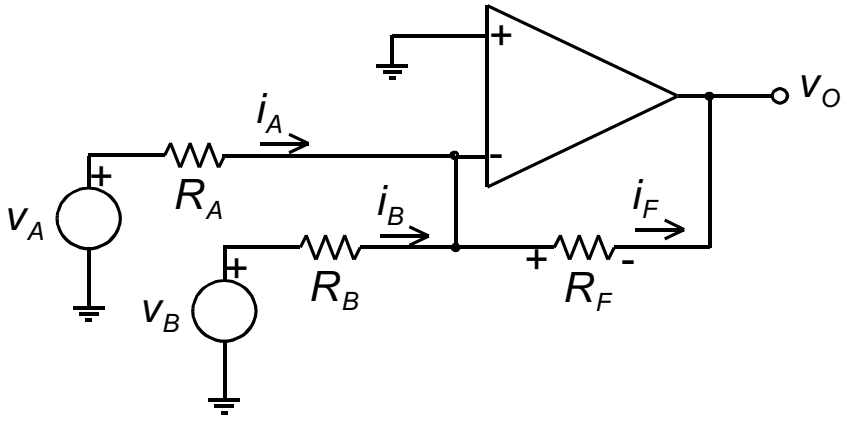

Fig. 48. The inverting summer.

Voltage Gain

We could use the superposition approach as we did for the standard inverter, but with three sources the equations become unnecessarily complicated . . . so let's try this instead . . .

Recall . . . v_O takes on the value that causes $v_- = v_+ = 0$ . . .

So the voltage across R_A is v_A and the voltage across R_B is v_B:

$$i_A = \frac{v_A}{R_A} \qquad \text{and} \qquad i_B = \frac{v_B}{R_B} \tag{45}$$

Because the current into the op amp is zero:

$$i_F = i_A + i_B \quad \text{and} \quad v_{R_F} = R_F\left(i_A + i_B\right) = R_F\left(\frac{v_A}{R_A} + \frac{v_B}{R_B}\right) \tag{46}$$

Finally, the voltage rise to v_O equals the drop across R_F:

$$v_O = -\left(\frac{R_F}{R_A}v_A + \frac{R_F}{R_B}v_B\right) \tag{47}$$

Op Amp Circuits - Another Inverting Amplifier

If we want very large gains with the standard inverting amplifier of Fig. 44, one of the resistors will be unacceptably large or unacceptably small . . .

We solve this problem with the following circuit:

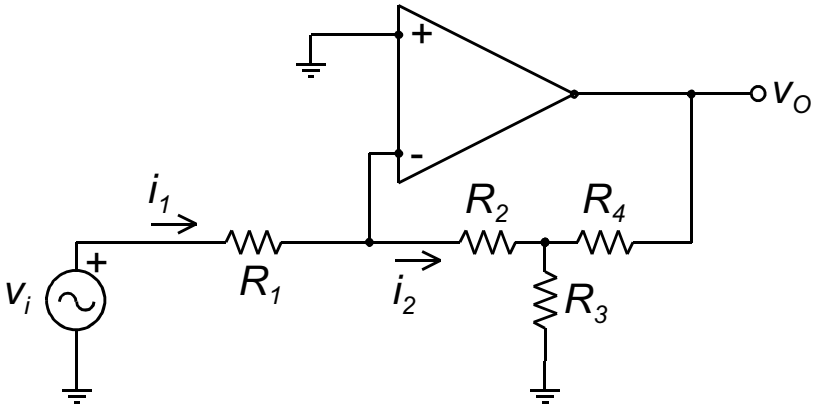

Fig. 49. An inverting amplifier with a resistive *T*-network for the feedback element.

Voltage Gain

One common approach to a solution begins with a KCL equation at the R_2 - R_3 - R_4 junction . . .

. . . we'll use the superposition & voltage divider approach, *after* we apply some network reduction techniques.

Notice that R_3, R_4 and the op amp output voltage source can be replaced with a Thevenin equivalent:

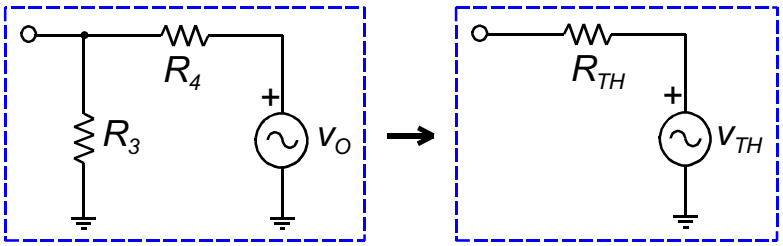

Fig. 50. Replacing part of the original circuit with a Thevenin equivalent

The values of the Thevenin elements in Fig. 50 are:

$$v_{TH} = \frac{R_3}{R_3 + R_4} v_O \qquad \text{and} \qquad R_{TH} = R_3 || R_4 \tag{48}$$

With the substitution of Fig. 50 we can simplify the original circuit:

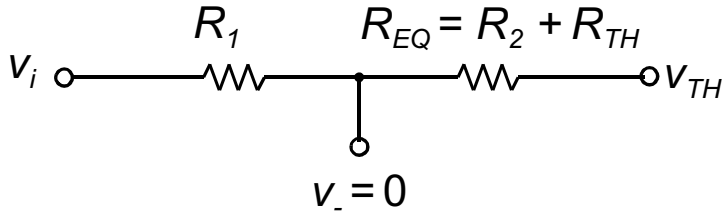

Fig. 51. Equivalent circuit to original amplifier.

Again, v_O, and therefore v_{TH}, takes on the value necessary to make $v_+ - v_- = 0$ . . .

We've now solved this problem *twice* before (the "quick exercise" on p. 4, and the standard inverting amplifier analysis of p. 31):

$$v_{TH} = -\frac{R_{EQ}}{R_1} v_i \tag{49}$$

Substituting for v_{TH} and R_{EQ}, and solving for v_O and A_v:

$$\frac{R_3}{R_3 + R_4} v_O = -\frac{R_2 + (R_3 || R_4)}{R_1} v_i = -\left(\frac{R_2}{R_1} + \frac{R_3 || R_4}{R_1} \right) v_i \tag{50}$$

$$A_v = \frac{v_O}{v_i} = -\left(1 + \frac{R_4}{R_3} \right) \left(\frac{R_2}{R_1} + \frac{R_3 || R_4}{R_1} \right) \tag{51}$$

Op Amp Circuits - Differential Amplifier

The op amp is a differential amplifier to begin with, so *of course* we can build one of these*!!!*

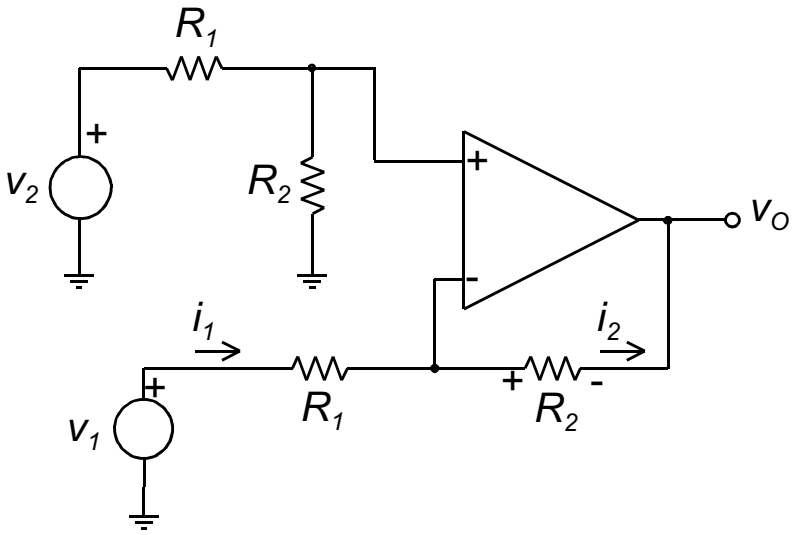

Fig. 52. The differential amplifier.

Voltage Gain

Again, v_O takes on the value required to make $v_+ = v_-$. Thus:

$$v_+ = \frac{R_2}{R_1 + R_2} v_2 = v_- \qquad \textbf{(52)}$$

We can now find the current i_1, which must equal the current i_2:

$$i_1 = \frac{v_1 - v_-}{R_1} = \frac{v_1}{R_1} - \frac{R_2}{R_1(R_1 + R_2)} v_2 = i_2 \qquad \textbf{(53)}$$

Knowing i_2, we can calculate the voltage across R_2. . .

$$v_{R_2} = i_2 R_2 = \frac{R_2}{R_1} v_1 - \frac{R_2 R_2}{R_1(R_1 + R_2)} v_2 \qquad \textbf{(54)}$$

Then we sum voltage rises to the output terminal:

$$v_O = v_+ - v_{R_2} = \frac{R_2}{R_1 + R_2} v_2 - \frac{R_2}{R_1} v_1 + \frac{R_2 R_2}{R_1(R_1 + R_2)} v_2 \qquad \textbf{(55)}$$

Working with just the v_2 terms from eq. (55) . . .

$$\frac{R_2}{R_1+R_2}v_2+\frac{R_2R_2}{R_1(R_1+R_2)}v_2=\frac{R_1R_2}{R_1(R_1+R_2)}v_2+\frac{R_2R_2}{R_1(R_1+R_2)}v_2 \quad \textbf{(56)}$$

$$=\frac{R_1R_2+R_2R_2}{R_1(R_1+R_2)}v_2=\frac{R_2(R_1+R_2)}{R_1(R_1+R_2)}v_2=\frac{R_2}{R_1}v_2 \quad \textbf{(57)}$$

And, finally, returning the resulting term to eq. (55):

$$v_O=-\frac{R_2}{R_1}v_1+\frac{R_2}{R_1}v_2=\frac{R_2}{R_1}(v_2-v_1) \quad \textbf{(58)}$$

So, under the conditions that we can have identical resistors (and an ideal op amp) we truly have a differential amplifier*!!!*

Op Amp Circuits - Integrators and Differentiators

Op amp circuits are not limited to resistive elements!!!

The Integrator

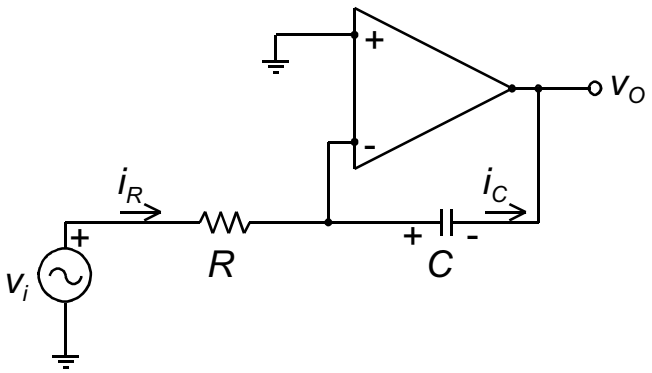

Fig. 53. Op amp integrator.

From our rules and previous experience we know that $v_- = 0$ and $i_R = i_C$, so . . .

$$i_R = \frac{v_i}{R} = i_C \qquad \textbf{(59)}$$

From the *i-v* relationship of a capacitor:

$$v_C = \frac{1}{C}\int_{-\infty}^{t} i_C dt = \frac{1}{C}\int_{0}^{t} i_C dt + v_C(0) \qquad \textbf{(60)}$$

Combining the two previous equations, and recognizing that $v_O = -\,v_C$:

$$v_O = -\frac{1}{C}\int_{0}^{t}\frac{v_i}{R}dt + v_C(0) = -\frac{1}{RC}\int_{0}^{t} v_i dt + v_C(0) \qquad \textbf{(61)}$$

Normally $v_C(0) = 0$ (but not always). Thus the output is the integral of v_i, inverted, and scaled by $1/RC$.

The Differentiator

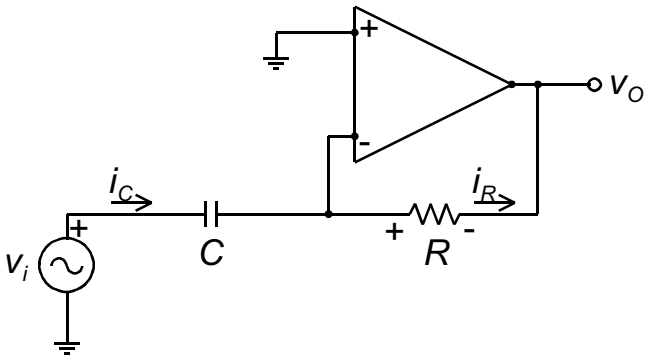

Fig. 54. The op amp differentiator.

This analysis proceeds in the same fashion as the previous analysis.

From our rules and previous experience we know that $v_- = 0$ and $i_C = i_R$ . . .

From the *i-v* relationship of a capacitor:

$$i_C = C\frac{dv_C}{dt} = C\frac{dv_i}{dt} = i_R \qquad \textbf{(62)}$$

Recognizing that $v_O = -v_R$:

$$v_O = -v_R = -i_R R = -RC\frac{dv_i}{dt} \qquad \textbf{(63)}$$

Op Amp Circuits - Designing with Real Op Amps

Resistor Values

Our ideal op amp can supply unlimited current; real ones can't . . .

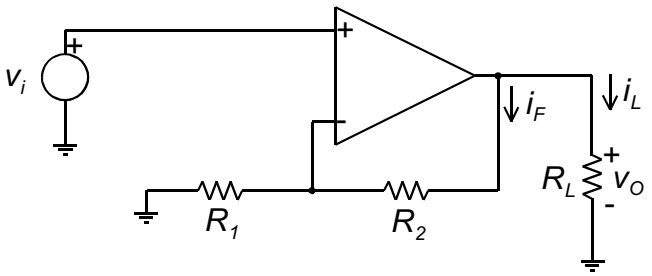

Fig. 55. Noninverting amplifier with load.

To limit $i_F + i_L$ to a reasonable value, we adopt the "rule of thumb" that resistances should be greater than approx. 100 Ω.

Of course this is highly dependent of the type of op amp to be used in a design.

Larger resistances render circuits more susceptible to noise and more susceptible to environmental factors.

To limit these problems we adopt the "rule of thumb" that resistances should be less than approximately 1 MΩ.

Source Resistance and Resistor Tolerances

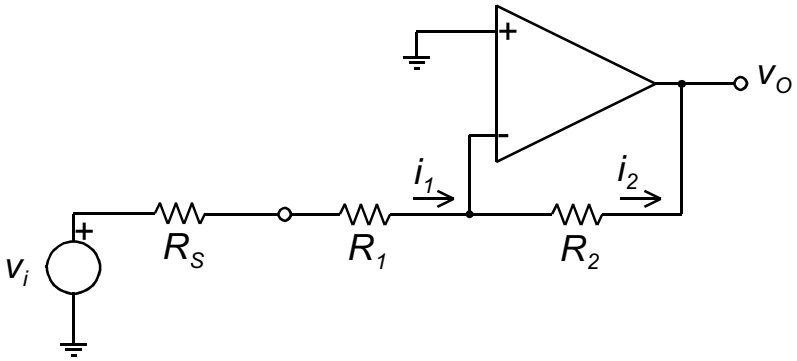

Fig. 56. Inverting amplifier including source resistance.

In some designs R_S will affect desired gain.

Resistor tolerances will also affect gain.

If we wish to ignore source resistance effects, resistances must be much larger than R_S (if possible).

Resistor tolerances must also be selected carefully.

Graphical Solution of Simultaneous Equations

Let's re-visit some 7th-grade algebra . . .we can find the solution of two simultaneous equations by plotting them on the same set of axes.

Here's a trivial example:

$$y = x \qquad \text{and} \qquad y = 4 \tag{64}$$

We plot both equations:

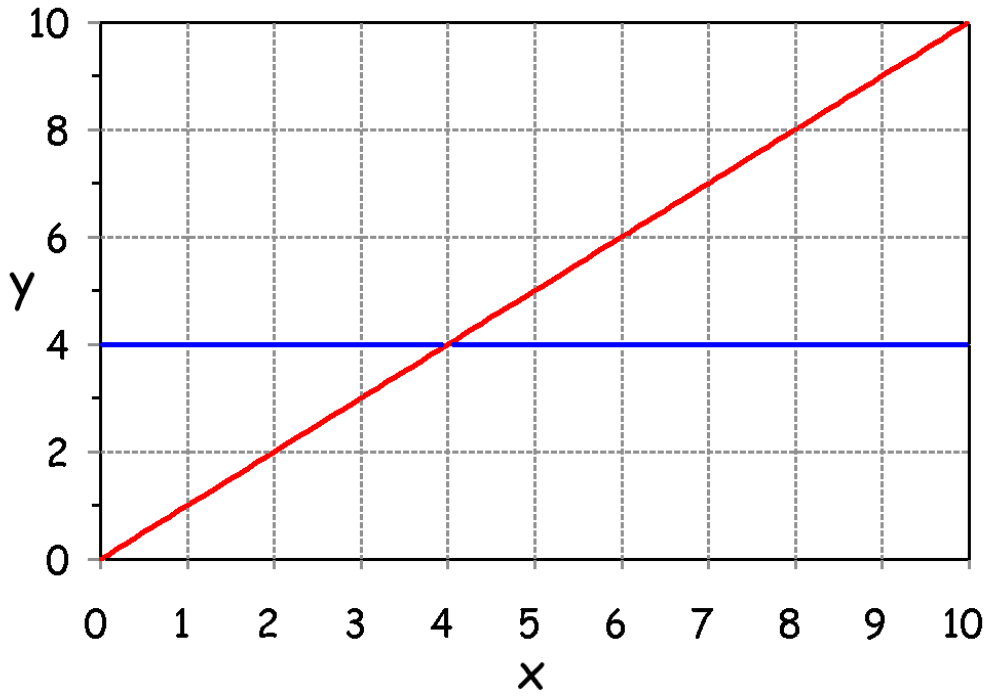

Fig. 57. Simple example of obtaining the solution to simultaneous equations using a graphical method.

Obviously, the solution is where the two plots intersect, at $x = 4$, $y = 4$ . . .

Let's try another one:

$$y = \begin{cases} 0, \text{ for } x < 0 \\ 0.4x^2, \text{ for } x \geq 0 \end{cases} \quad (65)$$

and

$$y = 8 - \frac{4x}{5} \quad (66)$$

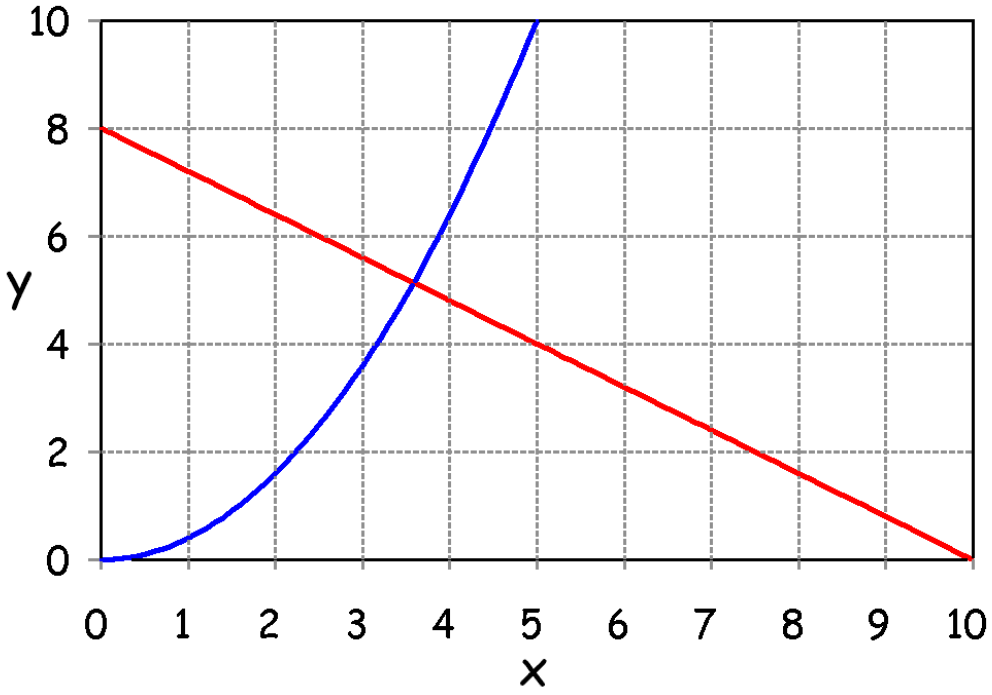

Fig. 58. Another example of graphically finding the solution to simultaneous equations.

Here we see that the solution is approximately at $x = 3.6$, $y = 5.2$.

Note that we lose some accuracy with a graphical method, but, we gain the insight that comes with the "picture."

If we change the previous example slightly, we'll see that we can't arbitrarily neglect the other quadrants:

$$y = 0.4x^2, \text{ for all } x \tag{67}$$

and

$$y = 8 - \frac{4x}{5} \tag{68}$$

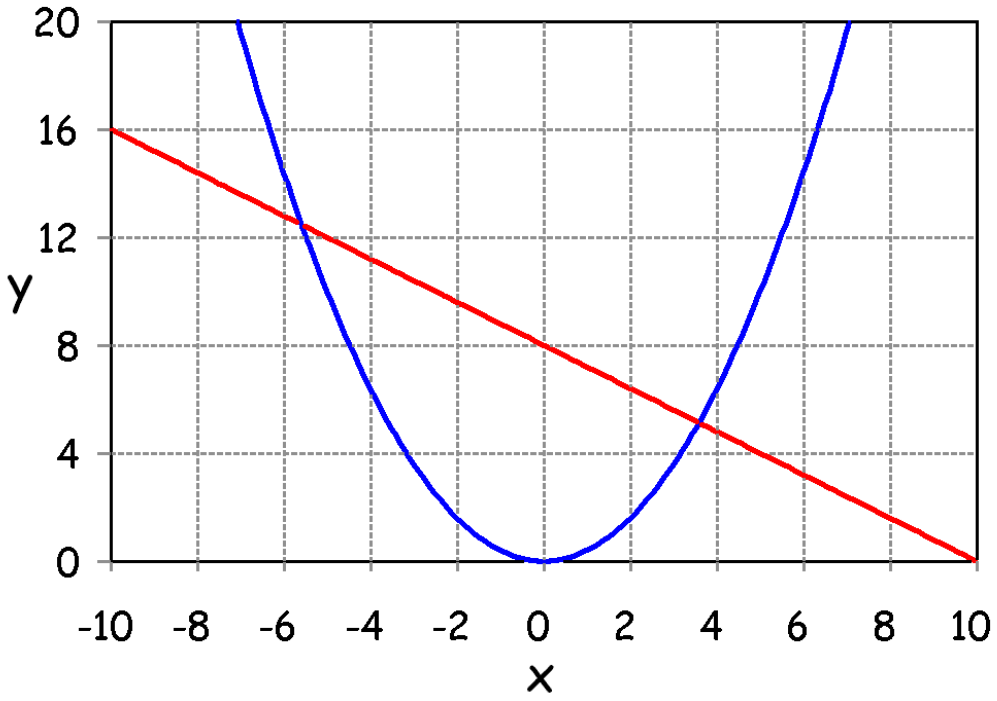

Fig. 59. Graphically finding multiple solutions.

Now we have *two* solutions - the first one we found before, at x = 3.6, y = 5.2 . . . the second solution is at x = -5.5, y = 12.5.

In the pages and weeks to come, we will often use a graphical method to find current and voltage in a circuit.

This technique is especially well-suited to circuits with nonlinear elements.

Diodes

When we “place” *p*-type semiconductor adjacent to *n*-type semiconductor, the result is an element that easily allows current to flow in one direction, but restricts current flow in the opposite direction . . . this is our first nonlinear element:

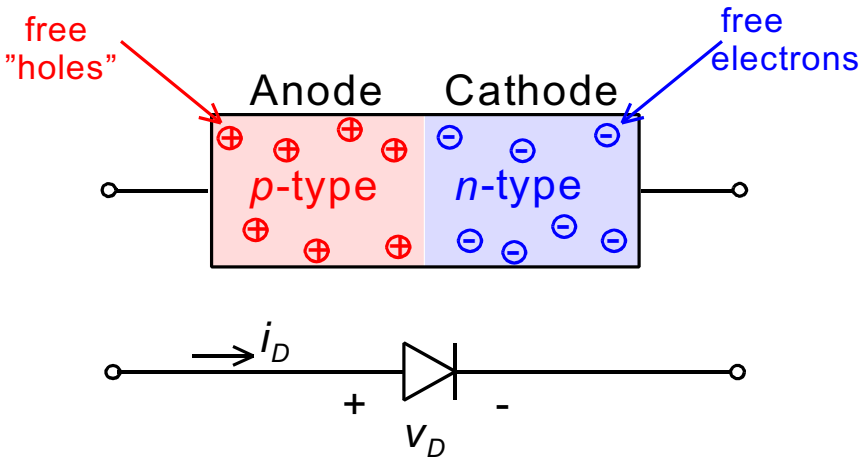

Fig. 60. Simplified physical construction and schematic symbol of a diode.

The free holes “wish” to combine with the free electrons . . .

When we apply an external voltage that facilitates this combination (a *forward* voltage, $v_D > 0$), current flows easily.

When we apply an external voltage that opposes this combination, (a *reverse* voltage, $v_D < 0$), current flow is essentially zero.

Of course, we can apply a large enough reverse voltage to *force* current to flow . . .this is not necessarily destructive.

Thus, the typical diode *i-v* characteristic:

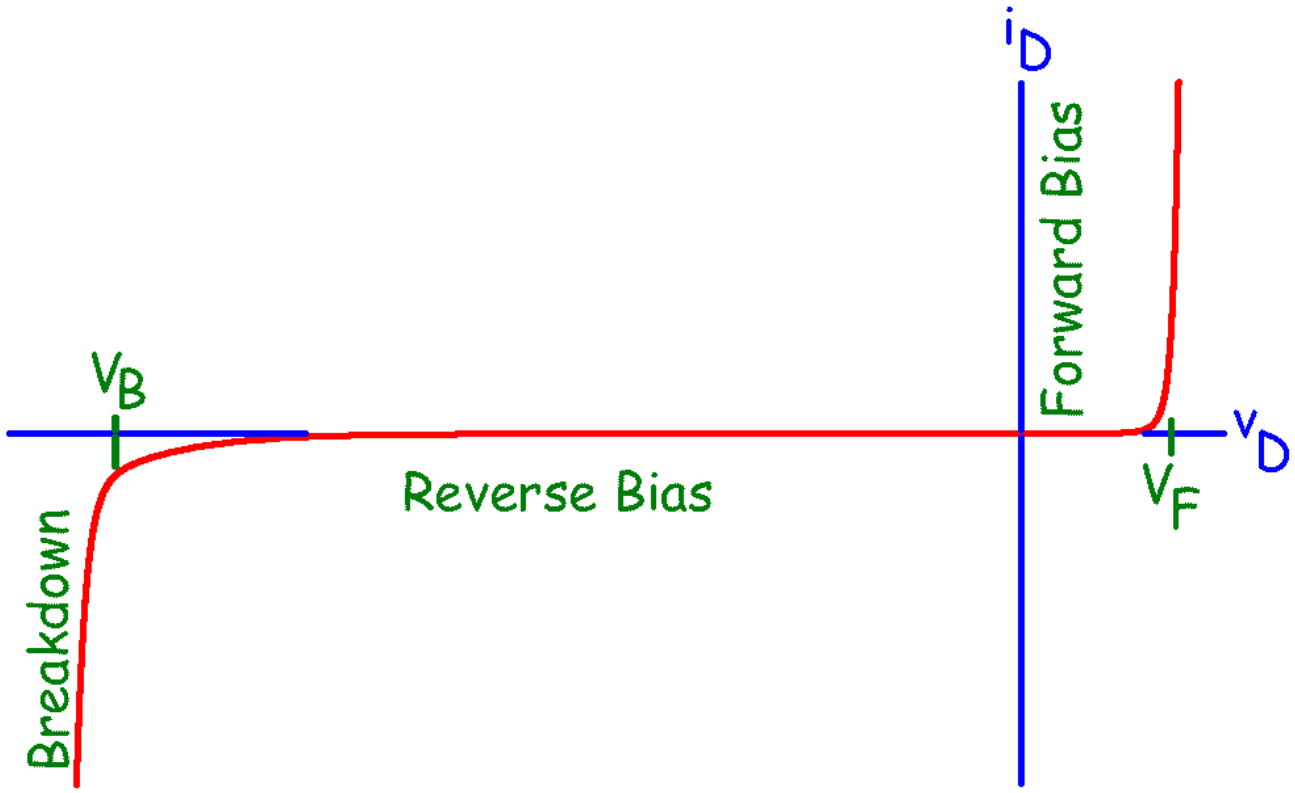

Fig. 61. PSpice-generated *i-v* characteristic for a 1N750 diode showing the various regions of operation.

V_F is called the *forward knee voltage*, or simply, the *forward voltage*.

- It is typically approximately 0.7 V, and has a temperature coefficient of approximately -2 mV/K

V_B is called the *breakdown voltage*.

- It ranges from 3.3 V to kV, and is usually given as a positive value.

Diodes intended for use in the breakdown region are called *zener diodes* (or, less often, *avalanche diodes*).

In the reverse bias region, $|i_D| \approx 1$ nA for low-power ("*signal*") diodes.

Graphical Analysis of Diode Circuits

We can analyze simple diode circuits using the graphical method described previously:

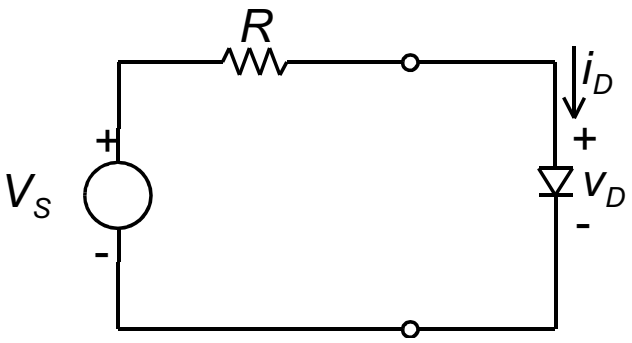

Fig. 62. Example circuit to illustrate graphical diode circuit analysis.

We need two equations to find the two unknowns i_D and v_D.

The first equation is "provided" by the diode *i-v* characteristic.

The second equation comes from *the circuit to which the diode is connected*.

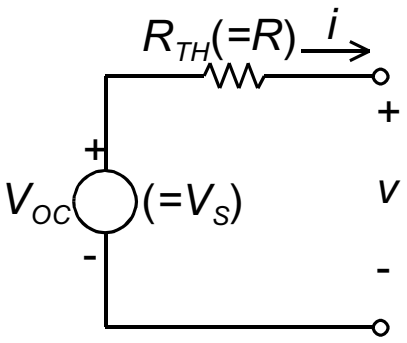

Fig. 63. Thevenin eq. of Fig. 62 identified.

This is just a standard Thevenin equivalent circuit . . .

. . . *and we already know its i-v characteristic* . . . from Fig. 5 and eq. (4) on p. 2:

$$v = V_{OC} - iR_{TH} \quad \text{or} \quad i = I_{SC} - \frac{v}{R_{TH}} \qquad \textbf{(69)}$$

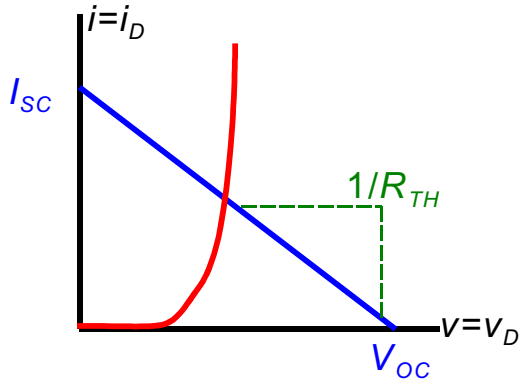

Fig. 64. Graphical solution.

. . . where V_{OC} and I_{SC} are the open-circuit voltage and the short-circuit current, respectively.

A plot of this line is called the *load line*, and the graphical procedure is called *load-line analysis*.

Examples of Load-Line Analysis

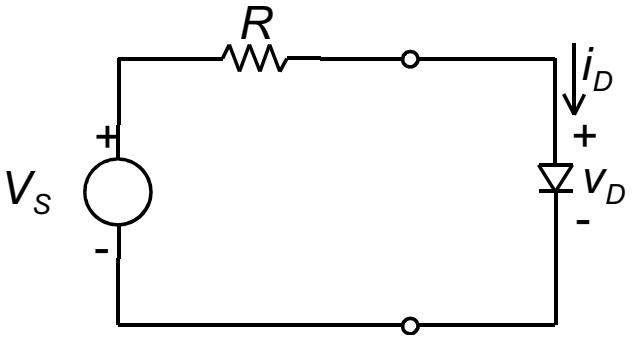

Fig. 65. Example circuit (Fig. 62 repeated).

Case 1: V_S = 2.5 V and R = 125 Ω

Case 2: V_S = 1 V and R = 25 Ω

Case 3: V_S = 10 V and R = 1 kΩ

Case 1: $V_{OC} = V_S = 2.5$ V and $I_{SC} = 2.5$ V / 125 Ω = 20 mA.

We locate the intercepts, and draw the line.

The solution is at $v_D \approx 0.71$ V, $i_D \approx 14.3$ mA

Case 2: $V_{OC} = V_S = 1$ V and $I_{SC} = 1$ V / 25 Ω = 40 mA

I_{SC} is not on scale, so we use the slope: $\frac{1}{25\,\Omega} = \frac{40\text{ mA}}{\text{V}} = \frac{20\text{ mA}}{0.5\text{ V}}$

The solution is at $v_D \approx 0.70$ V, $i_D \approx 12.0$ mA

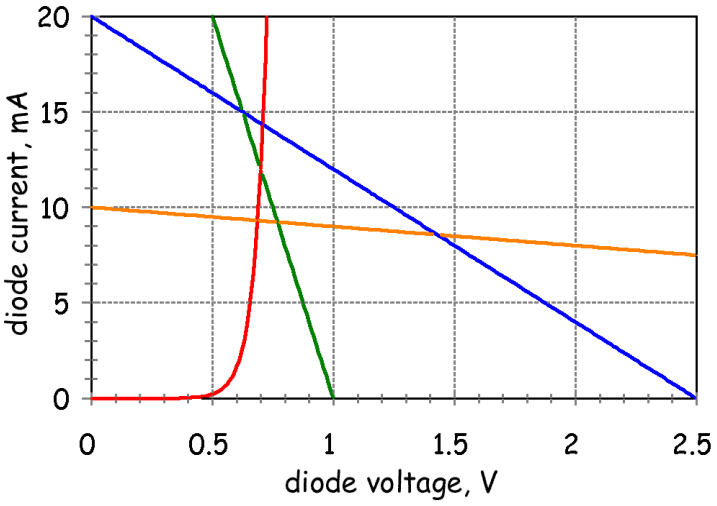

Fig. 66. Example solutions.

Case 3: $V_{OC} = V_S = 10$ V

$I_{SC} = 10$ V / 1 kΩ = 10 mA

V_{OC} not on scale, use slope:

$\frac{1}{1\text{k}\Omega} = \frac{1\text{mA}}{\text{V}} = \frac{2.5\text{ mA}}{2.5\text{ V}}$

The solution is at:

$v_D \approx 0.68$ V, $i_D \approx 9.3$ mA

Diode Models

Graphical solutions provide insight, but neither convenience nor accuracy . . . for accuracy, we need an *equation.*

The Shockley Equation

$$i_D = I_S\left[\exp\left(\frac{v_D}{nV_T}\right)-1\right] \quad \textbf{(70)}$$

or conversely

$$v_D = nV_T \ln\left(\frac{i_D}{I_S}+1\right) \quad \textbf{(71)}$$

where,

I_S is the *saturation current*, $\approx$10 fA for signal diodes

I_S approx. doubles for every 5 K increase in temp.

n is the *emission coefficient*, $1 \le n \le 2$

n = 1 is usually accurate for signal diodes (i_D < 10 mA)

V_T is the *thermal voltage*, $V_T = \dfrac{kT}{q}$ **(72)**

k, Boltzmann's constant, k = 1.38 (10^{-23}) J/K

T. temperature in kelvins

q, charge of an electron, q = 1.6 (10^{-19}) C

Note: at T = 300 K, V_T = 25.9 mV

we'll use V_T = 25 mV as a matter of convenience.

Repeating the two forms of the Shockley equation:

$$i_D = I_S\left[\exp\left(\frac{v_D}{nV_T}\right)-1\right] \quad \textbf{(73)}$$

$$v_D = nV_T \ln\left(\frac{i_D}{I_S}+1\right) \quad \textbf{(74)}$$

Forward Bias Approximation:

For v_D greater than a few tenths of a volt, $\exp(v_D/nV_T) >> 1$, and:

$$i_D \approx I_S \exp\left(\frac{v_D}{nV_T}\right) \quad \textbf{(75)}$$

Reverse Bias Approximation:

For v_D less than a few tenths (negative), $\exp(v_D/nV_T) << 1$, and:

$$i_D \approx -I_S \quad \textbf{(76)}$$

At High Currents:

$$v_D = nV_T \ln\left(\frac{i_D}{I_S}+1\right)+i_D R_S \quad \textbf{(77)}$$

where R_S is the resistance of the bulk semiconductor material, usually between 10 Ω and 100 Ω.

Let's stop and review . . .

- Graphical solutions provide insight, not accuracy.
- The Shockley equation provides accuracy, not convenience.

But we can approximate the diode *i-v* characteristic to provide convenience, and reasonable accuracy in many cases . . .

The Ideal Diode

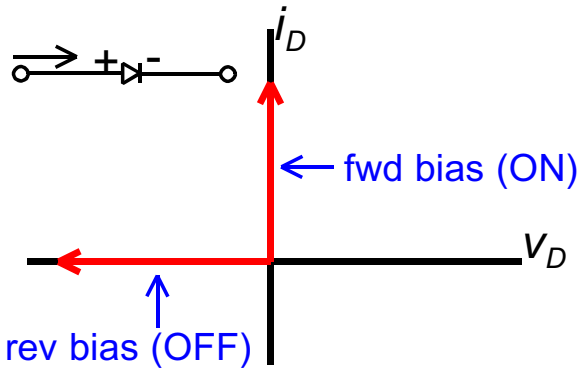

Fig. 67. Ideal diode *i-v* characteristic.

This is the diode we'd *like* to have.

We normally ignore the breakdown region (although we could model this, too).

Both segments are *linear* . . . *if* we knew the correct segment we could use linear analysis*!!!*

In general we *don't* know which line segment is correct . . .so we must *guess* , and then determine if our guess is correct.

If we guess "ON," we know that $v_D = 0$, and that i_D must turn out to be positive if our guess is correct.

If we guess "OFF," we know that $i_D = 0$, and that v_D must turn out to be negative if our guess is correct.

An Ideal Diode Example:

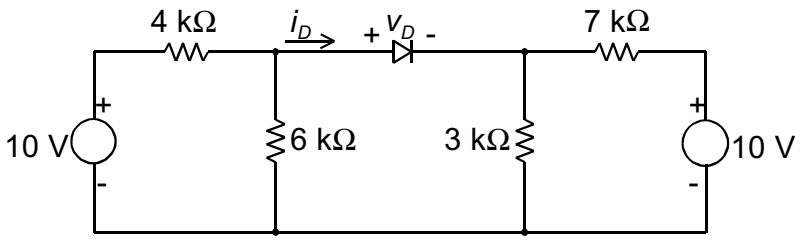

Fig. 68.Circuit for an ideal diode example.

We need first to assume a diode state, i.e., ON or OFF.

We'll arbitrarily choose OFF.

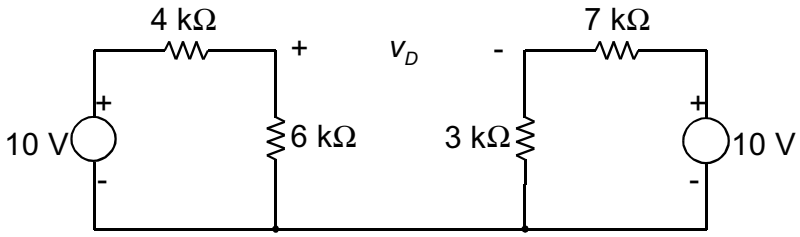

Fig. 69.Equivalent circuit if the diode is OFF.

If OFF, i_D = 0, i.e., the diode is an *open circuit*.

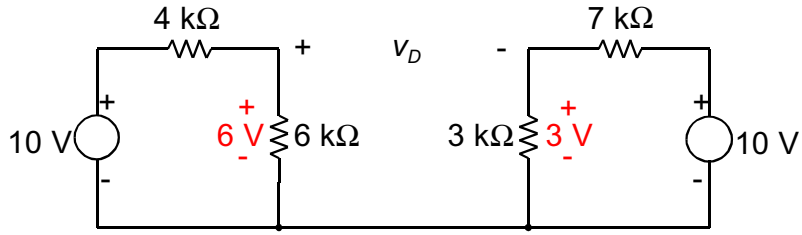

Fig. 70.Calculating v_D for the OFF diode.

We can easily find v_D using voltage division and KVL $\Rightarrow$ v_D = 3 V.

v_D is <u>*not*</u> negative, so diode must be ON.

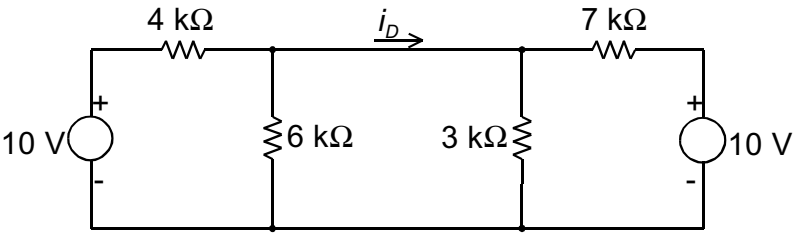

Fig. 71.Equivalent circuit if the diode is ON.

If ON, v_D = 0, i.e., the diode is a *short circuit*.

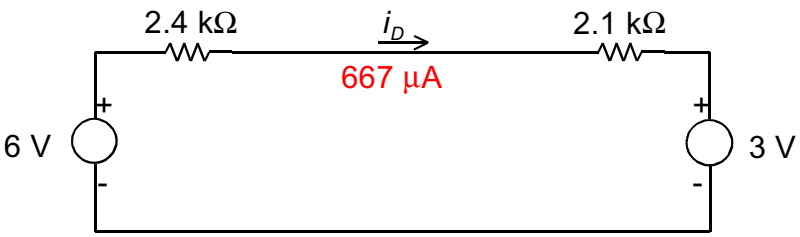

Fig. 72.Calculating i_D for the ON diode.

We can easily find i_D using Thevenin eqs. $\Rightarrow$ i_D = 667 µA.

No contradictions *!!!*

Let's review the techniques, or *rules*, used in analyzing ideal diode circuits. These rules apply even to circuits with multiple diodes:

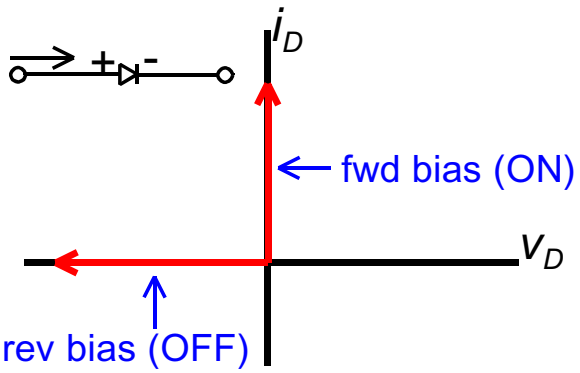

Fig. 73. Ideal diode *i-v* characteristic.
(Fig. 67 repeated)

1. Make assumptions about diode states.

2. Calculate v_D for all OFF diodes, and i_D for all ON diodes.

3. If *all* OFF diodes have $v_D < 0$, and *all* ON diodes have $i_D > 0$, the initial assumption was correct. If not make new assumption and repeat.

Piecewise-Linear Diode Models

This is a generalization of the ideal diode concept.

Piecewise-linear modeling uses straight line segments to approximate various parts of a nonlinear *i-v* characteristic.

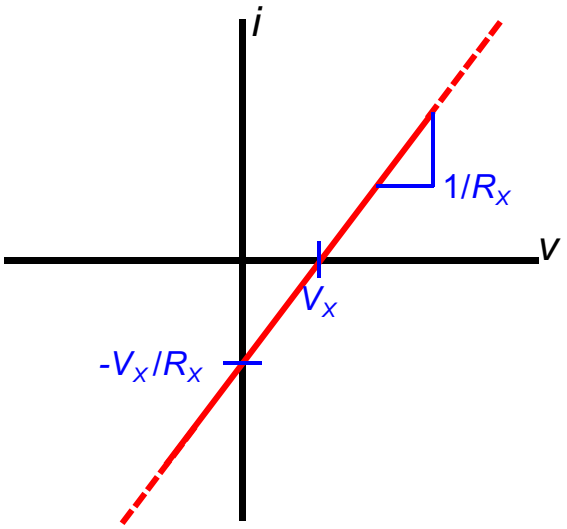

Fig. 74. A piecewise-linear segment.

The line segment at left has the equation:

$$v = V_X + iR_X \qquad \textbf{(78)}$$

The same equation is provided by the following circuit:

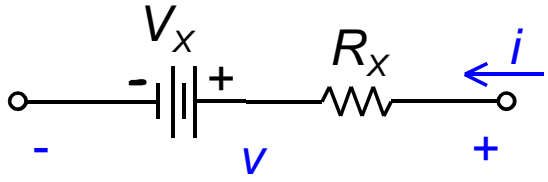

Fig. 75. Circuit producing eq. (?).

Thus, we can use the line segments of Fig. 74 to approximate portions of an element's nonlinear *i-v* characteristic . . .

. . . and use the equivalent circuits of Fig. 75 to represent the element with the approximated characteristic*!!!*

A “complete” piecewise-linear diode model looks like this:

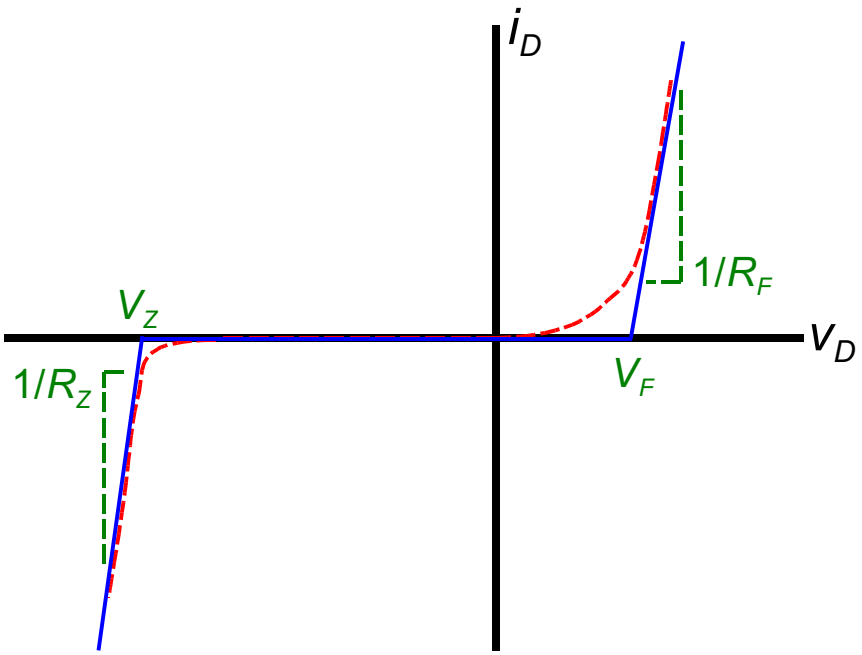

Fig. 76. A diode *i-v* characteristic (red) and its piecewise-linear equivalent (blue).

- In the *forward bias* region . . .

  . . . the approximating segment is characterized by the *forward voltage,* V_F, and the *forward resistance,* R_F.

- In the *reverse bias* region . . .

  . . . the approximating segment is characterized by $i_D = 0$, i.e., an open circuit.

- In the *breakdown* region . . .

  . . . the approximating segment is characterized by the *zener voltage,* V_Z , (or *breakdown voltage,* V_B) and the *zener resistance,* R_Z.

A Piecewise-Linear Diode Example:

We have modeled a diode using piecewise-linear segments with:

$$V_F = 0.5\text{ V},\ R_F = 10\ \Omega,\quad \text{and}\quad V_Z = 7.5\ \text{V},\ R_Z = 2.5\ \Omega$$

Let us find i_D and v_D in the following circuit:

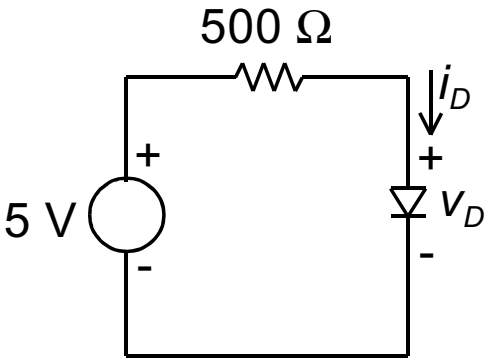

Fig. 77. Circuit for piecewise-linear example.

We need to "guess" a line segment.

Because the 5 V source would tend to force current to flow in a clockwise direction, and that is the direction of forward diode current, let us choose the forward bias region first.

Our equivalent circuit for the forward bias region is shown at left. We have

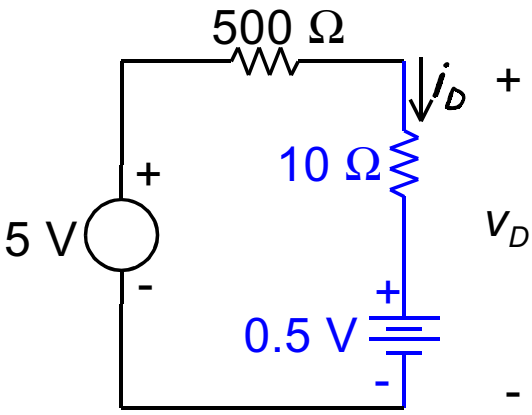

Fig. 78. Equivalent circuit in forward bias region.

$$i_D = \frac{5\text{ V} - 0.5\text{ V}}{500\ \Omega + 10\ \Omega} = 8.82\text{ mA} \qquad \textbf{(79)}$$

and

$$v_D = 0.5\text{ V} + (8.82\text{ mA})(10\ \Omega) = 0.588\text{ V} \qquad \textbf{(80)}$$

This solution does not contradict our forward bias assumption, so it must be the correct one for our model.

Other Piecewise-Linear Models

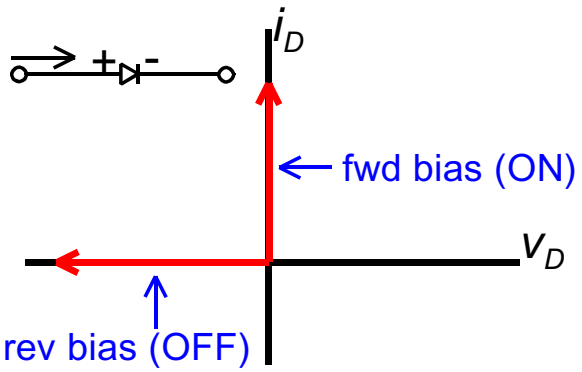

Fig. 79. Ideal diode *i-v* characteristic. (Fig. 67 repeated)

Our *ideal diode model* is a special case . . .

. . . it has $V_F = 0$, $R_F = 0$ in the forward bias region . . .

. . . it doesn't have a breakdown region.

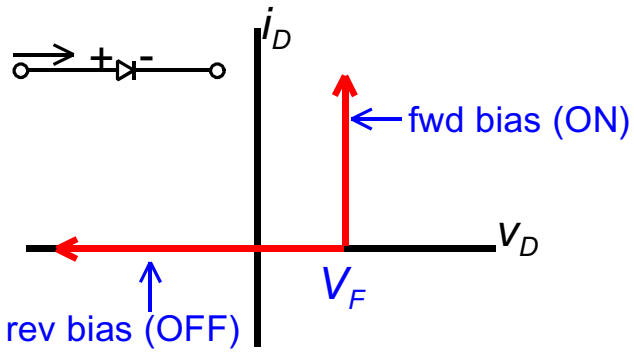

Fig. 80. *I-v* characteristic of constant voltage drop diode model.

The *constant voltage drop diode model* is also a special case . . .

. . . it has $R_F = 0$ in the forward bias region . . .

. . . V_F usually 0.6 to 0.7 V . . .

. . . it doesn't have a breakdown region

Diode Applications - The Zener Diode Voltage Regulator

Introduction

This application uses diodes in the breakdown region . . .

For V_Z < 6 V the physical breakdown phenomenon is called *zener breakdown* (high electric field). It has a negative temperature coefficient.

For V_Z > 6 V the mechanism is called *avalanche breakdown* (high kinetic energy). It has a positive temperature coefficient.

For $V_Z \approx 6$ V the breakdown voltage has nearly *zero* temperature coefficient, and a nearly vertical *i-v* char. in breakdown region, i.e., a very small R_Z.

These circuits can produce nearly constant voltages when used with voltage supplies that have variable or unpredictable output voltages. Hence, they are called *voltage regulators*.

Load-Line Analysis of Zener Regulators

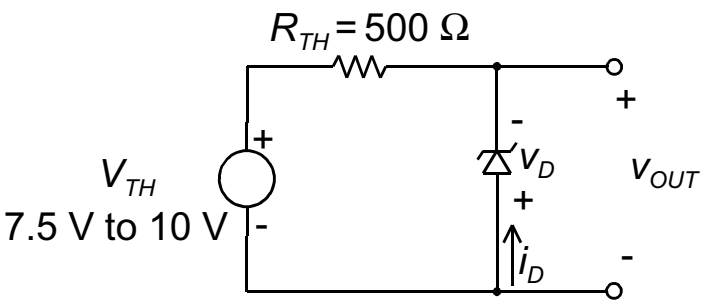

Fig. 81. Thevenin equivalent source with unpredictable voltage and zener diode.

Note: when intended for use as a *zener diode*, the schematic symbol changes slightly . . .

With V_{TH} positive, zener current can flow *only* if the zener is in the breakdown region . . .

We can use load line analysis with the zener diode *i-v* characteristic to examine the behavior of this circuit.

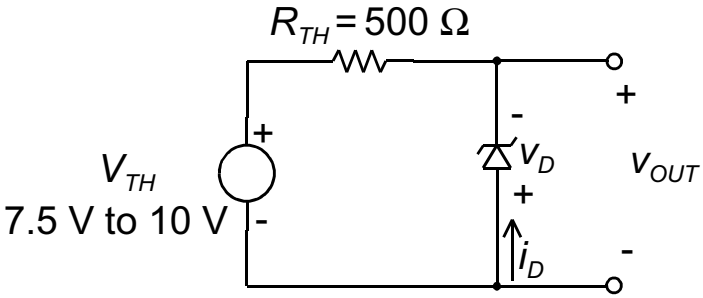

Fig. 82. Thevenin equivalent source with unpredictable voltage and zener diode. (Fig. 81 repeated)

Note that $v_{OUT} = -v_D$. Fig. 83 below shows the graphical construction.

Because the zener is upside-down the Thevenin equivalent load line is in the 3rd quadrant of the diode characteristic.

As V_{TH} varies from 7.5 V to 10 V, the load line moves from its blue position, to its green position.

As long as the zener remains in breakdown, v_{OUT} remains nearly constant, at ≈4.7 V.

As long as the minimum V_{TH} is somewhat greater than V_Z (in this case V_Z = 4.7 V) the zener remains in the breakdown region.

If we're willing to give up some output voltage <u>magnitude</u>, in return we get a <u>very</u> constant output voltage.

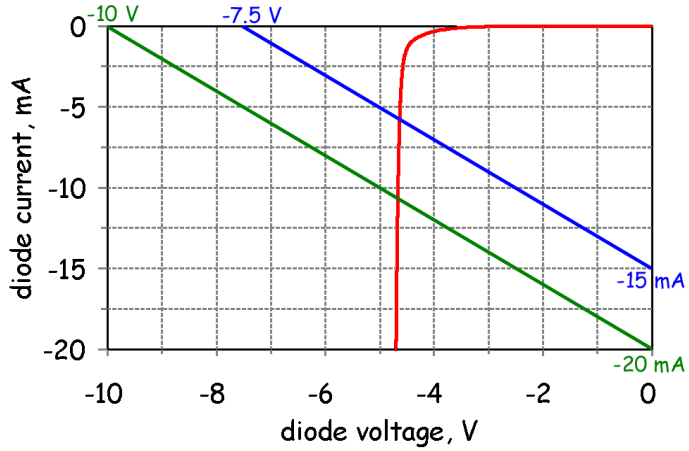

Fig. 83. 1N750 zener (V_Z = 4.7 V) *i-v* characteristic in breakdown region, with load lines from source voltage extremes.

This is an example of a *zener diode voltage regulator* providing *<u>line voltage regulation</u>* . . . V_{TH} is called the *line voltage*.

Numerical Analysis of Zener Regulators

To describe line voltage regulation numerically we use linear circuit analysis with a piecewise-linear model for the diode.

To obtain the model we draw a tangent to the curve in the vicinity of the operating point:

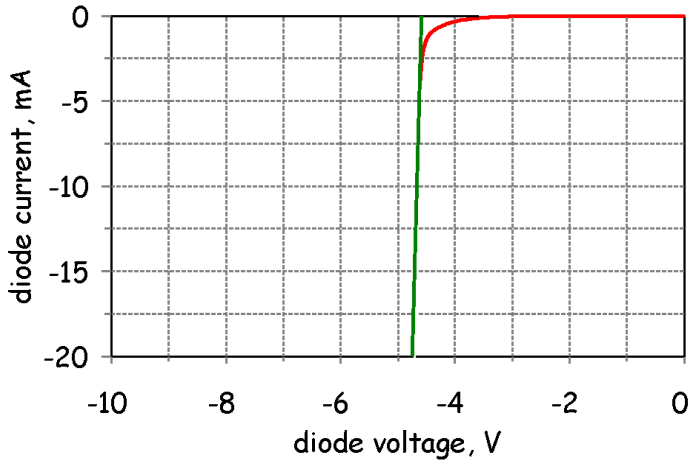

Fig. 84. Zener *i-v* characteristic of Fig. 83 with piecewise-linear segment.

From the intercept and slope of the piecewise-linear segment we obtain V_Z = 4.6 V and R_Z = 8 Ω. Our circuit model then becomes:

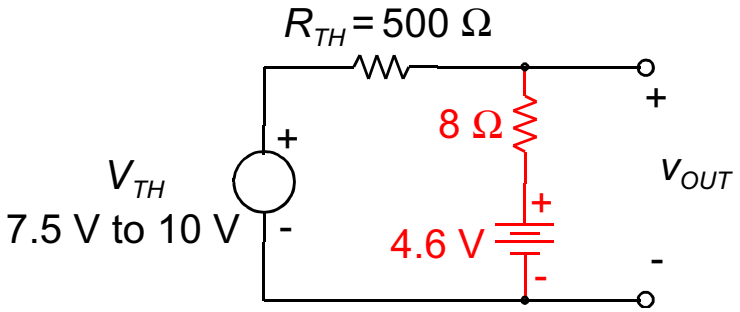

Fig. 85. Regulator circuit of Fig. 81 with piecewise-linear model replacing the diode.

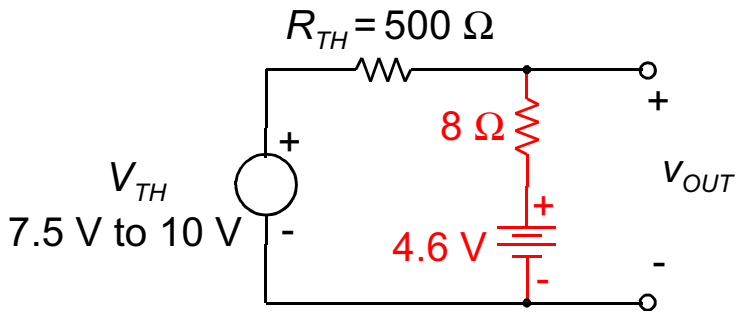

Fig. 86. Regulator with diode model (Fig. 85 repeated).

Important: The model above is valid *only* if zener is in breakdown region *!!!*

Circuit Analysis:

The 500 Ω and 8 Ω resistors are in series, forming a voltage divider.

For V_{TH} = 7.5 V:

$$V_{8\,\Omega} = \frac{8\ \Omega}{500\ \Omega + 8\ \Omega}(7.5\ \text{V} - 4.6\ \text{V}) = 45.67\ \text{mV} \quad \textbf{(81)}$$

$$V_O = 4.6\ \text{V} + 45.67\ \text{mV} = 4.64567\ \text{V} \quad \textbf{(82)}$$

For V_{TH} = 10 V:

$$V_{8\,\Omega} = \frac{8\ \Omega}{500\ \Omega + 8\ \Omega}(10\ \text{V} - 4.6\ \text{V}) = 85.04\ \text{V} \quad \textbf{(83)}$$

$$V_O = 4.6\ \text{V} + 85.04\ \text{mV} = 4.68504\ \text{V} \quad \textbf{(84)}$$

Thus, for a 2.5 V change in the line voltage, *the output voltage change is only 39.4 mV !!!*

Zener Regulators with Attached Load

Now let's add a load to our regulator circuit . . .

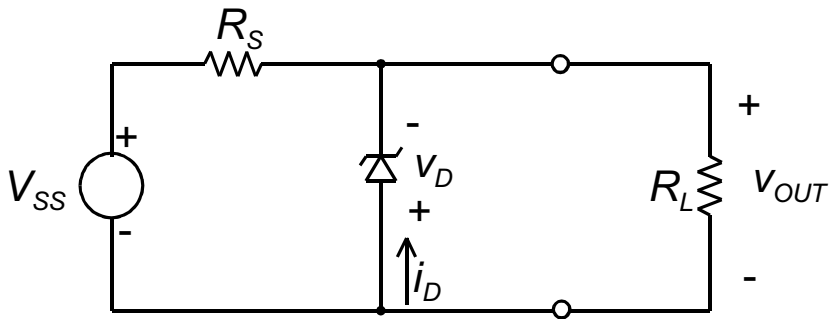

Fig. 87. Zener regulator with load.

Only the zener is nonlinear, so we approach this problem by finding the Thevenin equivalent seen by the diode:

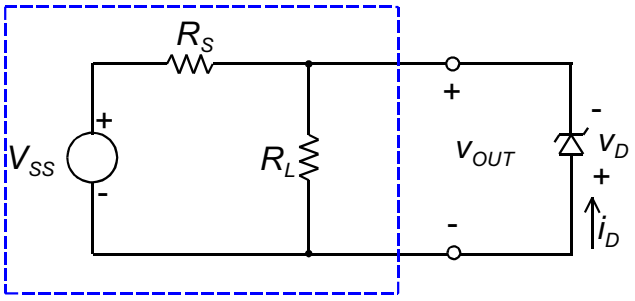

Fig. 88. Regulator drawn with zener and load in reversed positions.

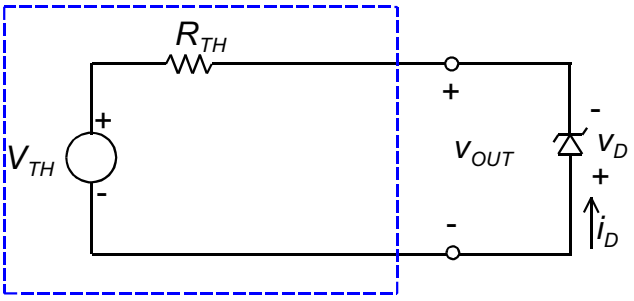

Fig. 89. Regulator of Fig. 87 with V_{SS}, R_S, and R_L replaced by Thevenin eq.

The resulting circuit is topologically identical to the circuit we just analyzed*!!!*

Different loads will result in different values for V_{TH} and R_{TH}, but the analysis procedure remains the same*!!!*

Example - Graphical Analysis of Loaded Regulator

Let's examine graphically the behavior of a loaded zener regulator.

Let V_{SS} = 10 V, R_S = 500 Ω and,

(a) R_L = 10 kΩ (b) R_L = 1 kΩ (c) R_L = 100 Ω

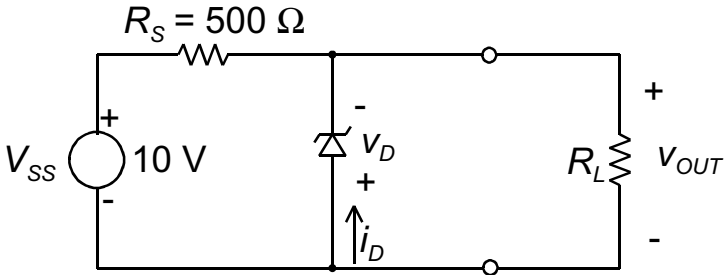

Fig. 90. Example of loaded zener regulator for graphical analysis.

We find the load lines in each case by calculating the open-circuit (Thevenin) voltage and the short-circuit current:

(a)

$$V_{OC} = V_{TH} = \frac{10\ \text{k}\Omega}{10\ \text{k}\Omega + 500\ \Omega} 10\ \text{V} = 9.52\ \text{V} \quad (85)$$

$$I_{SC} = \frac{V_{SS}}{R_S} = \frac{10\ \text{V}}{500\ \Omega} = 20\ \text{mA} \quad (86)$$

(b)

$$V_{OC} = V_{TH} = \frac{1\ \text{k}\Omega}{1\ \text{k}\Omega + 500\ \Omega} 10\ \text{V} = 6.67\ \text{V} \quad (87)$$

$$I_{SC} = \frac{V_{SS}}{R_S} = \frac{10\ \text{V}}{500\ \Omega} = 20\ \text{mA} \quad (88)$$

(c)

$$V_{OC} = V_{TH} = \frac{100\ \Omega}{100\ \Omega + 500\ \Omega} 10\ \text{V} = 1.67\ \text{V} \quad (89)$$

$$I_{SC} = \frac{V_{SS}}{R_S} = \frac{10\ \text{V}}{500\ \Omega} = 20\ \text{mA} \quad (90)$$

The three load lines are plotted on the zener characteristic below:

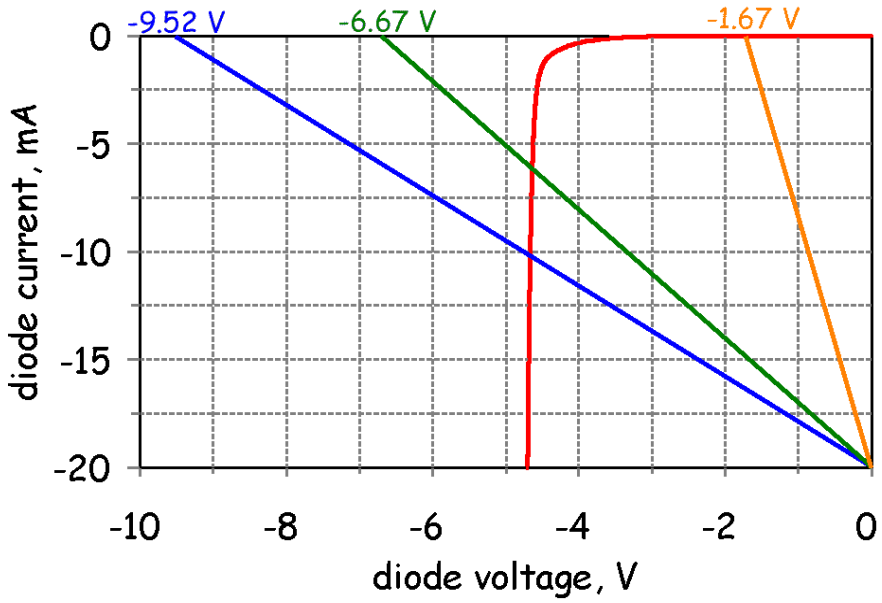

Fig. 91. Load line analysis for the loaded zener regulator.

As long as R_L (and therefore V_{TH}) is large enough so that the zener remains in breakdown, *the output voltage is nearly constant !!!*

This is an example of a zener diode voltage regulator providing *load voltage regulation* (or simply, *load regulation*).

Diode Applications - The Half-Wave Rectifier

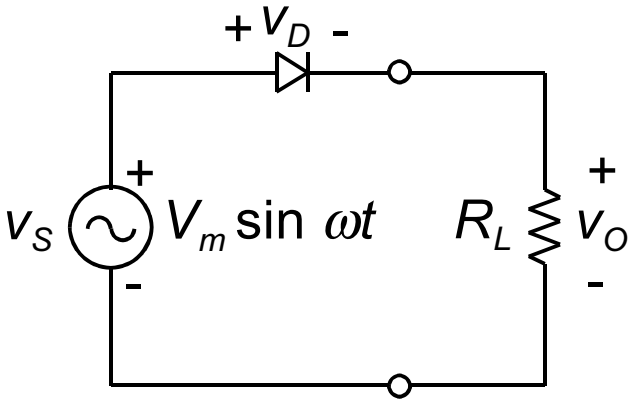

Fig. 92. The half-wave rectifier circuit.

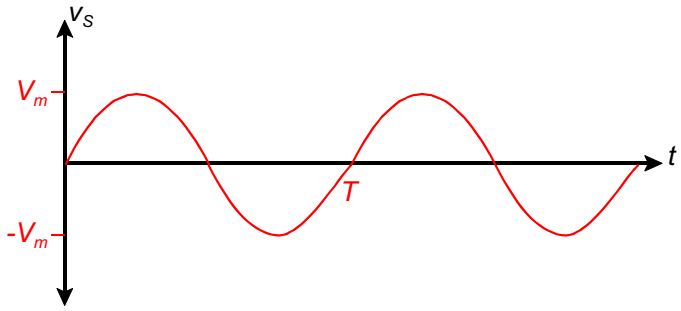

Fig. 93. Waveform of voltage source.

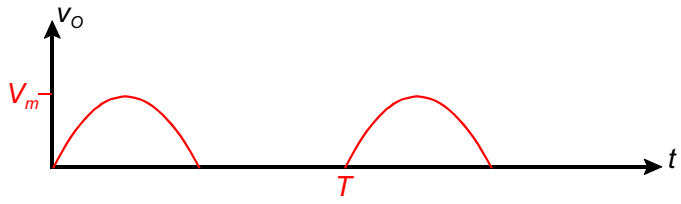

Fig. 94. Output voltage waveform.

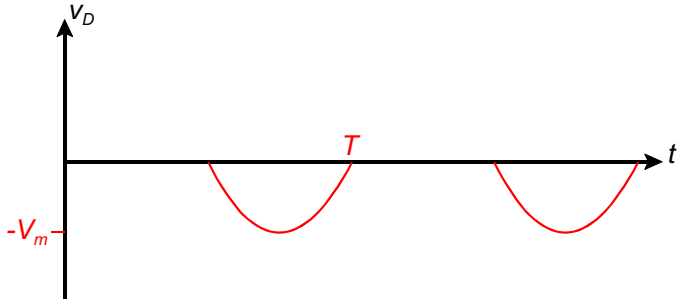

Fig. 95. Diode voltage waveform.

Introduction

This diode application changes ac into dc. The voltage source is most often a sinusoid (but can be anything).

We'll assume the diode is ideal for our analysis.

During *positive* half-cycle . . .

. . . diode conducts ("ON")

. . . $v_D = 0$

. . . $v_O = v_S$

During *negative* half-cycle . . .

. . . diode "OFF"

. . . $i_D = 0$, $v_O = 0$

. . . $v_D = v_S$

Peak Inverse Voltage, PIV:

Another term for breakdown voltage rating . . .

. . . in this circuit, the diode PIV rating must be > V_m.

A Typical Battery Charging Circuit

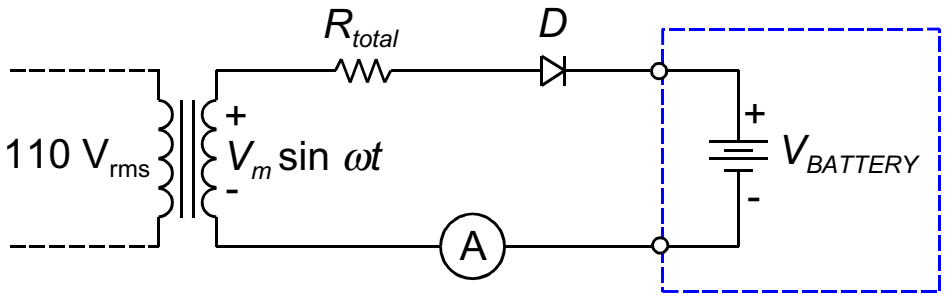

Fig. 96. A circuit typical of most battery chargers.

In the figure above . . .

. . . $V_{BATTERY}$ represents the battery to be charged . . .

. . . R_{total} includes all resistance (wiring, diode, battery, etc.) reflected to the transformer secondary winding.

Charging current flows only when V_m sin ωt > $V_{BATTERY}$ . . .

. . . inertia of meter movement allows indication of average current.

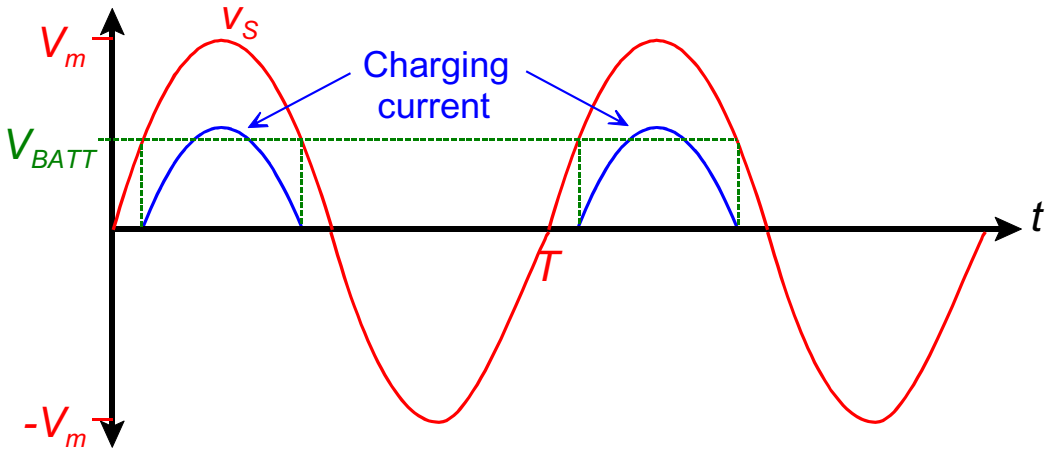

Fig. 97. Battery charger waveforms.
Here v_S represents the transformer secondary voltage, and V_{BATT} represents the battery voltage.

The Filtered Half-Wave Rectifier

Also called a *peak rectifier*, a half-wave rectifier with a *smoothing capacitor*, or a half-wave rectifier with a *capacitor-input filter*.

We create it by placing a capacitor in parallel with the rectifier load (creating a low-pass filter):

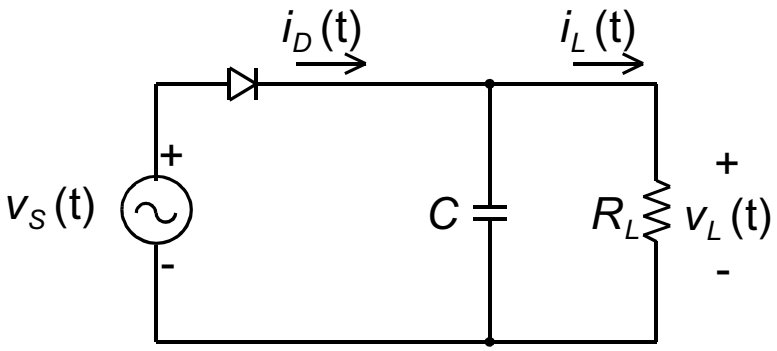

Fig. 98. Filtered half-wave rectifier.

Analysis of this circuit with a nonlinear element is *very* difficult . . .

. . . so we will use the ideal diode model.

A lot happens in this circuit!!! Let's look at the load voltage:

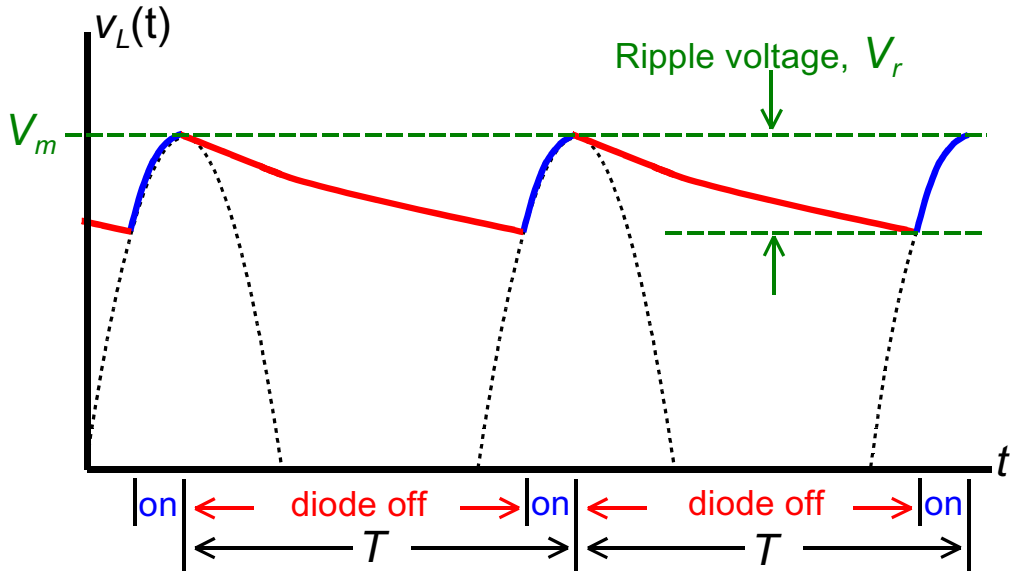

Fig. 99. Load voltage waveform in the filtered half-wave rectifier.

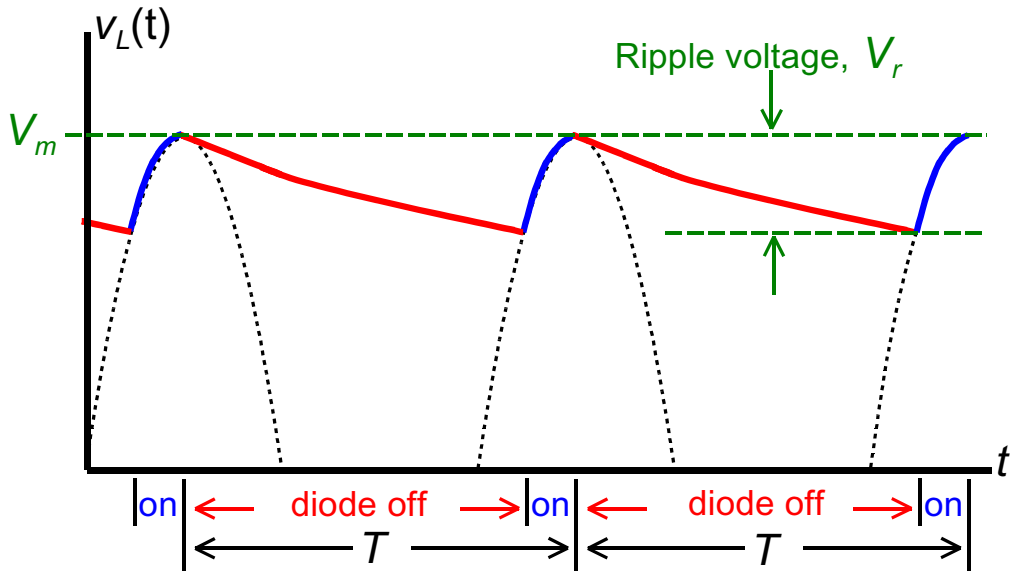

Fig. 100. Load voltage waveform (Fig. 99 repeated).

We let v_S(t) = V_m sin ωt . . . and assume steady-state . . .

1. When $v_S > v_L$ (shown in blue), the diode is on, and the voltage source charges the capacitor.

(Because the diode and source are ideal, v_S can only be infinitesimally greater than v_L)

2. When $v_S < v_L$ (shown in red), the diode is off, and C discharges exponentially through R_L .

3. We define *peak-to-peak ripple voltage*, V_r, as the total change in v_L over one cycle.

4. In practice, V_r is *much* smaller than shown here, typically being 1% to 0.01% of V_m (e.g., a few mV). This means that:

(a) *the load voltage is essentially "pure" dc*

(b) *the diode is off for almost the entire period, T !!!*

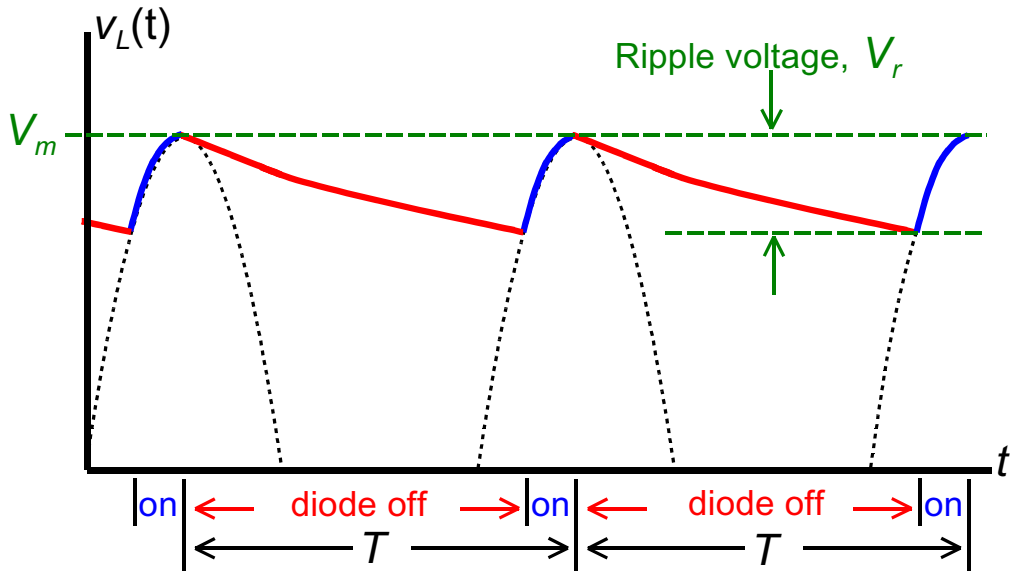

Fig. 101. Load voltage waveform (Fig. 99 repeated).

Relating Capacitance to Ripple Voltage

Because the diode is off for nearly the entire period, T, the capacitor must supply the "*dc*" load current during this interval.

The *charge* taken from the capacitor in this interval is:

$$Q \approx I_L T \approx \frac{V_m}{R_L} T = \frac{V_m}{f R_L} \tag{91}$$

The capacitor voltage decreases by V_r in this interval, which requires a decrease in the charge stored in the capacitor:

$$Q = V_r C \tag{92}$$

Equating these equations and solving for C gives us a design equation *that is valid only for small* V_r:

$$V_r C = \frac{V_m}{f R_L} \quad \Rightarrow \quad C = \frac{V_m}{V_r f R_L} \tag{93}$$

Because *all* of the charge supplied to the load must come from the source only when the diode is ON, $i_{D\ PEAK}$ can be very large, as illustrated below..

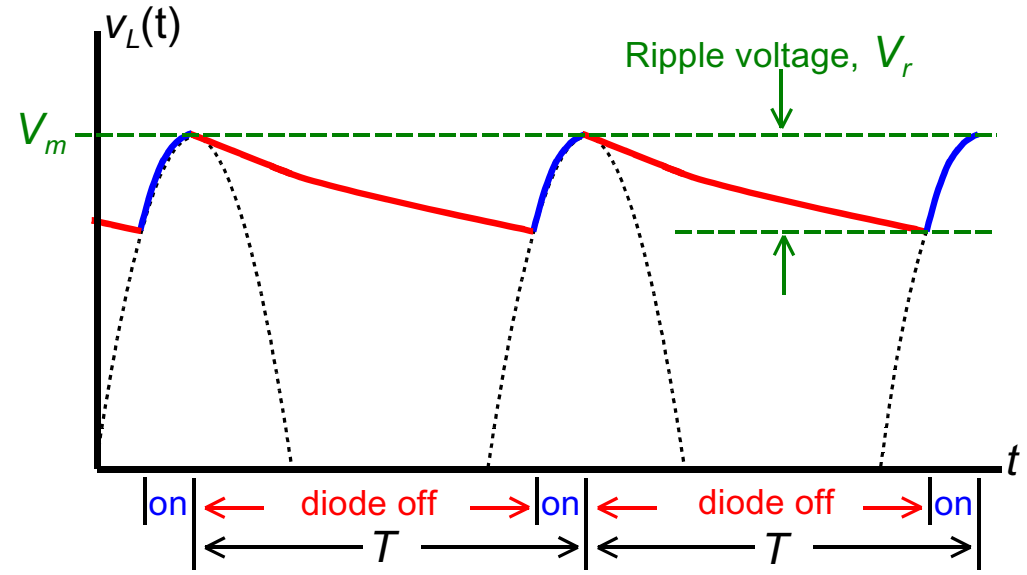

Fig. 102. Load voltage waveform (Fig. 99 repeated).

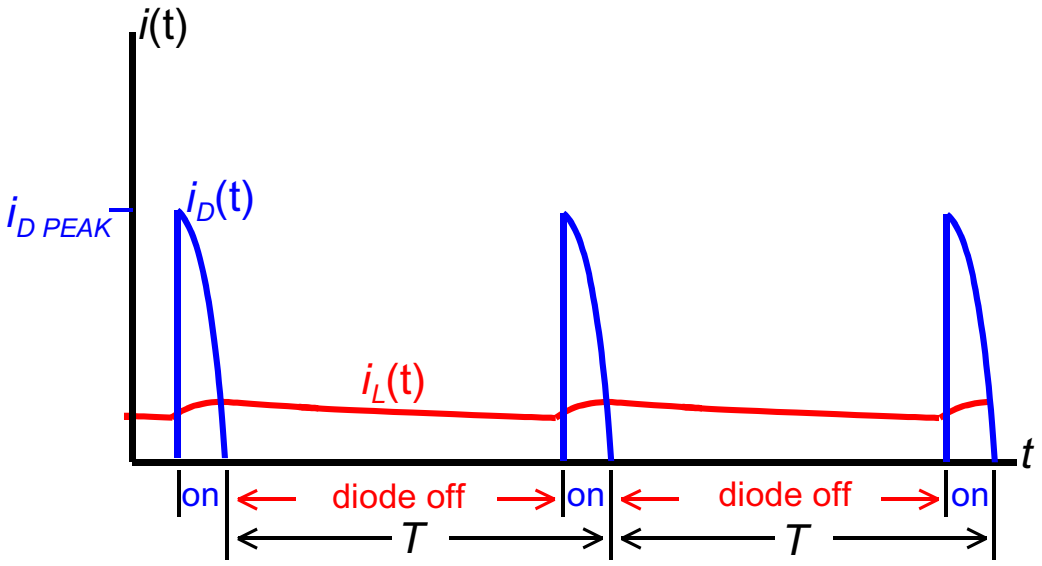

Fig. 103. Current waveforms in filtered half-wave rectifier.

Diode Applications - The Full-Wave Rectifier

The *full-wave rectifier* makes use of a *center-tapped transformer* to effectively create *two* equal input sources:

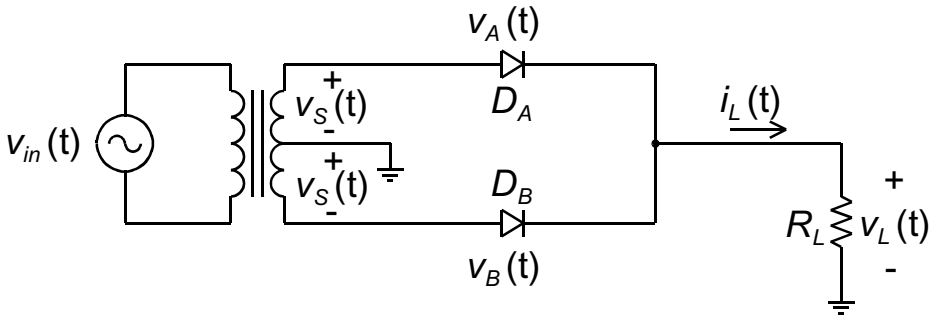

Fig. 104. The full-wave rectifier.

Operation

Note that the upper half of the transformer secondary voltage has its negative reference at ground, while the lower half of the secondary voltage has its positive reference at ground.

1st (Positive) Half-Cycle:

Current flows from upper source, through D_A and R_L, returning to upper source via ground. Any current through D_B would be in reverse direction, thus D_B is off.

2nd (Negative) Half-Cycle:

Current flows from lower source, through D_B and R_L, returning to lower source via ground. Any current through D_A would be in reverse direction, thus D_A is off.

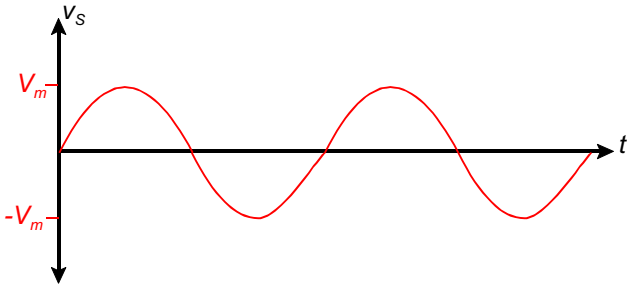

Fig. 105. Voltage across each half of the transformer secondary.

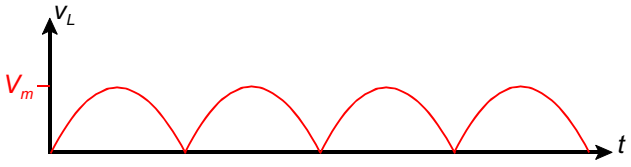

Fig. 106. Full-wave load voltage.

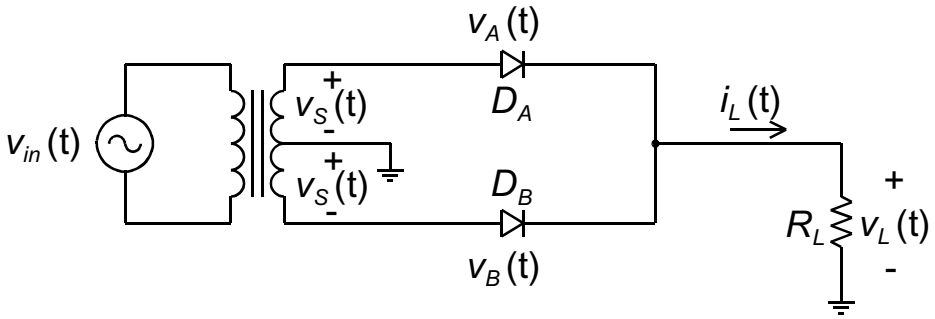

Fig. 107. The full-wave rectifier (Fig. 104 repeated).

Diode Peak Inverse Voltage

When D_A is on, D_B is off . . . a KVL path around the "outside" loop of the transformer secondary shows that D_B must withstand a voltage of $2v_S$.

When D_B is on, D_A is off . . . now a KVL path shows that D_B must withstand $2v_S$.

Thus the diode PIV rating must be $2V_m$. Diode voltage waveforms are shown below . . .

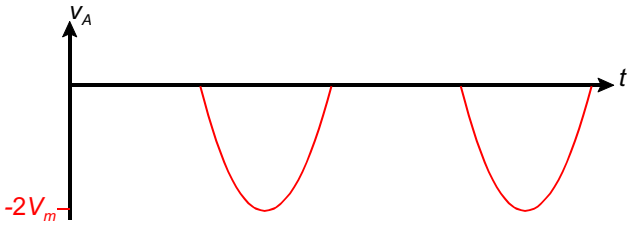

Fig. 108. Voltage across diode D_A.

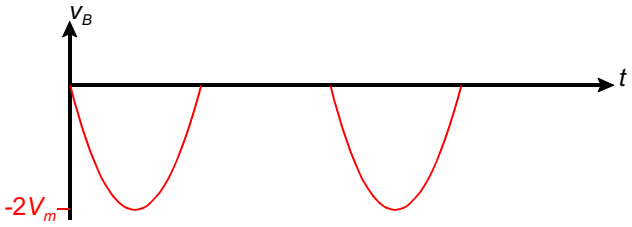

Fig. 109. Voltage across diode D_B.

Diode Applications - The Bridge Rectifier

The bridge rectifier is also a full-wave rectifier, but uses a *diode bridge* rather than a center-tapped transformer:

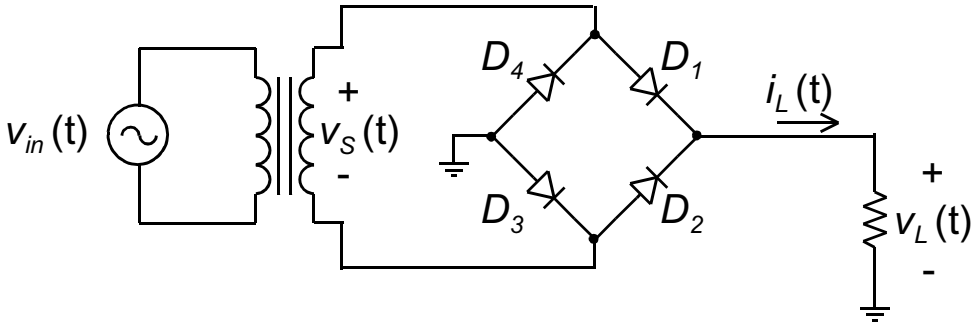

Fig. 110. The bridge rectifier.

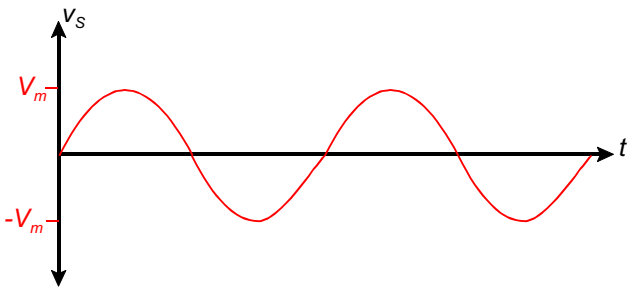

Fig. 111. Input voltage to diode bridge.

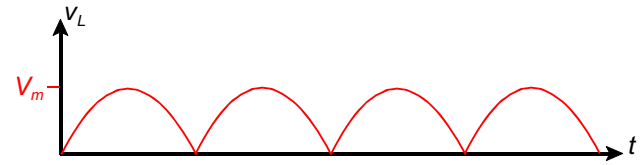

Fig. 112. Full-wave load voltage.

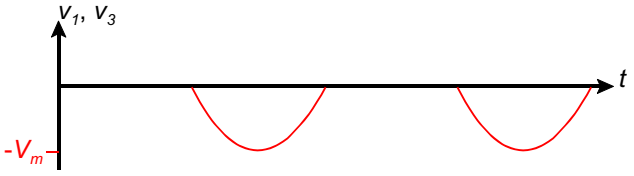

Fig. 113. Diode voltage for D_1 and D_3.

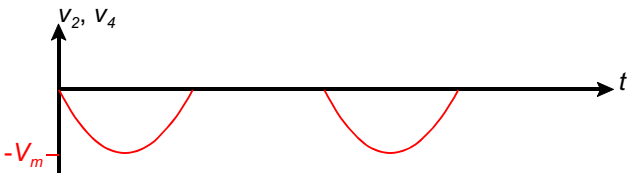

Fig. 114. Diode voltage for D_2 and D_4.

Operation

1st (Positive) Half-Cycle:

Current flows from top end of v_S, through D_1 and R_L, then via ground through D_3, and back to v_S.

2nd (Negative) Half-Cycle:

Current flows from bottom end of v_S, through D_2 and R_L, then via ground through D_4, and back to v_S.

Peak Inverse Voltage:

In each half-cycle the OFF diodes are directly across v_S, thus the diode PIV is V_m.

Diode Applications - Full-Wave/Bridge Rectifier Features

Bridge Rectifier

Much cheaper transformer more than offsets the negligible cost of two more diodes.

Full-Wave Rectifier

Archaic since vacuum tube rectifiers have largely been replaced by semiconductor rectifiers.

Preferable *only* at low voltages (one less diode forward-voltage drop), if at all.

Filtered Full-Wave and Bridge Rectifiers

Because the rectifier output voltage is “full-wave,” C discharges for approximately only half as long as in the half-wave case.

Thus, for a given ripple voltage, only half the capacitance is required (all other parameters being equal).

That is, a factor of 2 appears in denominator of eq. (93):

$$V_r C = \frac{V_m}{2fR_L} \quad \Rightarrow \quad C = \frac{V_m}{2V_r fR_L} \tag{94}$$

Remember though, the design equation *is valid only for small* V_r.

Bipolar Junction Transistors (BJTs)

Introduction

The BJT is a nonlinear, 3-terminal device based on the junction diode. A representative structure sandwiches one semiconductor type between layers of the opposite type. We first examine the *npn* BJT:

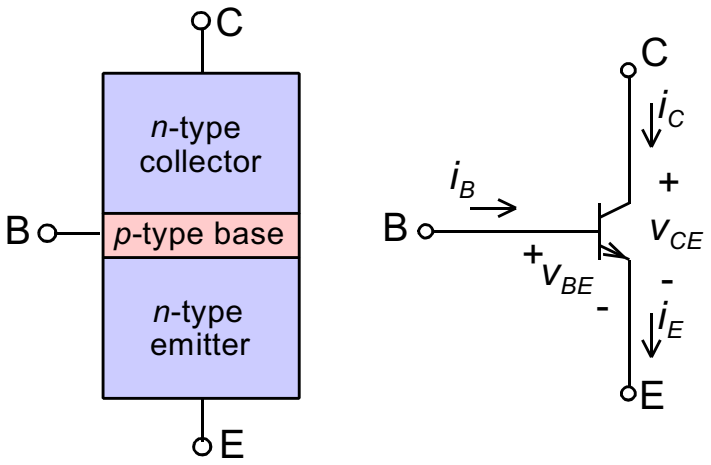

Fig. 115. The *npn* BJT representative physical structure (left), and circuit symbol (right).

Two junctions: collector-base junction (CBJ); emitter-base junction (EBJ).

Current in one *p-n* junction affects the current in the other *p-n* junction.

There are four regions of operation:

Operating Region	EBJ	CBJ	Feature
cutoff	rev.	rev.	$i_C = i_E = i_B = 0$
active	fwd.	rev.	amplifier
saturation	fwd.	fwd.	v_{CE} nearly zero
inverse	rev.	fwd.	limited use

We're most interested in the active region, but will have to deal with cutoff and saturation, as well.

Discussion of inverse region operation is left for another time.

Qualitative Description of BJT Active-Region Operation

- Emitter region is heavily doped . . .lots of electrons available to conduct current.
- Base region very lightly doped and very narrow . . .very few holes available to conduct current.
- Rev-biased CBJ $\Rightarrow$ collector positive w.r.t base.
- Fwd-biased EBJ $\Rightarrow$ base positive w.r.t emitter.
- Emitter current, i_E, consists mostly of electrons being injected into base region; because the base is lightly doped, i_B is small.

  Some of the injected electrons combine with holes in base region.

  Most of the electrons travel across the narrow base and are attracted to the positive collector voltage, creating a *collector current!!!*

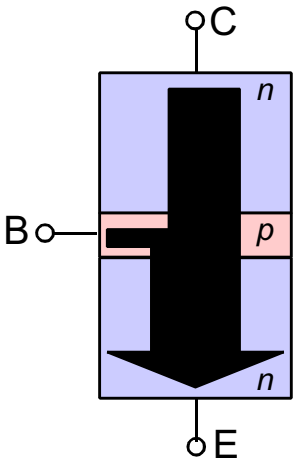

Fig. 116. Active-region BJT currents.

- The relative current magnitudes are indicated by the arrow thicknesses in the figure.
- Because i_B is so small, a small change in base current can cause a large change in collector current - *this is how we get this device to amplify!!!*

Quantitative Description of BJT Active-Region Operation

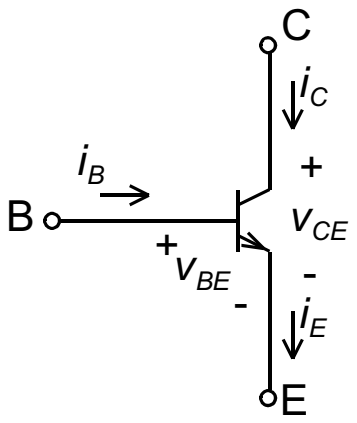

Fig. 117. *Npn* BJT schematic symbol.

The emitter-base junction (EBJ) is a diode and is governed by the Shockley eqn.:

$$i_E = I_{ES}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right] \quad \textbf{(95)}$$

where, I_{ES} ranges from pA to fA
and n is usually ≈ 1

Also, from KCL:

$$i_E = i_B + i_C \quad \textbf{(96)}$$

In the active region (*only!!!*) i_C is a fixed % of i_E, which is dependent on the manufacturing process.

We assign the symbol α to that ratio, thus:

$$\alpha = \frac{i_C}{i_E} \quad \textbf{(97)}$$

Ideally, we would like $\alpha = 1$. Usually, α falls between 0.9 and 1.0, with 0.99 being typical.

Remember*!!!* Eqs. (95) and (96) apply *always*.

Eq. (97) applies *only in the active region*.

From eqs. (95) and (97) we have:

$$i_C = \alpha i_E = \alpha I_{ES}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right] \quad \textbf{(98)}$$

and for a forward-biased EBJ, we may approximate:

$$i_C \approx I_S \exp\left(\frac{v_{BE}}{V_T}\right) \quad \textbf{(99)}$$

where the *scale current,* $I_S = \alpha I_{ES}$.

Also, from eqs. (96) and (97) we have:

$$i_E = i_C + i_B \quad \Rightarrow \quad i_E = \alpha i_E + i_B \quad \Rightarrow \quad i_B = (1-\alpha) i_E \quad \textbf{(100)}$$

thus

$$\frac{i_C}{i_B} = \frac{\alpha i_E}{(1-\alpha) i_E} = \frac{\alpha}{1-\alpha} = \beta \quad \textbf{(101)}$$

Solving the right-hand half of eq. (101) for α:

$$\alpha = \frac{\beta}{\beta + 1} \quad \textbf{(102)}$$

For α = 0.99, we have β = 100. Rearranging eq. (101) gives:

$$i_C = \beta i_B \quad \textbf{(103)}$$

Thus, small changes in i_B produce large changes in i_C, so again we see that the BJT can act as an *amplifier!!!*

BJT Common-Emitter Characteristics

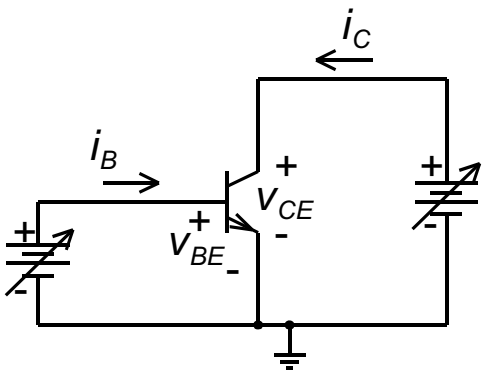

Fig. 118.Circuit for measuring BJT characteristics.

Introduction

We use the term *common-emitter characteristics* because the emitter is common to both voltage sources.

The figure at left represents only how we might *envision* measuring these characteristics. In practice we would *never* connect sources to *any* device without current-limiting resistors in series*!!!*

Input Characteristic

First, we measure the i_B - v_{BE} relationship (with v_{CE} fixed). Not surprisingly, we see a typical diode curve:

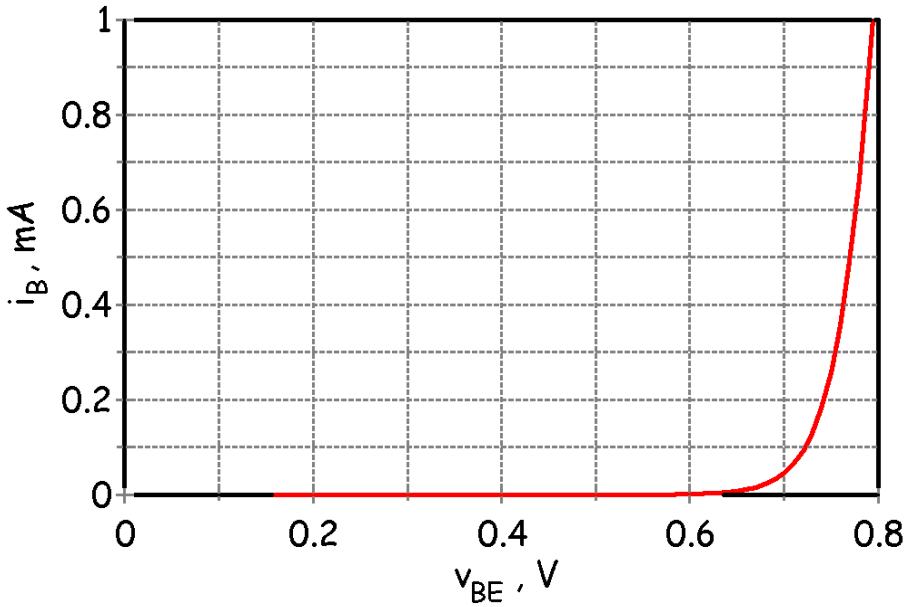

Fig. 119. Typical input characteristic of an *npn* BJT.

This is called the *input characteristic* because the base-emitter will become the *input terminals of our amplifier*.

Output Characteristics

Next, we measure a *family* of i_C - v_{CE} curves for various values of base current:

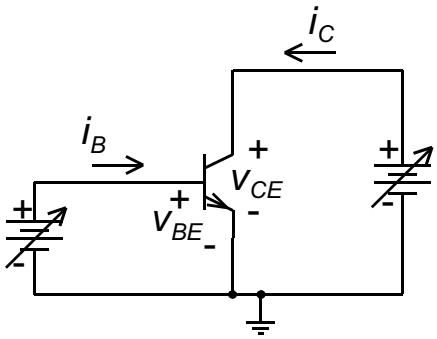

Fig. 120. Circuit for measuring BJT characteristics (Fig. 118 repeated).

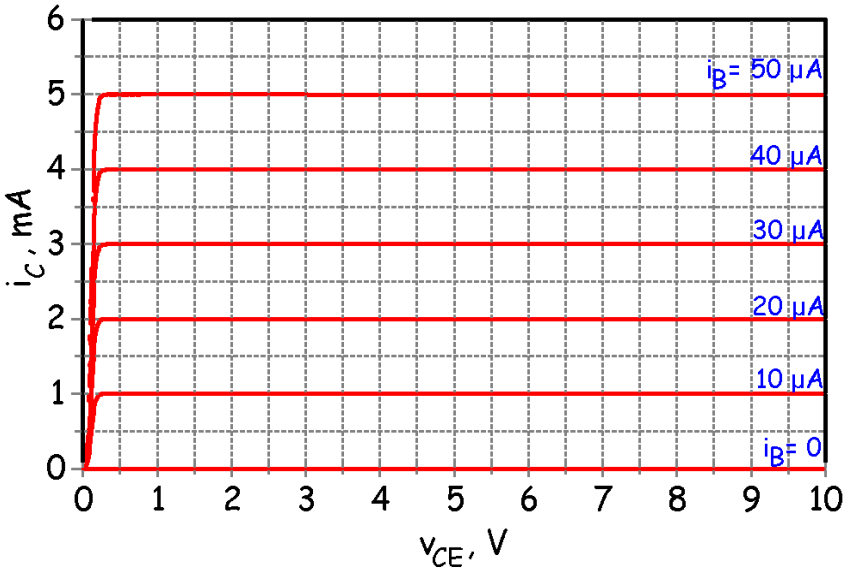

Fig. 121. Typical output characteristics of an *npn* BJT.

Active Region:

Recall that the active region requires that the EBJ be forward-biased, and that the CBJ be reverse-biased.

A forward-biased EBJ means that $v_{BE} \approx 0.7$ V. Thus, the CBJ will be reverse-biased as long as $v_{CE} > 0.7$ V.

Note that i_C and i_B are related by the ratio β, *as long as the BJT is in the active region*.

We can also identify the cutoff and saturation regions . . .

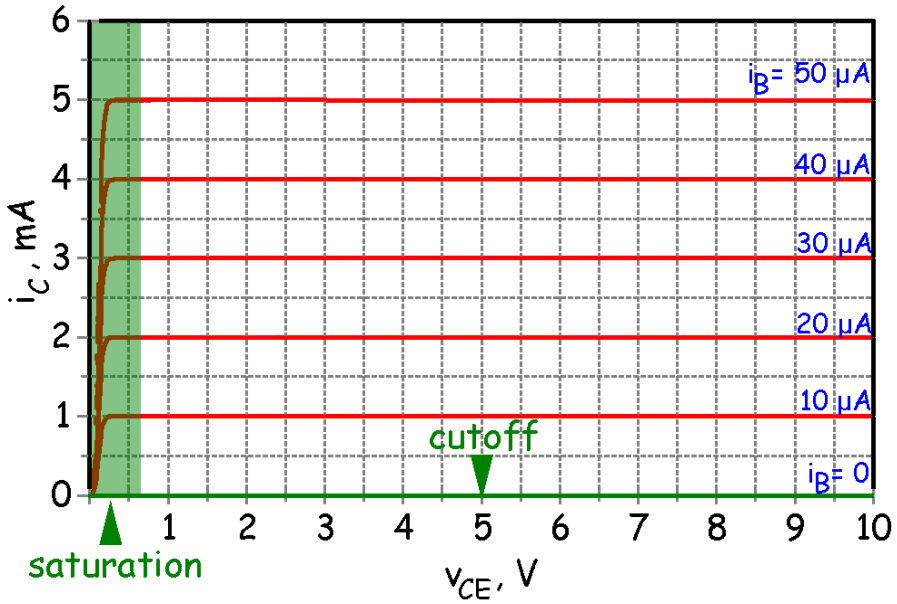

Fig. 122. BJT output characteristics with cutoff and saturation regions identified.

Cutoff:

The EBJ is not forward-biased (sufficiently) if $i_B = 0$. Thus the *cutoff region* is the particular curve for $i_B = 0$ (i.e., the horizontal axis).

Saturation:

When the EBJ is forward-biased, $v_{BE} \approx 0.7$ V. Then, the CBJ is reverse-biased for any $v_{CE} > 0.7$ V. Thus, the *saturation region* lies to the left of $v_{CE} = 0.7$ V.

Note that the CBJ must become forward-biased by 0.4 V to 0.5 V before the $i_C = \beta i_B$ relationship disappears, just as a diode must be forward-biased by 0.4 V to 0.5 V before appreciable forwardcurrent flows.

The *pnp* BJT

We get the same behavior with an *n*-type base sandwiched between a *p*-type collector and a *p*-type emitter:

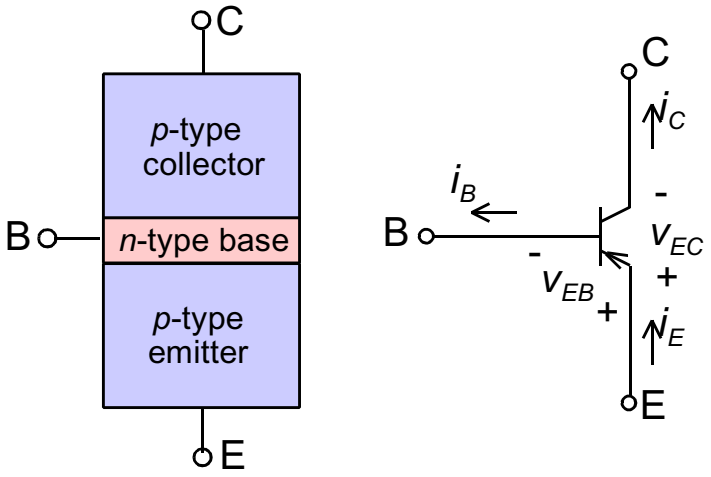

Fig. 123. A *pnp* BJT and its schematic symbol. Note that the current and voltage references have been reversed.

Now current in a fwd. biased EBJ flows in the opposite direction . . .

. . . i_C and i_E resulting from active region operation also flow in the opposite direction.

Note that the voltage and current references are reversed.

But the equations have the same appearance:

In general,

$$i_E = i_B + i_C \quad \text{and} \quad i_E = I_{ES}\left[\exp\left(\frac{v_{EB}}{V_T}\right) - 1\right] \tag{104}$$

And for the active region in particular,

$$i_C = \alpha i_E\,, \quad i_C = \beta i_B \quad \text{and} \quad i_C \approx I_S \exp\left(\frac{v_{EB}}{V_T}\right) \tag{105}$$

where, the latter equation is the approximation for a forward-biased EBJ.

Because the voltage and current references are reversed, the input and output characteristics appear the same also:

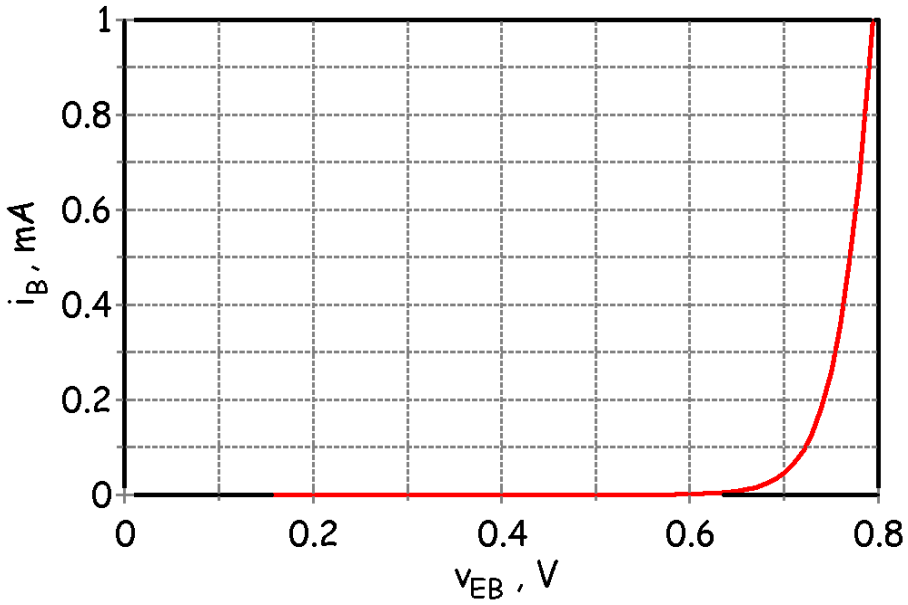

Fig. 124. Input characteristic of a *pnp* BJT.

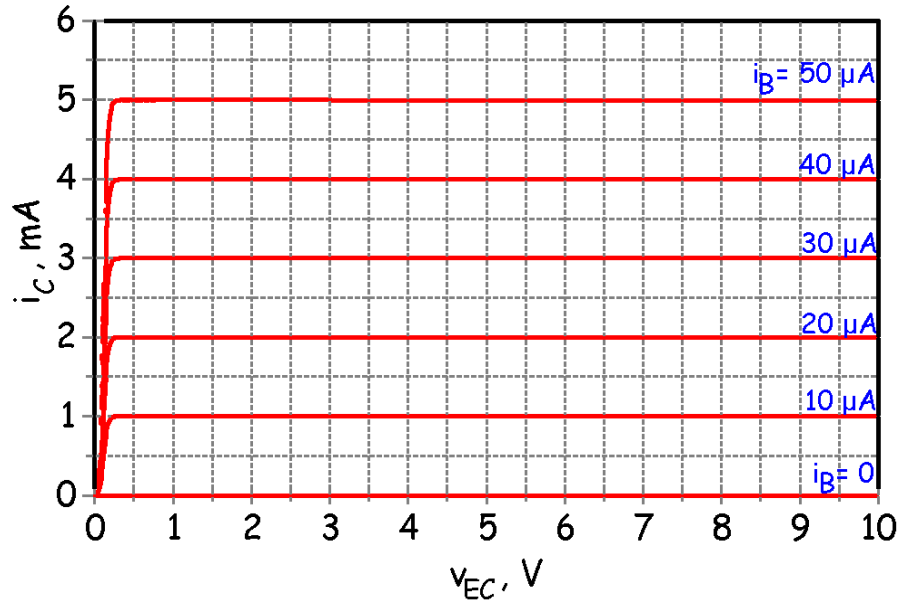

Fig. 125. Output characteristics of a *pnp* BJT.

BJT Characteristics - Secondary Effects

The characteristics of real BJTs are somewhat more complicated than what has been presented here (of course*!!!*).

One *secondary effect* you need to be aware of . . .

- Output characteristics are *not* horizontal in the active region, but have an upward slope . . .
- This is due to the *Early effect*, a change in base width as v_{CE} changes (also called *base width modulation*) . . .
- Extensions of the actual output characteristics intersect at the *Early voltage, V_A* . . .
- Typical value of V_A is 50 V to 100 V.

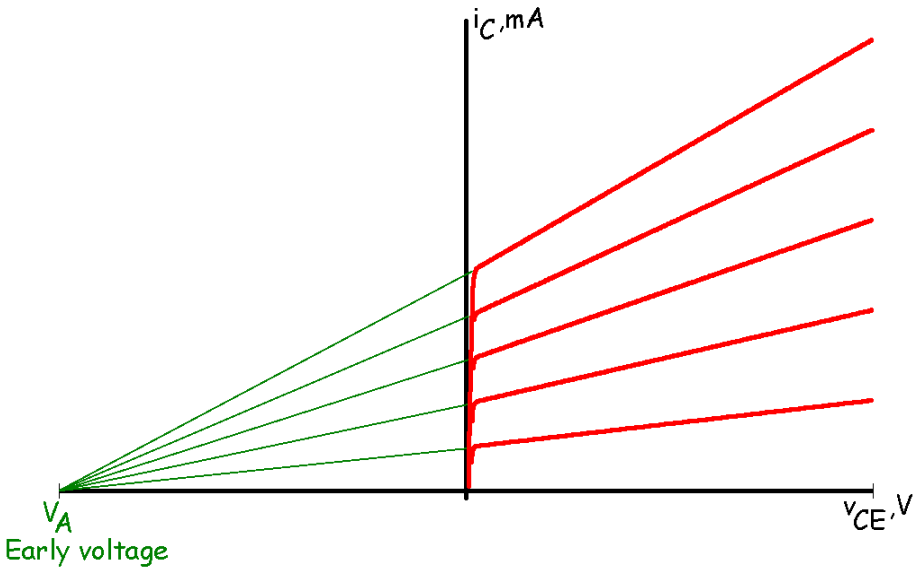

Fig. 126. BJT output characteristics illustrating Early voltage.

Other secondary effects will be described as needed.

The n-Channel Junction FET (JFET)

The *field-effect transistor*, or *FET*, is also a 3-terminal device, but it is constructed, and functions, somewhat differently than the BJT. There are several types. We begin with the *junction FET (JFET)*, specifically, the *n-channel JFET*.

Description of Operation

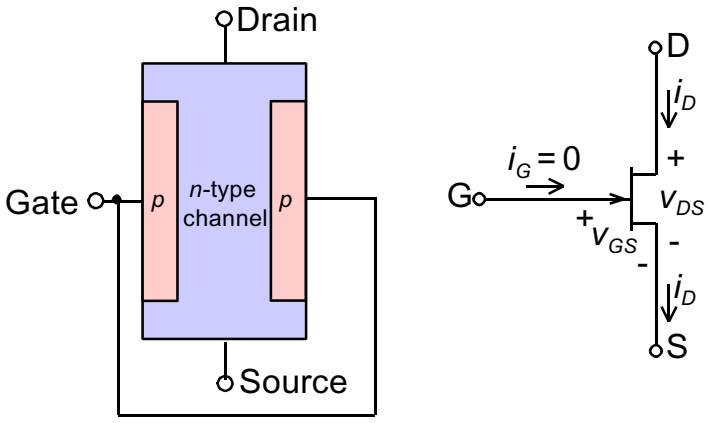

Fig. 127. The *n*-channel JFET representative physical structure (left) and schematic symbol (right).

The *p-n* junction is a typical diode . . .

Holes move from *p*-type into *n*-type . . .

Electrons move from *n*-type into *p*-type . . .

Region near the *p-n* junction is left without any available carriers - *depletion region*

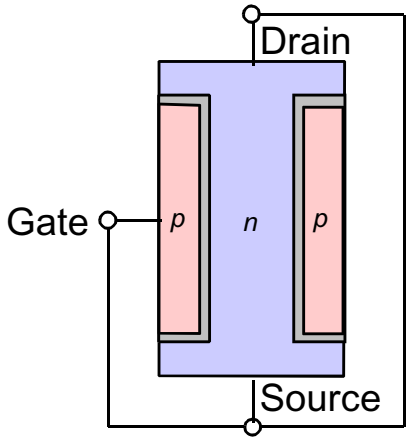

Fig. 128. Depletion region depicted for $v_{GS} = 0$, $v_{DS} = 0$.

The depletion region is shown at left for zero applied voltage (called *zero bias*). . .

Carriers are still present in the *n*-type channel . . .

Current could flow between drain and source (if $v_{DS} \neq 0$) . . .

Channel has relatively low resistance.

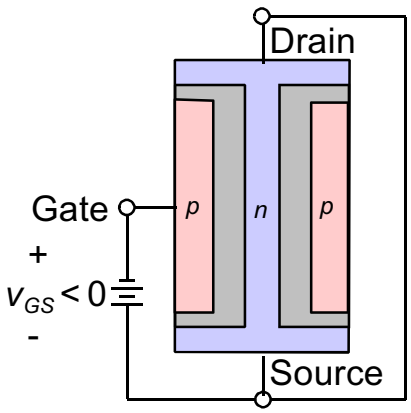

Fig. 129.
Depletion region for negative v_{GS} (reverse bias).

As the reverse bias increases across the *p-n* junction, the depletion region width increases,

Because negative voltage at the Gate pulls holes away from junction,

And positive voltage at the Source pulls electrons away from junction.

Thus, the channel becomes narrower, and the channel resistance increases.

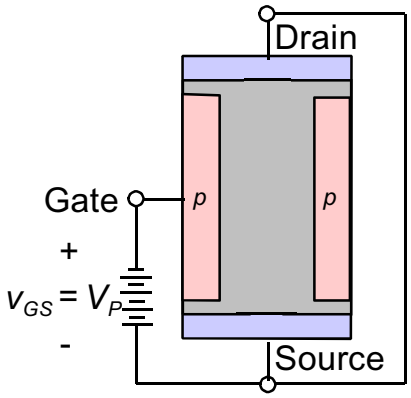

Fig. 130. Depletion region at pinch-off ($v_{GS} = V_P$).

With sufficient reverse bias the depletion region *pinches-off* the entire channel:

$$v_{GS} = V_P \text{, } \underline{\textit{pinch-off voltage}}$$

The channel resistance becomes infinite; current flow impossible for any v_{DS} (less than breakdown).

Typical values: $-5 < V_P < -2$

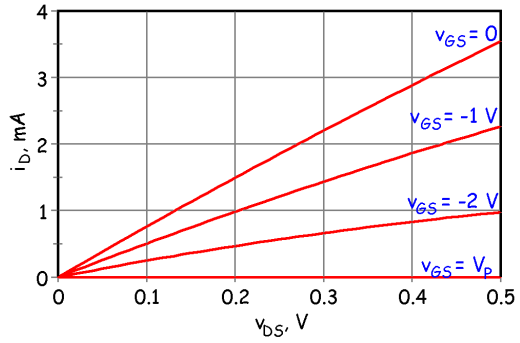

Fig. 131. FET *i-v* curves for small v_{DS}.

Thus, the FET looks like a *voltage-controlled resistance* at small values of v_{DS}.

This region of FET operation is called the *voltage-controlled resistance*, or *triode*, region.

Now, as v_{DS} increases, the depletion region becomes asymmetrical:

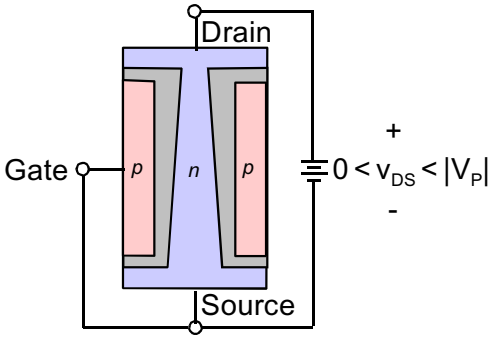

Fig. 132. Asymmetrical depletion region as v_{DS} increases.

Reverse bias is greater at the drain end, so the depletion region is greater at the drain end.

Thus the channel becomes more restricted and, for fixed v_{GS}, *i-v* curves become flatter (i.e., more horizontal).

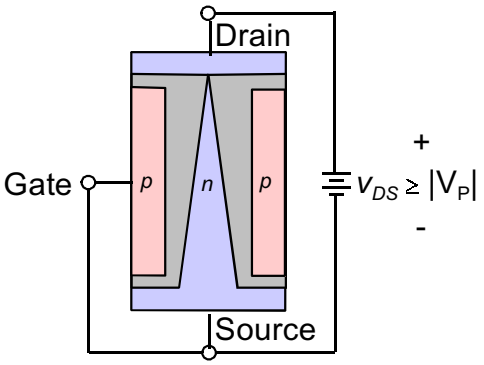

Fig. 133.Pinch-off at drain end for $v_{DS} = V_P$.

For $v_{DS} = |V_P|$ channel becomes pinched-off only at drain end.

Carriers drift across pinched-off region under influence of the *E* field.

The *rate* of drift, and therefore the drain current flow, is dependent on width of entire channel (i.e., on v_{GS}), but *independent of* v_{DS}*!!!*

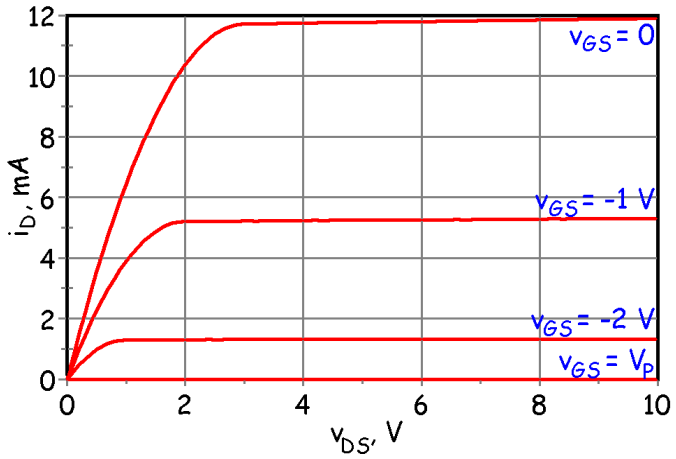

Fig. 134. *N*-channel JFET output characteristics (2N3819).

As v_{GS} changes, the curves become horizontal at different values of drain current.

Thus, we have a device with the <u>*output characteristics*</u> at left.

Note that they are *very* similar to BJT curves, though the physical operation is *very* different.

Equations Governing n-Channel JFET Operation

Cutoff Region:

The FET is in cutoff for $v_{GS} \leq V_P$, and for any v_{DS}:

$$i_D = 0 \tag{106}$$

Triode Region:

The FET is in the triode region for $0 > v_{GS} > V_P$, and $v_{GD} > V_P$:

$$i_D = K\left[2\left(v_{GS} - V_P\right)v_{DS} - {v_{DS}}^2\right] \tag{107}$$

where K has units of amperes per square volt, A/V^2

For very small values of v_{DS}, the ${v_{DS}}^2$ term in the above eguation is negligible:

$$i_D = 2K\left(v_{GS} - V_P\right)v_{DS}, \quad \text{for small } v_{DS} \tag{108}$$

and the channel resistance is approximately given by:

$$R_{channel} \approx \frac{v_{DS}}{i_D} \approx \frac{1}{2K\left(v_{GS} - V_P\right)} \tag{109}$$

Pinch-Off Region:

The FET is in the pinch-off region for $0 > v_{GS} > V_P$, and $v_{GD} < V_P$:

$$i_D = K\left(v_{GS} - V_P\right)^2 \tag{110}$$

The *pinch-off region* (also called the *saturation region*) is most useful for amplification.

*Note that v_{GS} is **never** allowed to forward bias the p-n junction !!!*

The Triode - Pinch-Off Boundary

We know pinch-off just occurs at the drain end when:

$$v_{GD} = V_P \quad \Rightarrow \quad v_{GS} - v_{DS} = V_P \quad \Rightarrow \quad v_{GS} - V_P = v_{DS} \tag{111}$$

But from eq. (110)

$$v_{GS} - V_P = \sqrt{\frac{i_D}{K}} \tag{112}$$

Combining eqs. (111) and (112) gives the boundary:

$$v_{DS} = \sqrt{\frac{i_D}{K}} \quad \Rightarrow \quad i_D = K v_{DS}^{\,2} \tag{113}$$

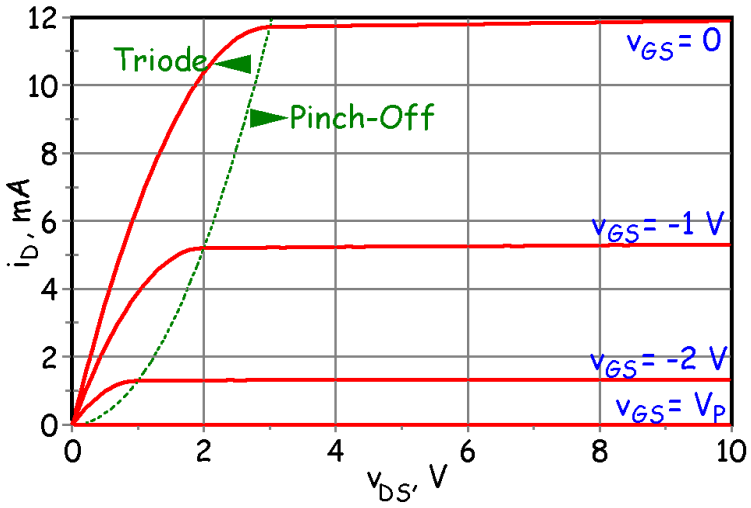

Fig. 135. 2N3819 *n*-channel JFET output characteristics showing the triode - pinch-off boundary.

The output characteristics exhibit a breakdown voltage for sufficient magnitude of v_{DS}.

"Real" output characteristics also have an upward slope and can be characterized with an "Early" voltage, V_A.

The Transfer Characteristic

Because the gate-channel *p*-*n* junction is reversed biased *always*, the input *i*-*v* characteristic of a FET is trivial.

However, the pinch-off region equation (110), repeated below, gives rise to a *transfer characteristic*:

$$i_D = K(v_{GS} - V_P)^2 \qquad \textbf{(114)}$$

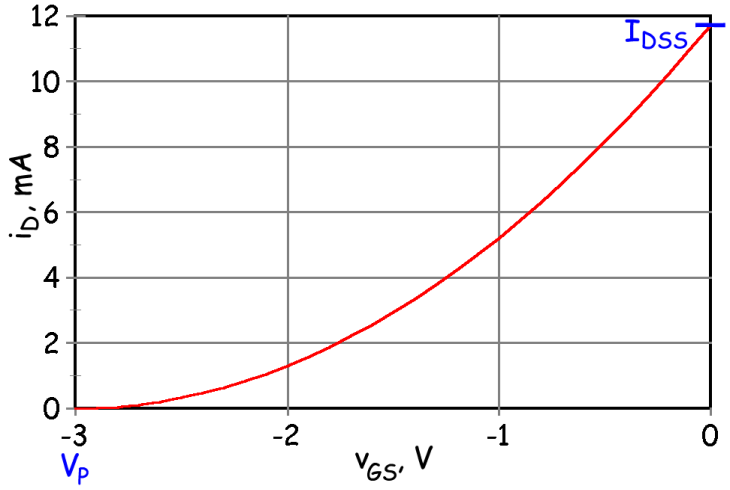

Fig. 136. 2N3819 *n*-channel JFET transfer characteristic.

I_{DSS} is the *zero-gate-voltage drain current*. Substituting $i_D = I_{DSS}$ and $v_{GS} = 0$ into eq. (114) gives a relationship between K and I_{DSS}:

$$K = \frac{I_{DSS}}{V_P^{\,2}} \qquad \textbf{(115)}$$

Metal-Oxide-Semiconductor FETs (MOSFETs)

MOSFETs are constructed quite differently than JFETs, but their electrical behavior is extremely similar . . .

The n-Channel Depletion MOSFET

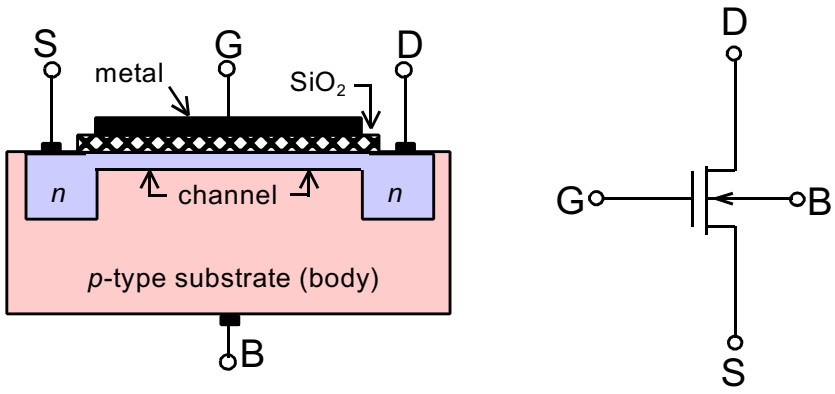

Fig. 137. The *n*-channel depletion MOSFET representative physical structure (left) and schematic symbol (right).

The depletion MOSFET is built horizontally on a *p*-type substrate:

- *n*-type wells, used for the source and drain, are connected by a very thin *n*-type channel . . .
- The gate is a metallized layer insulated from the channel by a thin oxide layer . . .
- Negative gate voltages repel electrons from the channel, causing the channel to narrow . . .

  When v_{GS} is sufficiently negative ($v_{GS} = V_P$), the channel is pinched-off . . .
- Positive gate voltages attract electrons from the substrate, causing the channel to widen . . .

The n-Channel Enhancement MOSFET

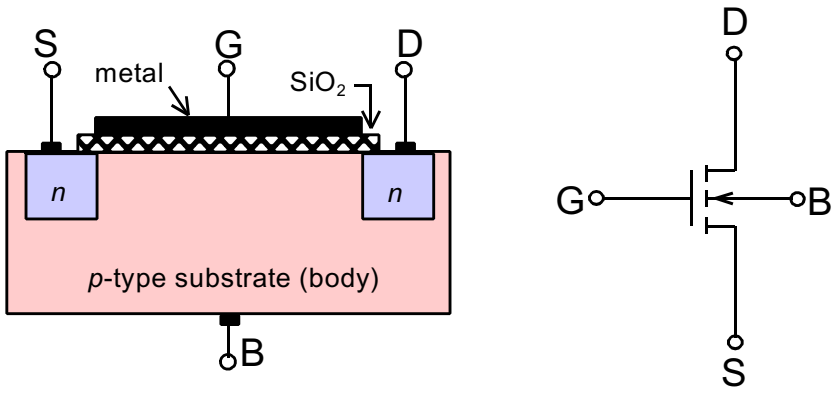

Fig. 138. The *n*-channel enhancement MOSFET physical structure (left) and schematic symbol (right).

The MOSFET is built horizontally on a *p*-type substrate. . .

- *n*-type wells, used for the source and drain, are not connected by a channel at all . . .
- The gate is a metallized layer insulated from the channel by a thin oxide layer . . .
- Positive gate voltages attract electrons from the substrate . . .

  When v_{GS} is sufficiently positive, i.e., greater than the *threshold voltage*, V_{TH}, an *n*-type channel *is formed* (i.e., a channel is *enhanced*) . . .

  V_{TH} functions exactly like a "positive-valued V_P"

Comparison of *n*-Channel FETs

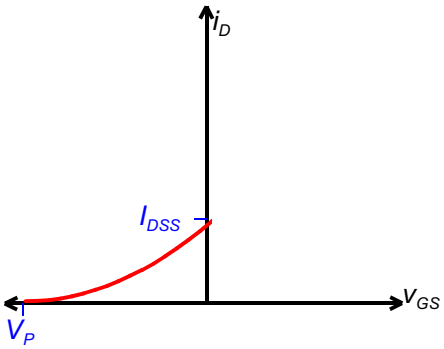

Fig. 139. Transfer char., *n*-channel JFET.

- The *n*-channel JFET can *only* have negative gate voltages . . .

  p-*n* junction must remain reversed biased . . .

  Actual device can operate with v_{GS} *slightly* positive, approx. 0.5 V max.

$$i_D = K(v_{GS} - V_P)^2 \qquad (116)$$

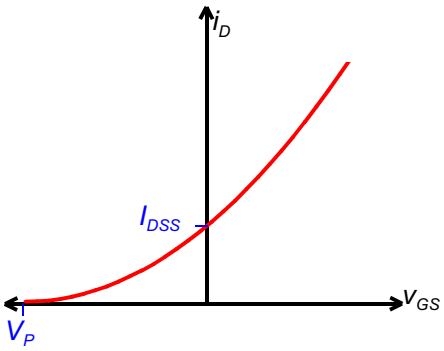

Fig. 140. Transfer char., *n*-channel depletion MOSFET.

- The *n*-channel depletion MOSFET can have either negative or positive gate voltages . . .

  Gate current prevented by oxide insulating layer in either case.

$$i_D = K(v_{GS} - V_P)^2 \qquad (117)$$

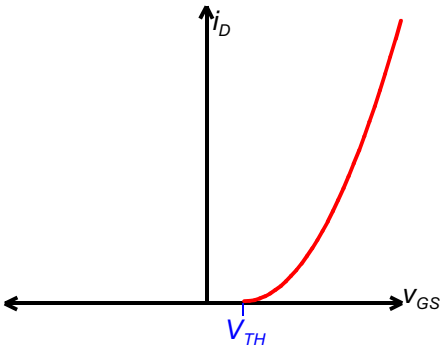

Fig. 141. Transfer char., *n*-channel enhancement MOSFET.

- The *n*-channel enhancement MOSFET can have only positive gate voltages . . .

  Gate current prevented by oxide insulating layer . . .

  Only the notation changes in the equation:

$$i_D = K(v_{GS} - V_{TH})^2 \qquad (118)$$

n-channel FET output characteristics differ only in v_{GS} values:

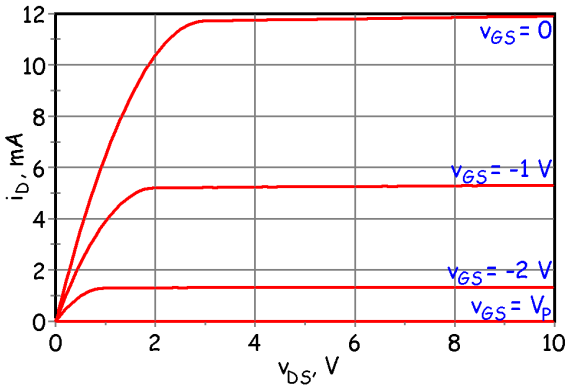

Fig. 142. Typical output characteristics, *n*-channel JFET.

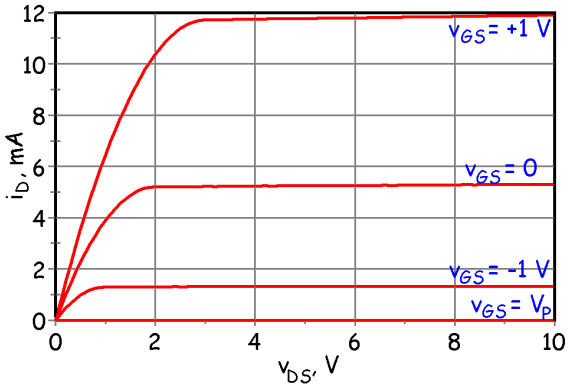

Fig. 143. Typical output characteristics, *n*-channel depletion MOSFET.

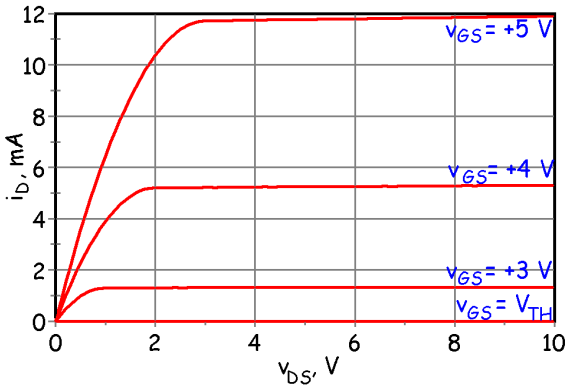

Fig. 144. Typical output characteristics, *n*-channel enhancement MOSFET.

p-Channel JFETs and MOSFETs

By switching *n*-type semiconductor for *p*-type, and vice versa, we create *p*-channel FETs . . .

The physical principles of operation are directly analogous . . .

Actual current directions and voltage polarities are reversed from the corresponding *n*-channel devices . . .

Schematic symbols simply have the arrows reversed (because arrow indicates direction of forward current in the corresponding *p*-*n* junction):

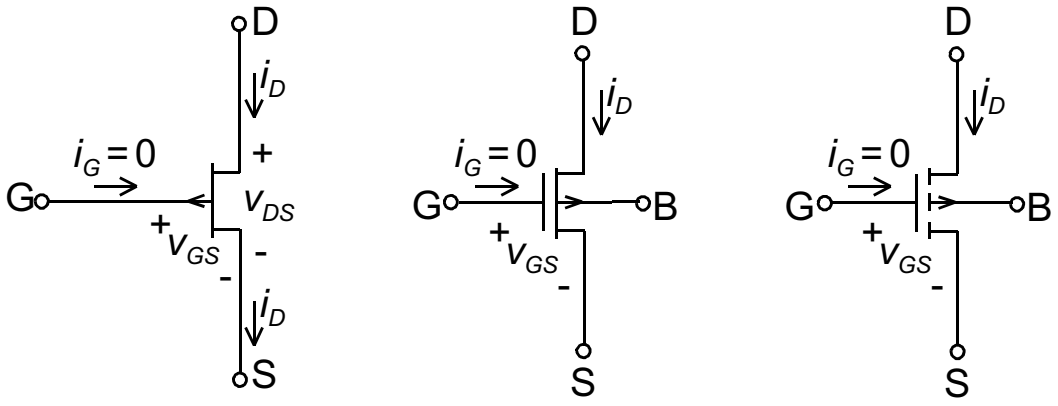

Fig. 145.Schematic symbols for *p*-channel FETs.
From left to right: JFET, depletion MOSFET, enhancement MOSFET.

Note the same reference directions and polarities for *p*-channel devices as we used for *n*-channel devices . . .

i-*v* curves for *p*-channel FETs are identical to *n*-channel curves, except algebraic signs are reversed.

For comparing transfer characteristics on *p*-channel and *n*-channel devices, the following approach is helpful:

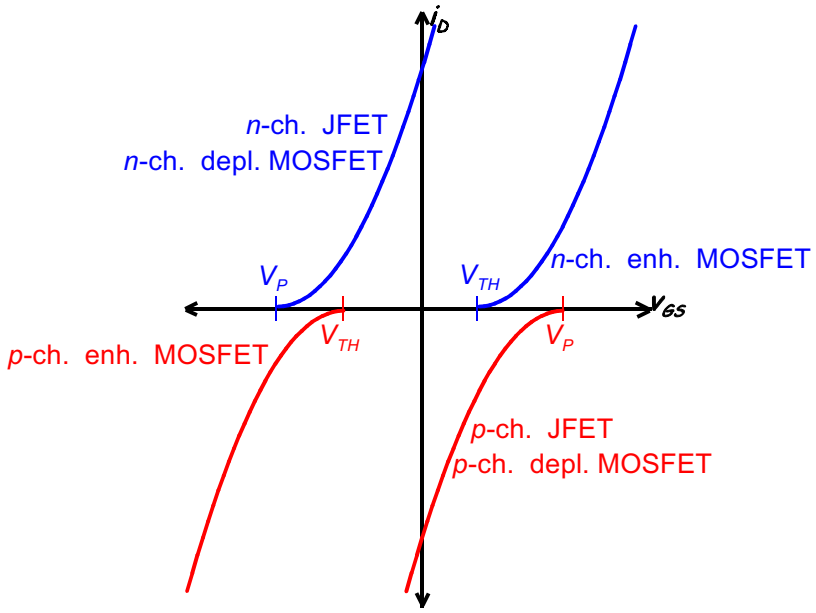

Fig. 146. Comparison of *p*-channel and *n*-channel transfer characteristics.

But more often you'll see negative signs used to labels axes, or values along the axes, such as these examples:

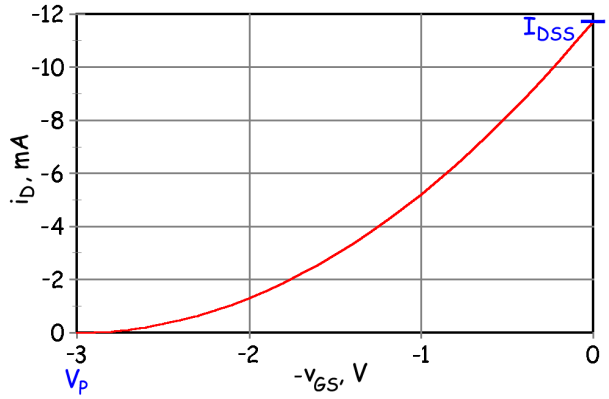

Fig. 147. Typical *p*-channel transfer characteristic.

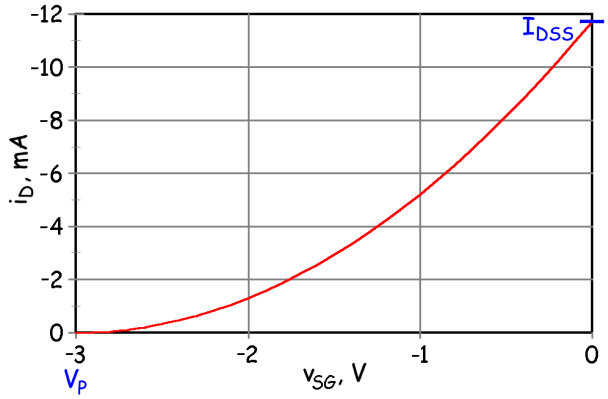

Fig. 148. Typical *p*-channel transfer characteristic.

Output characteristics for *p*-channel devices are handled in much the same way:

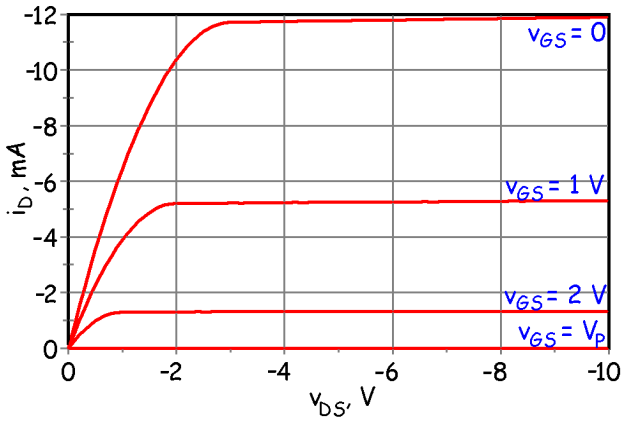

Fig. 149. Typical *p*-channel output characteristic.

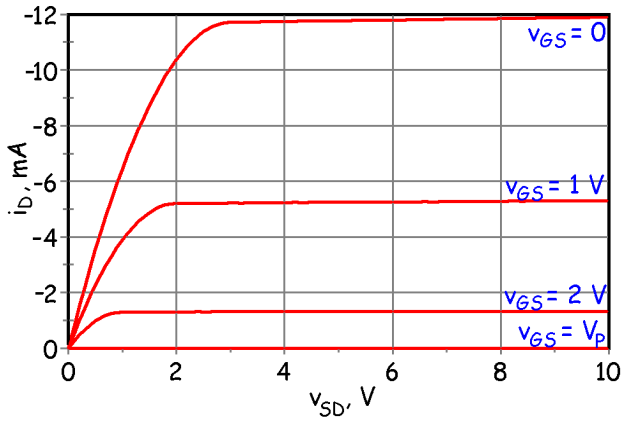

Fig. 150. Typical *p*-channel output characteristic.

Equations governing *p*-channel operation are *exactly* the same as those for *n*-channel operation. Replacing V_P with V_{TH} as necessary, they are:

Cutoff Region:

(in cutoff for $v_{GS} \geq V_P$, and for *any* v_{DS})

$$i_D = 0 \tag{119}$$

Triode Region:

(for $v_{GS} < V_P$, and $v_{GD} < V_P$)

$$i_D = K\left[2\left(v_{GS} - V_P\right)v_{DS} - {v_{DS}}^2\right] \tag{120}$$

where K is negative, and has units of -A/V^2

Pinch-Off Region:

(for $v_{GS} < V_P$, and $v_{GD} > V_P$)

$$i_D = K\left(v_{GS} - V_P\right)^2 \tag{121}$$

Other FET Considerations

FET Gate Protection

The gate-to-channel impedance (especially in MOSFETs) can exceed 1 GΩ *!!!*

To protect the thin gate oxide layer, zeners are often used:

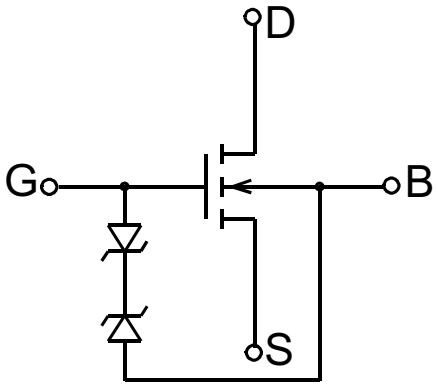

Fig. 151. Zener-diode gate protection of a MOSFET.

Zeners can be used externally, but are usually incorporated right inside the FET case.

Many FET device types available with or without zener protection.

Zener protection adds capacitance, which reduces FET performance at high frequencies.

The Body Terminal

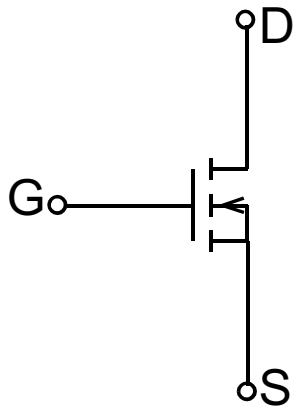

Fig. 152. Normal MOSFET body-source connection.

In some (rare) applications the body terminal of MOSFETs is used to influence the drain current.

Usually the body is connected to the source terminal or a more negative voltage (to prevent inadvertently forward-biasing the channel-body *parasitic* diode).

Basic BJT Amplifier Structure

Circuit Diagram and Equations

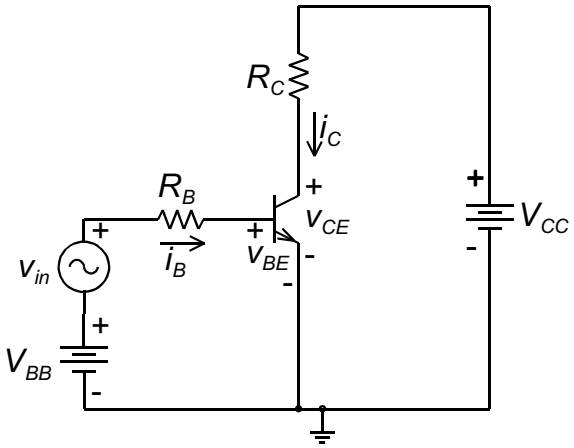

Fig. 153. Basic BJT amplifier structure.

The basic BJT amplifier takes the form shown:

KVL equation around B-E loop:

$$V_{BB} + v_{in} = i_B R_B + v_{BE} \quad \textbf{(122)}$$

KVL equation around C-E loop:

$$V_{CC} = i_C R_C + v_{CE} \quad \textbf{(123)}$$

Load-Line Analysis - Input Side

Remember that the base-emitter is a *diode*.

The Thevenin *resistance* is constant, *voltage* varies with time, but the Thevenin. Thus, the load line has constant slope ($-1/R_B$), and *moves with time*.

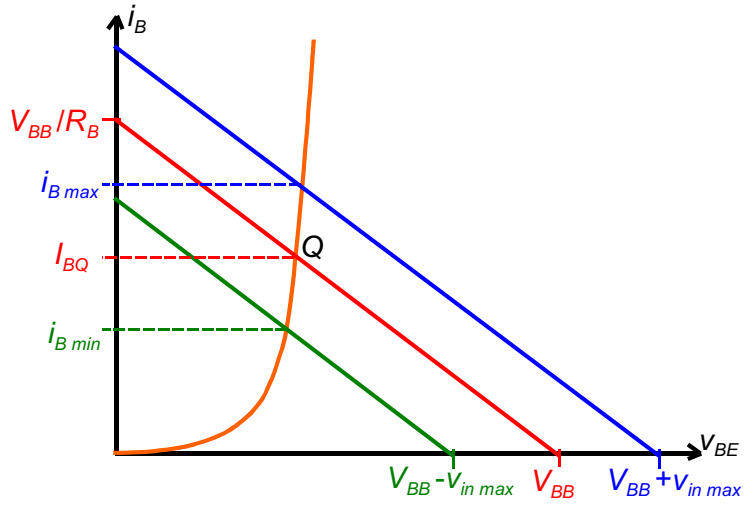

Fig. 154. Load-line analysis around base-emitter loop.

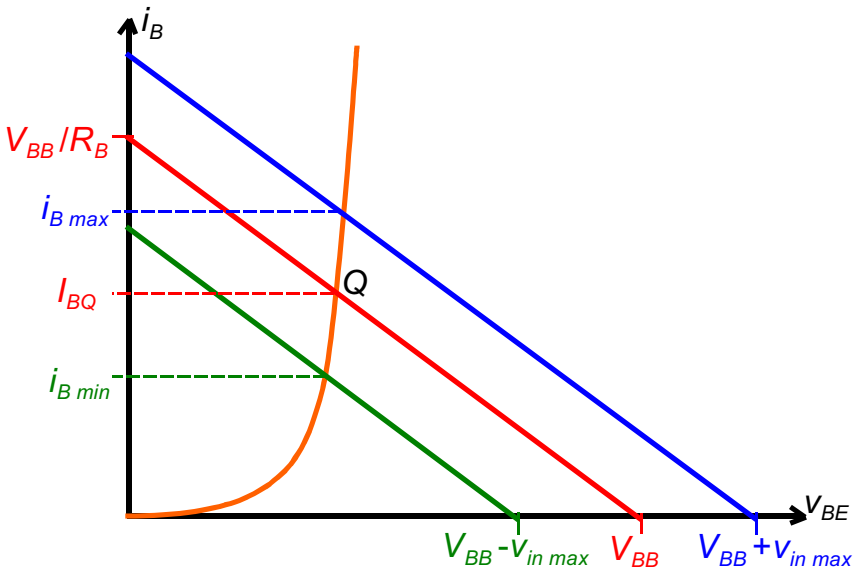

Fig. 155. Load-line analysis around base-emitter loop (Fig. 154 repeated).

- The load line shown in red for $v_{in} = 0$.

  When $v_{in} = 0$, only dc remains in the circuit.

  This i_B, v_{BE} operating pt. is called the *quiescent pt*.

  The *Q-point* is given special notation: I_{BQ}, V_{BEQ}

- Maximum excursion of load line with v_{in} is shown in blue.

- Minimum excursion of load line with v_{in} is shown in green.

- Thus, as v_{in} varies through its cycle, base current varies from $i_{B\,max}$ to $i_{B\,min}$.

  The base-emitter voltage varies also, from $v_{BE\,max}$ to $v_{BE\,min}$, though we are less interested in v_{BE} at the moment.

Load-Line Analysis - Output Side

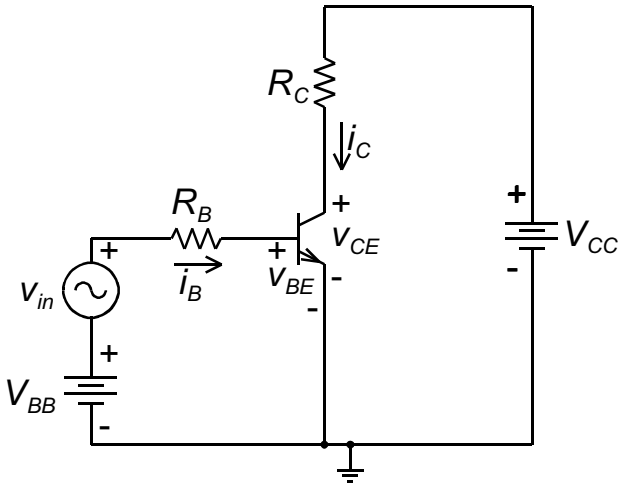

Fig. 156. Basic BJT amplifier structure (Fig. 153 repeated).

Returning to the circuit, observe that V_{CC} and R_C form a Thevenin equivalent, with output variables i_C and v_{CE}.

Thus we can plot this load line on the transistor *output characteristics!!!*

Because neither V_{CC} nor R_C are time-varying, this load line is fixed*!!!*

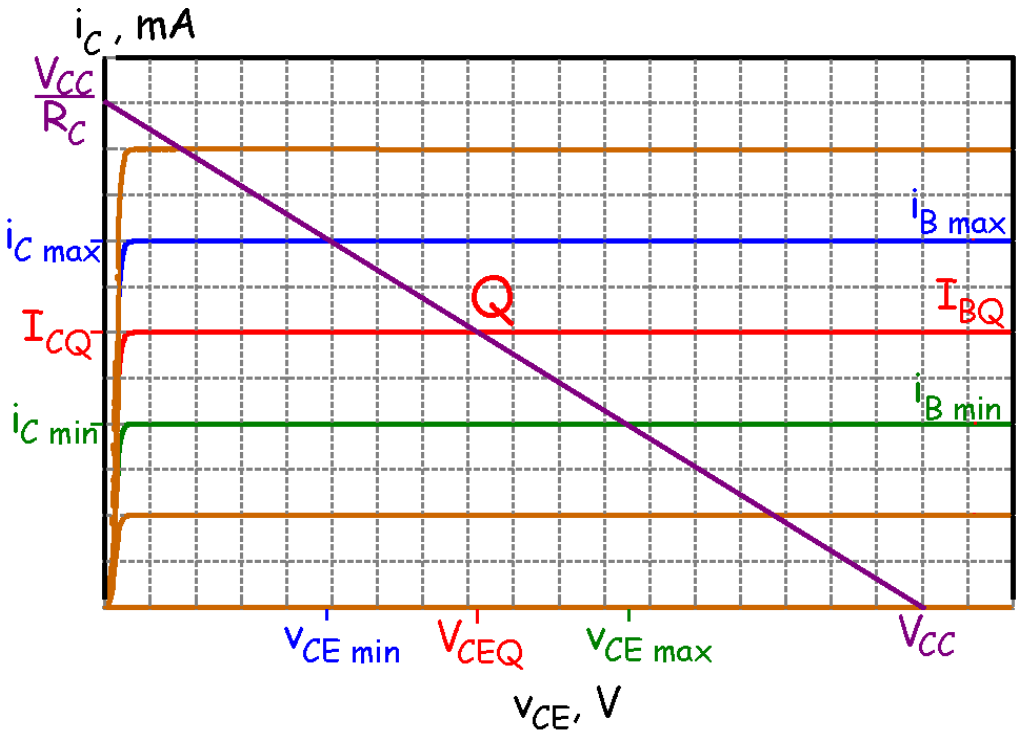

Fig. 157. Amplifier load line on BJT output characteristics.

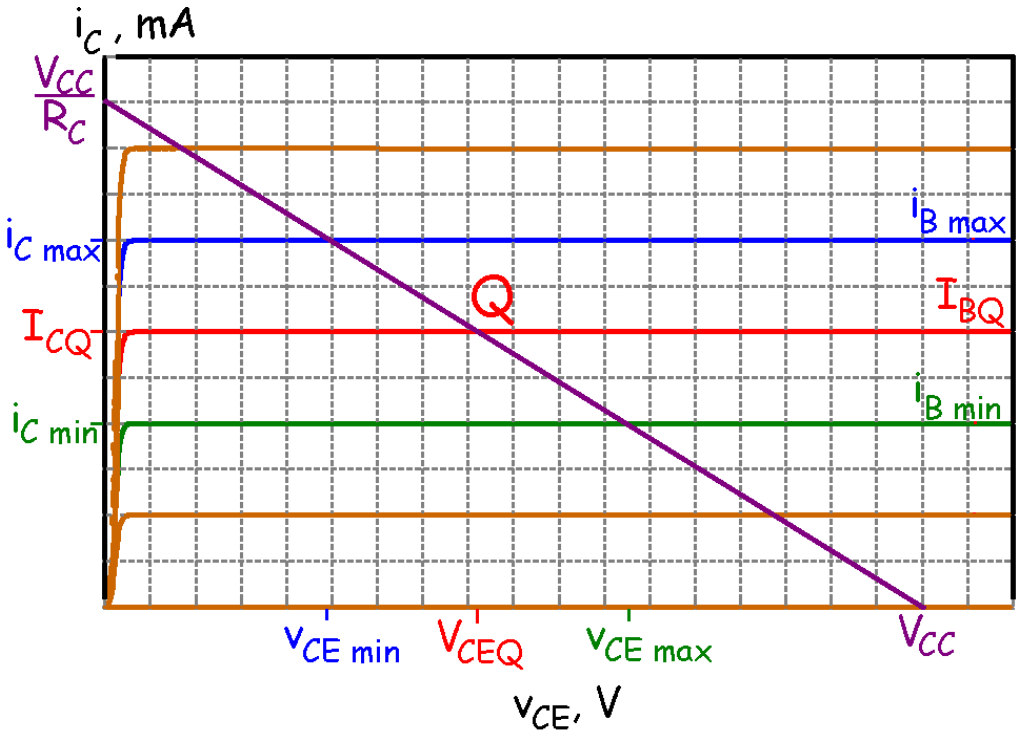

Fig. 158. Amplifier load line on BJT output characteristics (Fig. 157 repeated).

- The collector-emitter operating point is given by the intersection of the load line and the appropriate base current curve . . .

  when $v_{in} = 0$, $i_B = I_{BQ}$, and the quiescent pt. is I_{CQ}, V_{CEQ}

  at $v_{in\ max}$, $i_B = i_{B\ max}$, and the operating pt. is $i_{C\ max}$, $v_{CE\ min}$

  at $v_{in\ min}$, $i_B = i_{B\ min}$, and the operating pt. is $i_{C\ min}$, $v_{CE\ max}$

- If the total change in v_{CE} is greater than total change in v_{in}, we have an *amplifier* !!!

A Numerical Example

Let's look at a PSpice simulation of realistic circuit:

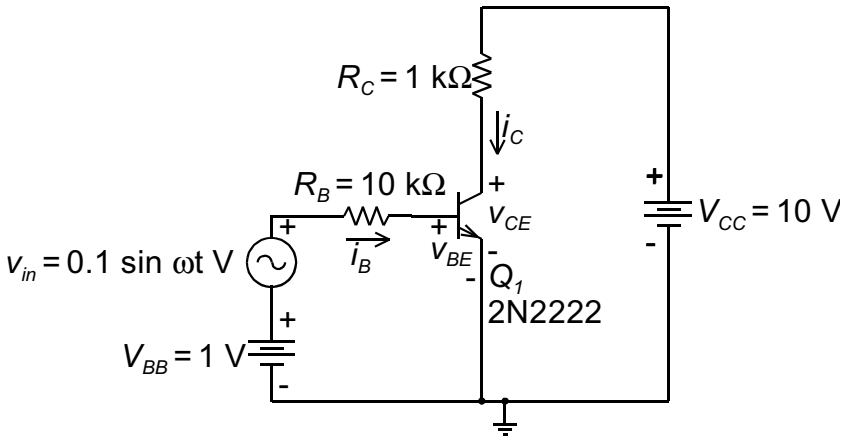

Fig. 159. Example circuit illustrating basic amplifier structure.

First we generate the input characteristic and draw the appropriate base-emitter circuit load lines:

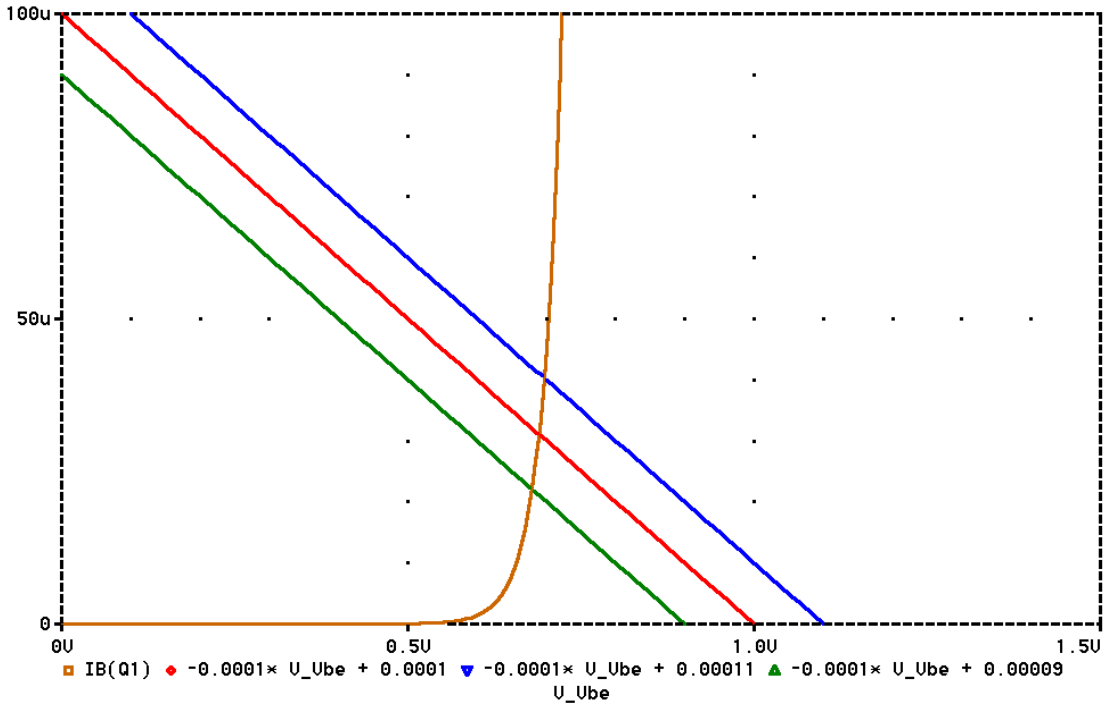

Fig. 160. PSpice-simulated 2N2222 input characteristic.

Using the *cursor* tool in the PSpice software plotting package, we determine:

$$i_{B\,min} = 22\ \mu A \qquad I_{BQ} = 31\ \mu A \qquad i_{B\,max} = 40\ \mu A$$

Next we generate the output characteristics and superimpose the collector-emitter circuit load line:

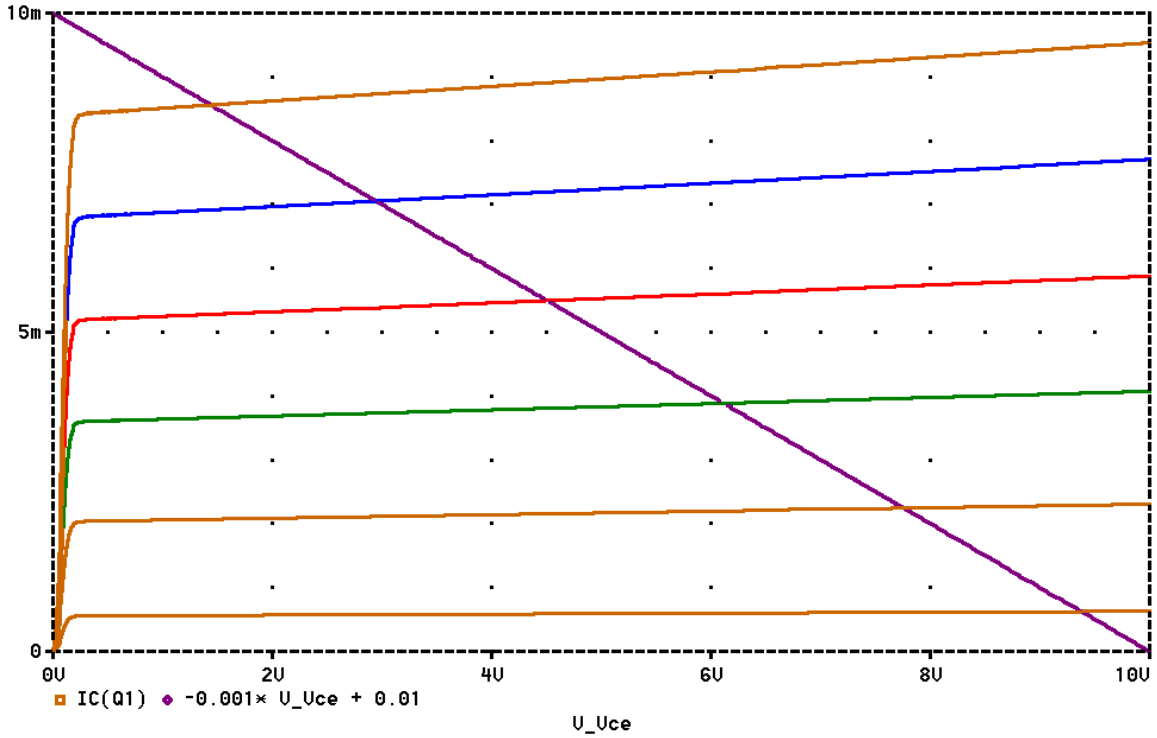

Fig. 161. 2N2222 output characteristics, with curves for base currents of (from bottom to top) 4 μA, 13 μA, 22 μA, 31 μA, 40 μA, and 49 μA.

The resulting collector-emitter voltages are:

$$v_{CE\,min} = 2.95\ V \qquad V_{CEQ} = 4.50\ V \qquad v_{CE\,max} = 6.11\ V$$

Finally, using peak-to-peak values we have a voltage gain of:

$$A_v = \frac{\Delta v_{CE}}{\Delta v_{in}} = \frac{2.95\,V - 6.11\,V}{0.2\,V} = -15.8 \quad !!! \qquad (124)$$

Of course, PSpice can give us the waveforms directly (and can even give us gain, if we desire):

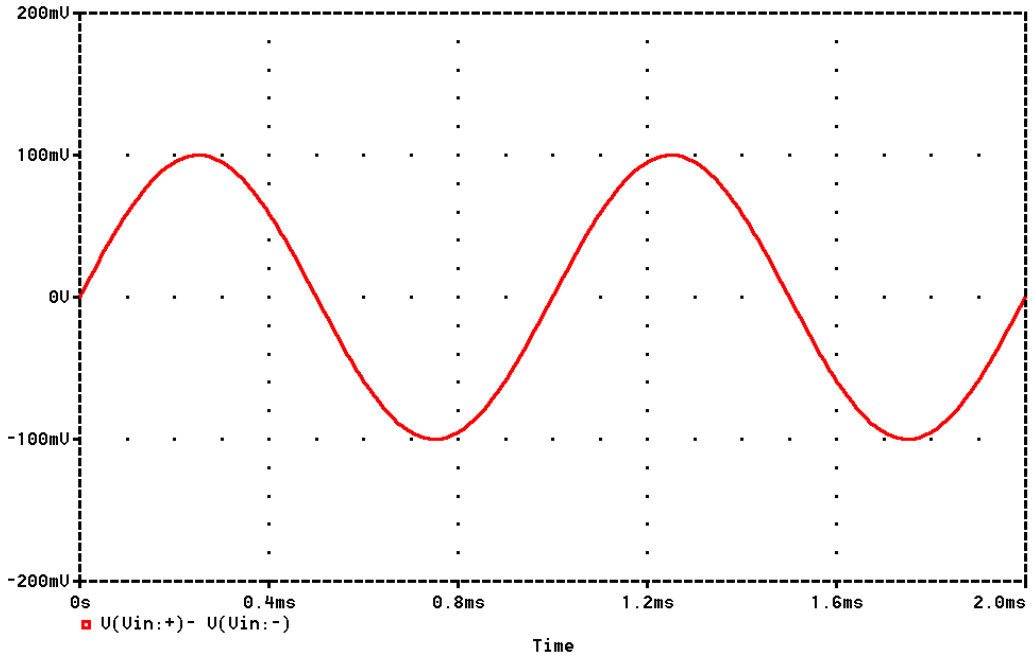

Fig. 162. Input waveform for the circuit of Fig. 159.

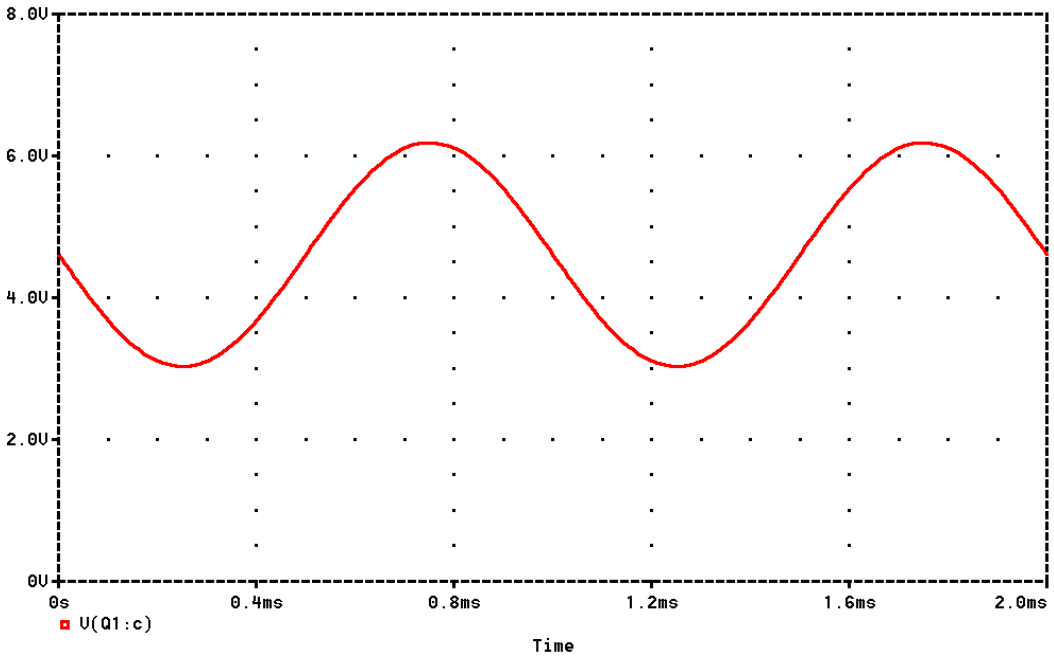

Fig. 163. Output (collector) waveform for the circuit of Fig. 159.

Basic FET Amplifier Structure

The basic FET amplifier takes the same form as the BJT amplifier. Let's go right to a PSpice simulation example using a 2N3819 *n*-channel JFET:

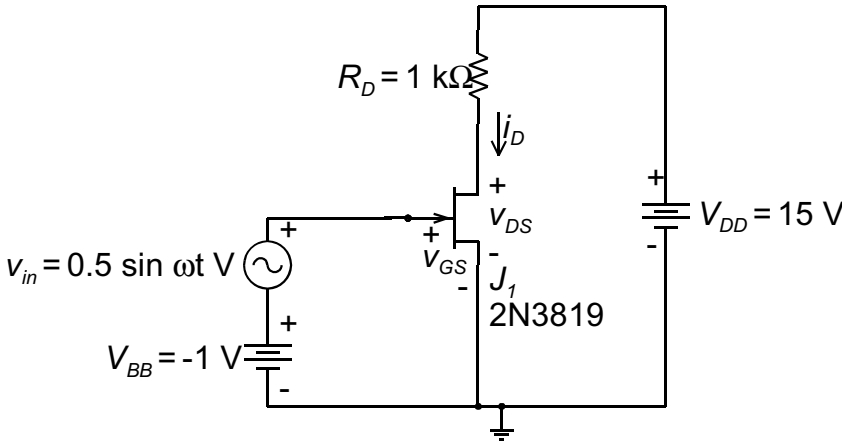

Fig. 164. Basic FET amplifier structure.

Now, KVL around the gate-source loop gives:

$$V_{GG} + v_{in} = v_{GS} \tag{125}$$

while KVL around the drain-source loop gives the familiar result:

$$V_{DD} = i_D R_D + v_{DS} \tag{126}$$

Because $i_G = 0$, the FET has no input characteristic, but we can plot the *transfer characteristic*, and use eq. (125) to add the appropriate load lines.

In this case, the load line locating the *Q* point, i.e., the line for $v_{in} = 0$, is called the *bias line*:

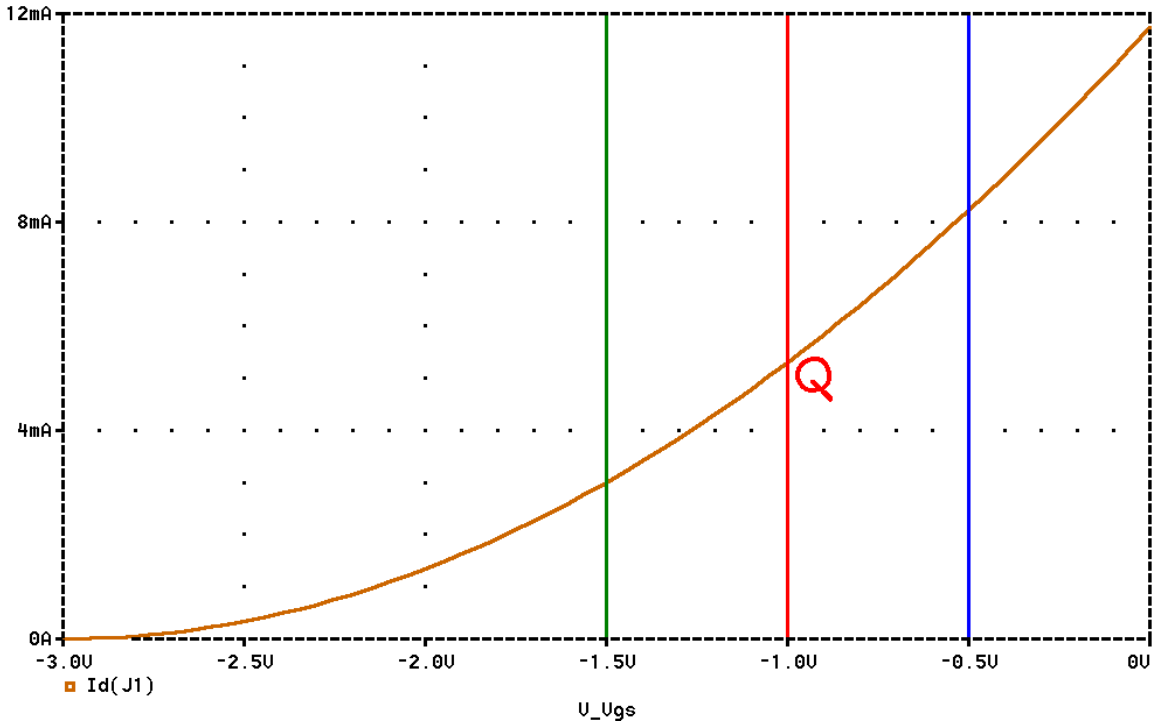

Fig. 165. PSpice-generated 2N3819 transfer characteristic showing the bias line, and lines for $v_{GS\,min}$ and $v_{GS\,max}$.

From the transfer characteristic, the indicated gate-source voltages correspond to the following drain current values:

$$v_{GS_{\min}} = -1.5\text{ V} \quad \Rightarrow \quad i_{D_{\min}} = 3.00\text{ mA} \tag{127}$$

$$V_{GSQ} = -1.0\text{ V} \quad \Rightarrow \quad I_{DQ} = 5.30\,\text{mA} \tag{128}$$

$$v_{GS_{\max}} = -0.5\text{ V} \quad \Rightarrow \quad i_{D_{\max}} = 8.22\,\text{mA} \tag{129}$$

Note, however, that we could have gone directly to the output characteristics, as the parameter for the family of output curves is v_{GS}:

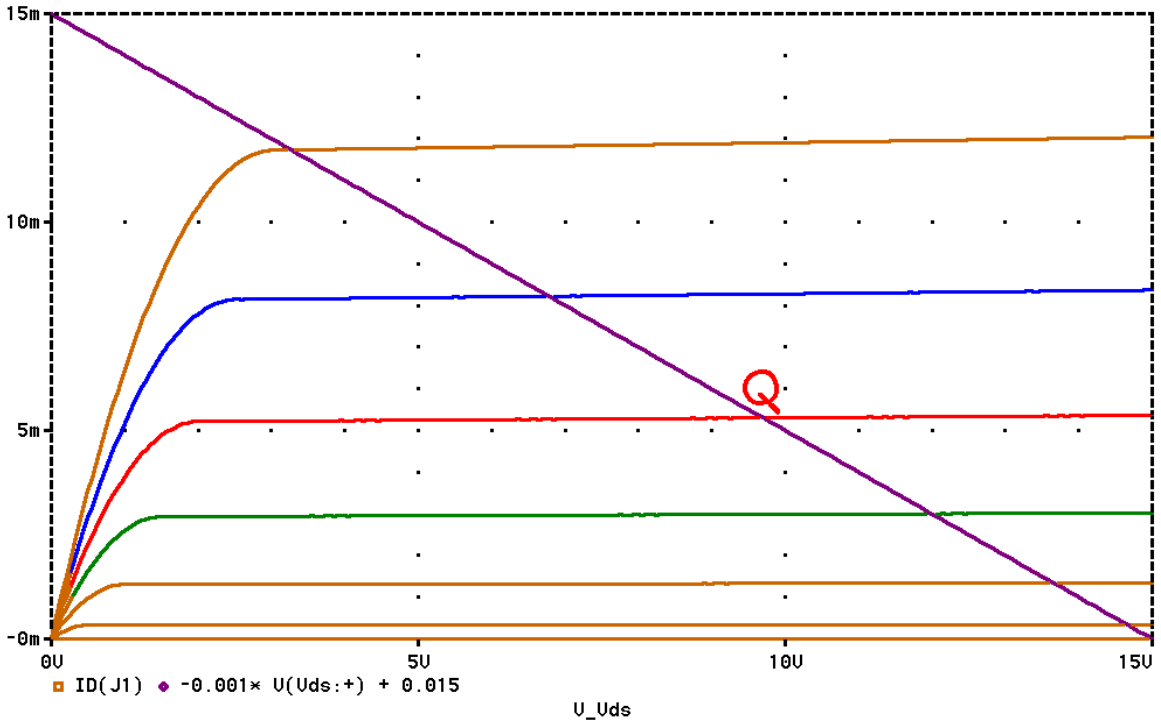

Fig. 166. 2N3819 output characteristics, with curves for gate-source voltages of (from bottom to top) -3 V, -2.5 V, -2 V, -1.5 V, -1 V, -0.5 V, and 0 V.

From the output characteristics and the drain-source load line, the indicated gate-source voltages correspond to the following drain-source voltage values:

$$v_{GS_{\min}} = -1.5\ \text{V} \quad \Rightarrow \quad v_{DS_{\max}} = 12.0\ \text{V} \tag{130}$$

$$V_{GSQ} = -1.0\ \text{V} \quad \Rightarrow \quad V_{DSQ} = 9.70\ \text{V} \tag{131}$$

$$v_{GS_{\max}} = -0.5\ \text{V} \quad \Rightarrow \quad v_{DS_{\min}} = 6.78\ \text{V} \tag{132}$$

Thus, using peak-to-peak values, we have a voltage gain of:

$$A_v = \frac{\Delta v_{DS}}{\Delta v_{GS}} = \frac{6.78\,\text{V} - 12.0\,\text{V}}{1\text{V}} = -5.22 \quad !!! \tag{133}$$

Amplifier Distortion

Let's look at the output waveform (v_{DS}) of the previous example:

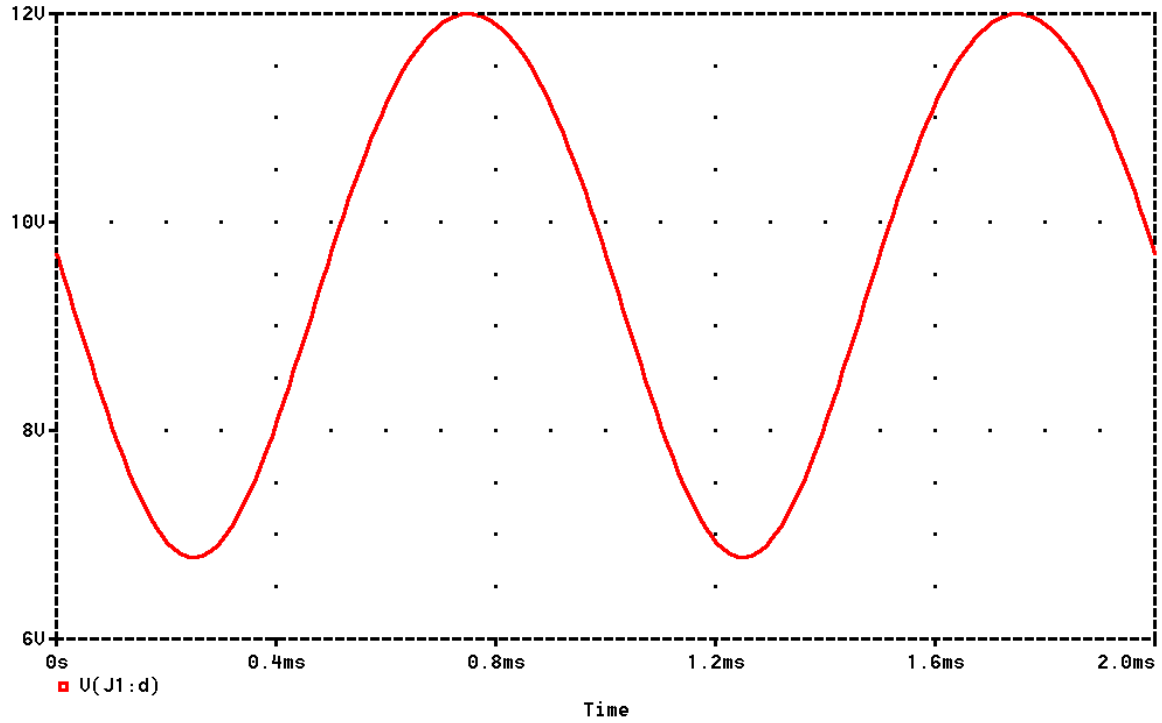

Fig. 167. Output (drain) waveform for the FET amplifier example.

Can you discern that the output sinusoid is distorted ?

The positive half-cycle has an amplitude of

$$12.0\ \text{V} - 9.70\ \text{V} = 2.30\ \text{V}$$

while the negative half cycle has an amplitude of

$$9.70\ \text{V} - 6.78\ \text{V} = 2.92\ \text{V}$$

This distortion results from the nonlinear (2^{nd}-order) transfer characteristic, the effects of which also can be seen in the nonuniform spacing of the family of output characteristics . . .

BJT's are also nonlinear, though less prominently so . . .

Distortion also results if the instantaneous operating point along the output-side load line ventures too close to the saturation or cutoff regions for the BJT (the triode or cutoff regions for the FET), as the following example illustrates:

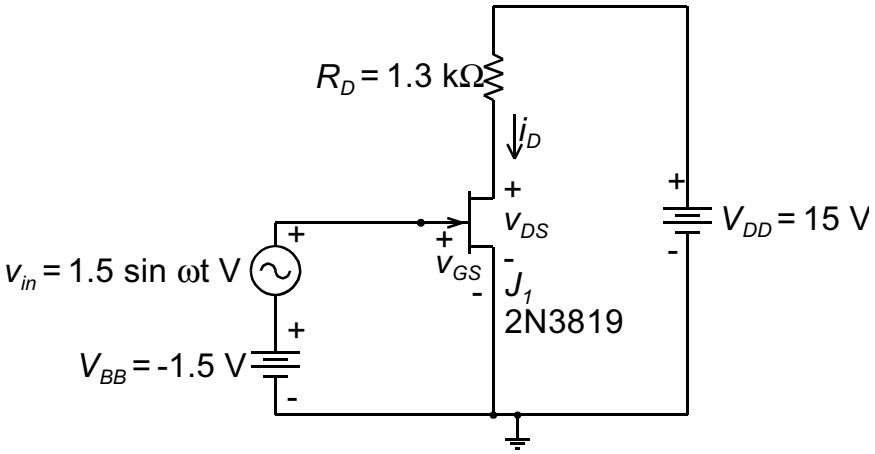

Fig. 168. Slight changes to the FET amplifier example to illustrate nonlinear distortion.

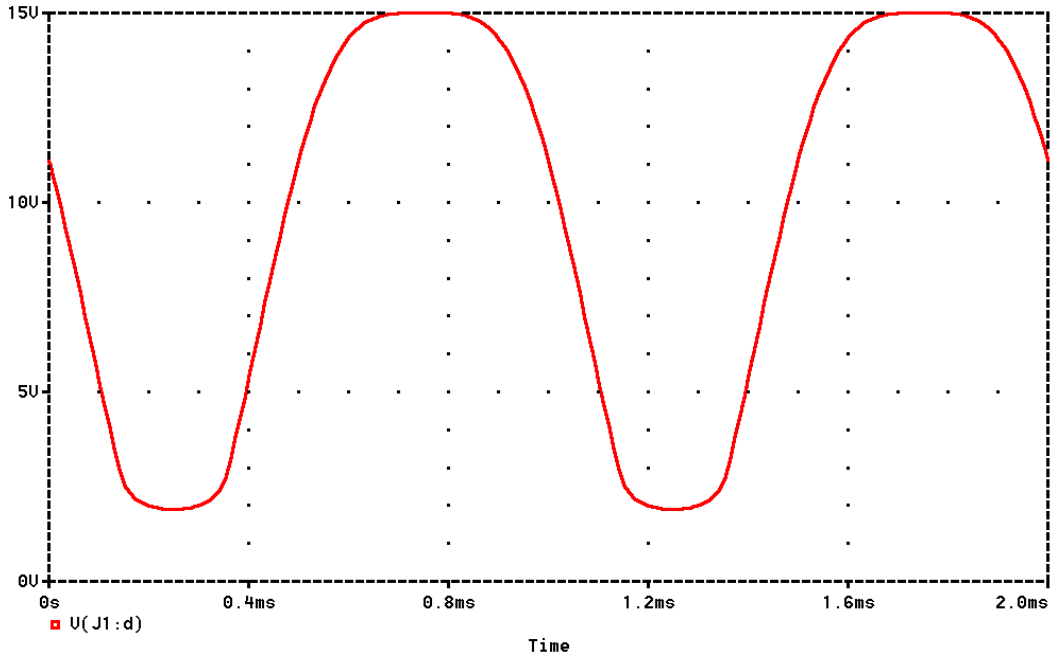

Fig. 169. Severely distorted output waveform resulting from operation in the cutoff region (top) and the triode region (bottom).

Biasing and Bias Stability

Notice from the previous load line examples:

- The instantaneous operating point moves with instantaneous signal voltage.

  Linearity is best when operating point stays within the active (BJTs) or pinch-off (FETs) regions.

- The quiescent point is the dc (zero signal) operating point.

  It lies near the "middle" of the range of instantaneous operating points.

  This dc operating point is *required* if linear amplification is to be achieved *!!!*

- The dc operating point (the *quiescent point*, the *Q point*, the *bias point*) obviously requires that dc sources be in the circuit.

- The process of establishing an appropriate bias point is called *biasing* the transistor.

- Given a specific type of transistor, biasing should result in the same or nearly the same bias point in every transistor of that type . . . this is called *bias stability*.

  Bias stability can also mean stability with temperature, with aging, etc.

We study BJT and FET bias circuits in the following pages . . .

Biasing BJTs - The Fixed Bias Circuit

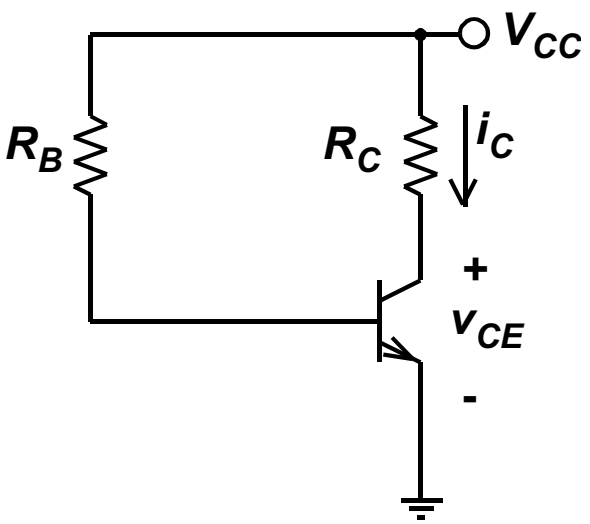

Fig. 170. BJT fixed bias circuit.

Example

We let V_{CC} = 15 V,

R_B = 200 kΩ, and R_C = 1 kΩ

β varies from 100 to 300

To perform the analysis, we assume that operation is in the active region, and that V_{BE} = 0.7 V.

For β = 100:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{15\,\text{V} - 0.7\,\text{V}}{200\,\text{k}\Omega} = 71.5\,\mu\text{A} \quad \textbf{(134)}$$

$$I_C = \beta I_B = 7.15\,\text{mA} \quad \Rightarrow \quad V_{CE} = V_{CC} - I_C R_C = 7.85\,\text{V} \quad \textbf{(135)}$$

Q. Active region??? A. $V_{CE} > 0.7$ V and $I_B > 0 \Rightarrow$ *Yes!!!*

For β = 300:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{15\,\text{V} - 0.7\,\text{V}}{200\,\text{k}\Omega} = 71.5\,\mu\text{A} \quad \textbf{(136)}$$

$$I_C = \beta I_B = 21.5\,\text{mA} \quad \Rightarrow \quad V_{CE} = V_{CC} - I_C R_C = -6.45\,\text{V} \quad \textbf{(137)}$$

Q. Active region? A. $V_{CE} < 0.7$ V $\Rightarrow$ ***No!!! Saturation!!!***

Thus our calculations for β = 300 are incorrect, but more importantly we conclude that fixed bias provides *extremely poor bias stability!!!*

Biasing BJTs - The Constant Base Bias Circuit

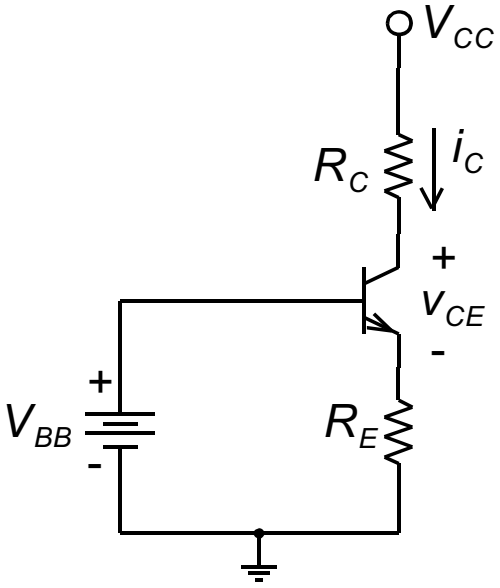

Fig. 171. BJT constant base bias circuit.

Example

Now we let V_{CC} = 15 V and V_{BB} = 5 V

R_C = 2 kΩ and R_E = 2 kΩ

β varies from 100 to 300

And we assume operation in active region and V_{BE} = 0.7 V, as before.

Though not explicitly shown here, the active-region assumption must always be verified.

For β = 100:

$$I_E = \frac{V_{BB} - V_{BE}}{R_E} = 2.15\ \text{mA} \quad \Rightarrow \quad I_C = \frac{\beta}{\beta + 1} I_E = 2.13\ \text{mA} \tag{138}$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E = 6.44\ \text{V} \tag{139}$$

For β = 300:

$$I_E = \frac{V_{BB} - V_{BE}}{R_E} = 2.15\ \text{mA} \quad \Rightarrow \quad I_C = \frac{\beta}{\beta + 1} I_E = 2.14\ \text{mA} \tag{140}$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E = 6.41\ \text{V} \tag{141}$$

Thus we conclude that *constant base bias provides excellent bias stability!!!* Unfortunately, we can't easily couple a signal into this circuit, so it is not as useful as it may first appear.

Biasing BJTs - The Four-Resistor Bias Circuit

Introduction

This combines features of fixed bias and constant base bias, but it takes a circuit-analysis "trick" to see that:

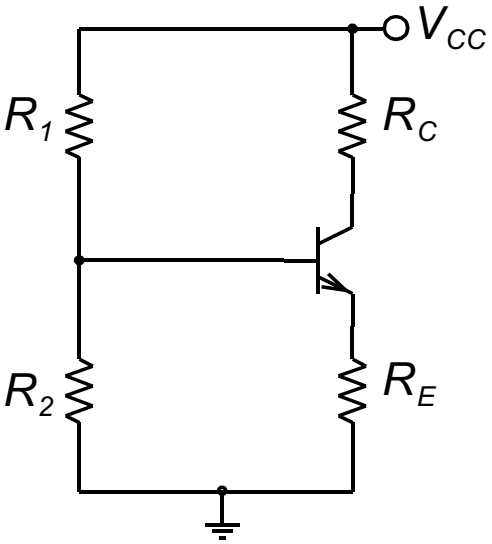

Fig. 172. The four-resistor bias circuit.

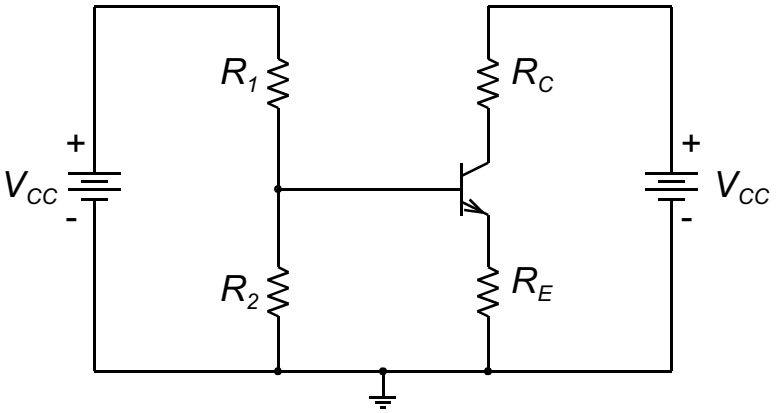

Fig. 173. Equivalent after "trick" with supply voltage.

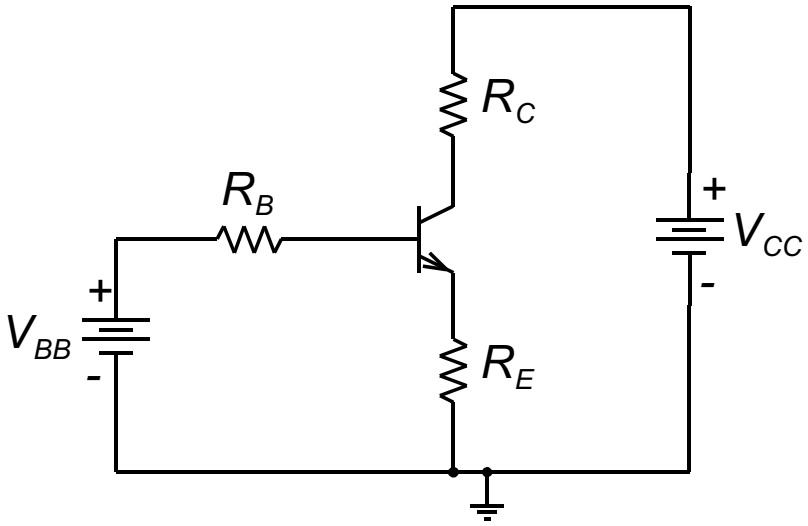

Fig. 174. Final equivalent after using Thevenin's Theorem on base divider.

Circuit Analysis

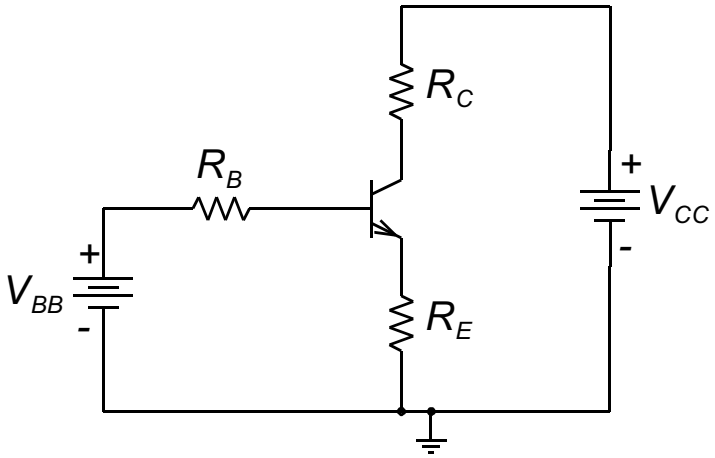

Fig. 175. Four-resistor bias circuit equivalent (Fig. 174 repeated).

Analysis begins with KVL around b-e loop:

$$V_{BB} = I_B R_B + V_{BE} + I_E R_E \tag{142}$$

But in the active region $I_E = (\beta + 1) I_B$:

$$V_{BB} = I_B R_B + V_{BE} + (\beta + 1) I_B R_E \tag{143}$$

Now we solve for I_B:

$$I_B = \frac{V_{BB} - V_{BE}}{R_B + (\beta + 1) R_E} \tag{144}$$

And multiply both sides by β:

$$\beta I_B = I_C = \frac{\beta (V_{BB} - V_{BE})}{R_B + (\beta + 1) R_E} \tag{145}$$

We complete the analysis with KVL around c-e loop:

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E \tag{146}$$

Bias Stability

Bias stability can be illustrated with eq. (145), repeated below:

$$\beta I_B = I_C = \frac{\beta(V_{BB} - V_{BE})}{R_B + (\beta + 1)R_E} \qquad \textbf{(147)}$$

Notice that if R_E = 0 we have *fixed bias*, while if R_B = 0 we have *constant base bias*.

To maximize bias stability:

- We minimize variations in I_C with changes in β . . .

  By letting $(\beta + 1)R_E >> R_B$,

  Because then β and $(\beta + 1)$ nearly cancel in eq. (147).

  Rule of Thumb: let $(\beta + 1)R_E \approx 10\ R_B$

  Equivalent Rule: let $I_{R_2} \approx 10 I_{B_{max}}$

  } $\beta = 100$

- We also minimize variations in I_C with changes in V_{BE} . . .

  By letting $V_{BB} >> V_{BE}$.

  Rule of Thumb: let $V_{R_C} \approx V_{CE} \approx V_{R_E} \approx \frac{1}{3} V_{CC}$

  Because $V_{R_E} \approx V_{BB}$ if V_{BE} and I_B are small.

Example

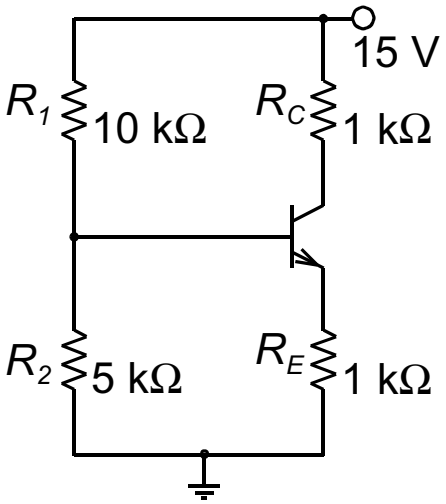

Fig. 176. Example circuit.

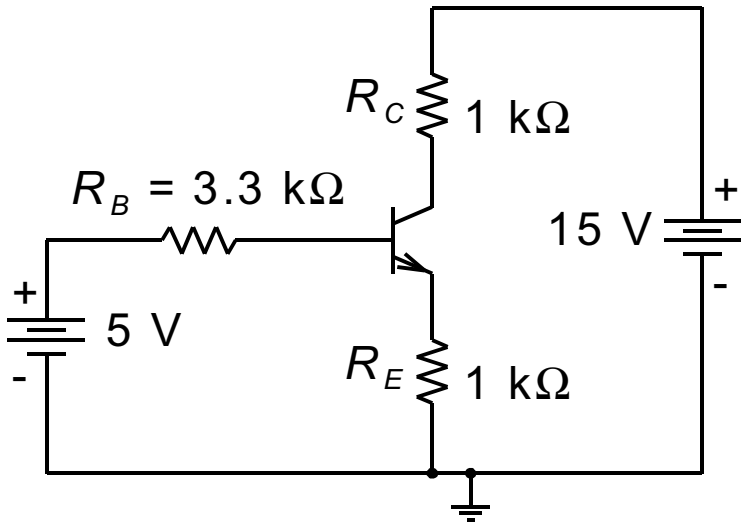

Fig. 177. Equivalent circuit.

For $\beta = 100$ (and $V_{BE} = 0.7$ V):

$$I_B = \frac{V_{BB} - V_{BE}}{R_B + (\beta + 1)R_E} = 41.2\ \mu\text{A} \quad \Rightarrow \quad I_C = \beta I_B = 4.12\ \text{mA} \tag{148}$$

$$\Rightarrow \quad I_E = \frac{I_C}{\alpha} = 4.16\ \text{mA} \quad \Rightarrow \quad V_{CE} = V_{CC} - I_C R_C - I_E R_E = 6.72\ \text{V} \tag{149}$$

For $\beta = 300$:

$$I_B = \frac{V_{BB} - V_{BE}}{R_B + (\beta + 1)R_E} = 14.1\ \mu\text{A} \quad \Rightarrow \quad I_C = \beta I_B = 4.24\ \text{mA} \tag{150}$$

$$\Rightarrow \quad I_E = \frac{I_C}{\alpha} = 4.25\ \text{mA} \quad \Rightarrow \quad V_{CE} = V_{CC} - I_C R_C - I_E R_E = 6.50\ \text{V} \tag{151}$$

Thus we have achieved a reasonable degree of bias stability.

Biasing FETs - The Fixed Bias Circuit

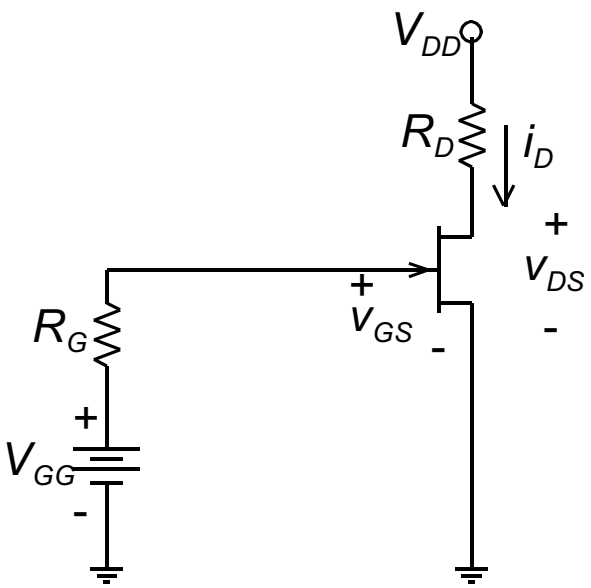

Fig. 178. FET fixed bias circuit.

Just as the BJT parameters b and V_{BE} vary from device to device, so do the FET parameters K and V_P (or V_{TH}).

Thus, bias circuits must provide *bias stability*, i.e., a reasonably constant I_{DQ}.

We look first at the fixed bias circuit shown at left, and note that $V_{GG} = v_{GSQ}$.

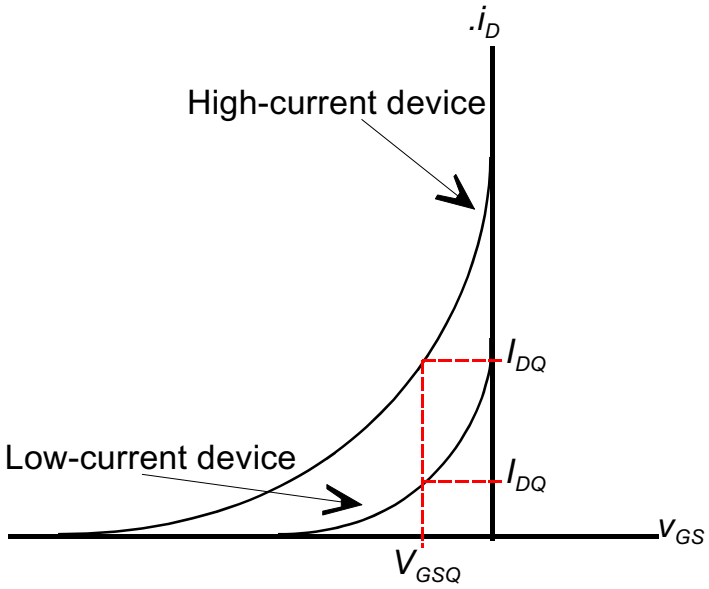

Fig. 179. Graphical illustration of fixed bias using an *n*-channel JFET.

For an n-channel JFET, note that V_{GG} must be < 0, which requires a second power supply.

For an n-ch. depl. MOSFET, V_{GG} can be either positive or negative.

For an n-ch. enh. MOSFET, V_{GG} must be > 0

Finally, note the complete lack of bias stability. *Fixed bias is not practical!!!*

Biasing FETs - The Self Bias Circuit

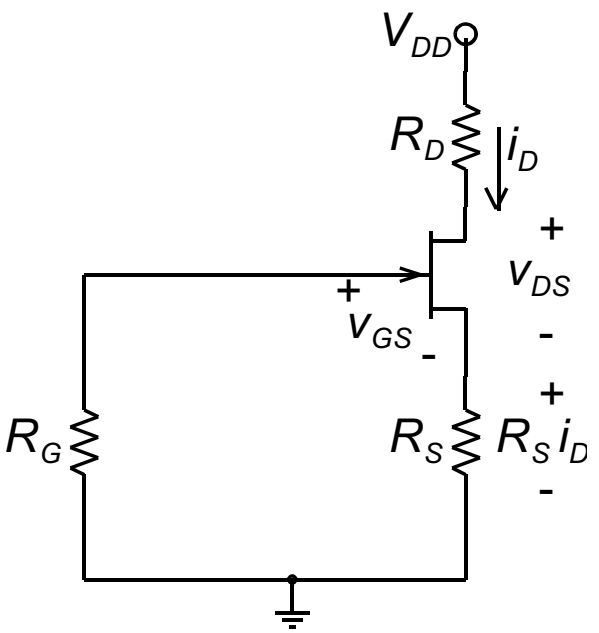

Fig. 180. FET self-bias circuit.

From a KVL equation around the gate-source loop we obtain the *bias line*:

$$v_{GS} = -i_D R_S \qquad \textbf{(152)}$$

And, assuming operation in the pinch-off region:

$$i_D = K\left(v_{GS} - V_P\right)^2 \qquad \textbf{(153)}$$

Solving simultaneously provides the *Q point.* A graphical solution is shown, below left.

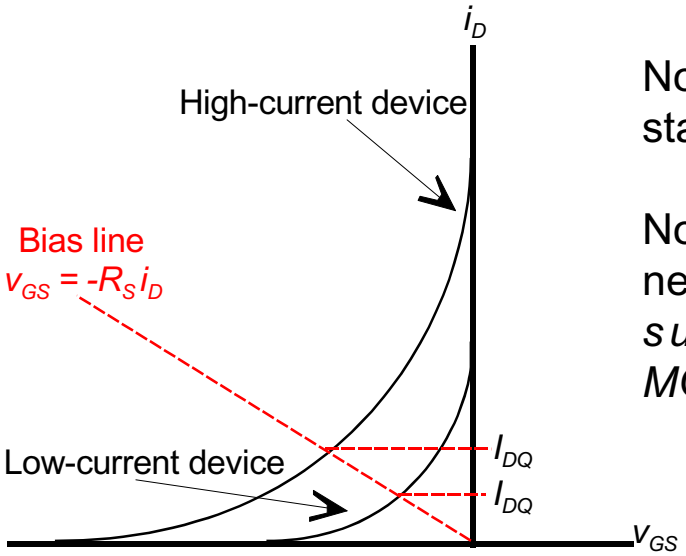

Fig. 181. Graphical solution to self-bias circuit, showing improved stability.

Note the improvement in bias stability over a fixed bias approach.

Note also that V_{GSQ} can only be negative. *Thus, self-bias is not suitable for enhancement MOSFETs!*

An analytical solution requires the quadratic formula (though a good guess often works) - the higher current solution is invalid (*why?*).

Biasing FETs - The Fixed + Self Bias Circuit

This is just the four-resistor bias circuit with a different name*!!!*

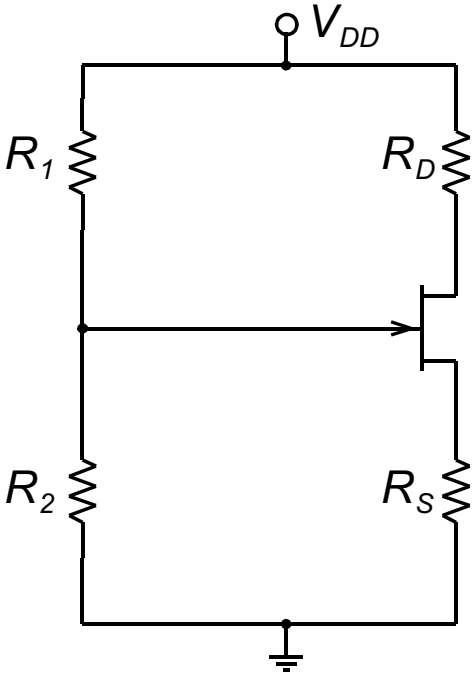

Fig. 182. Fixed + self-bias circuit for FETs.

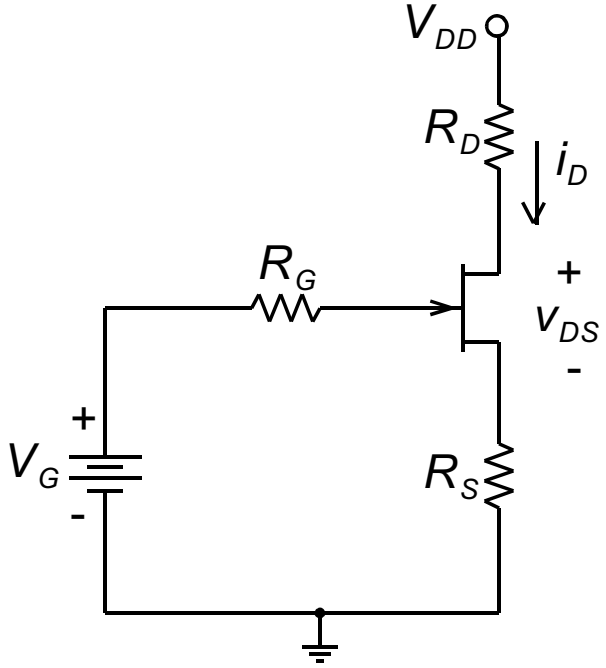

Fig. 183. Equivalent circuit after using Thevenin's Theorem on gate divider.

A KVL equation around gate-source loop provides the *bias line*:

$$v_{GS} = V_G - i_D R_S \tag{154}$$

And, as usual, assuming operation in the pinch-off region:

$$i_D = K\left(v_{GS} - V_P\right)^2 \tag{155}$$

Simultaneous solution provides *Q*-point - see next page.

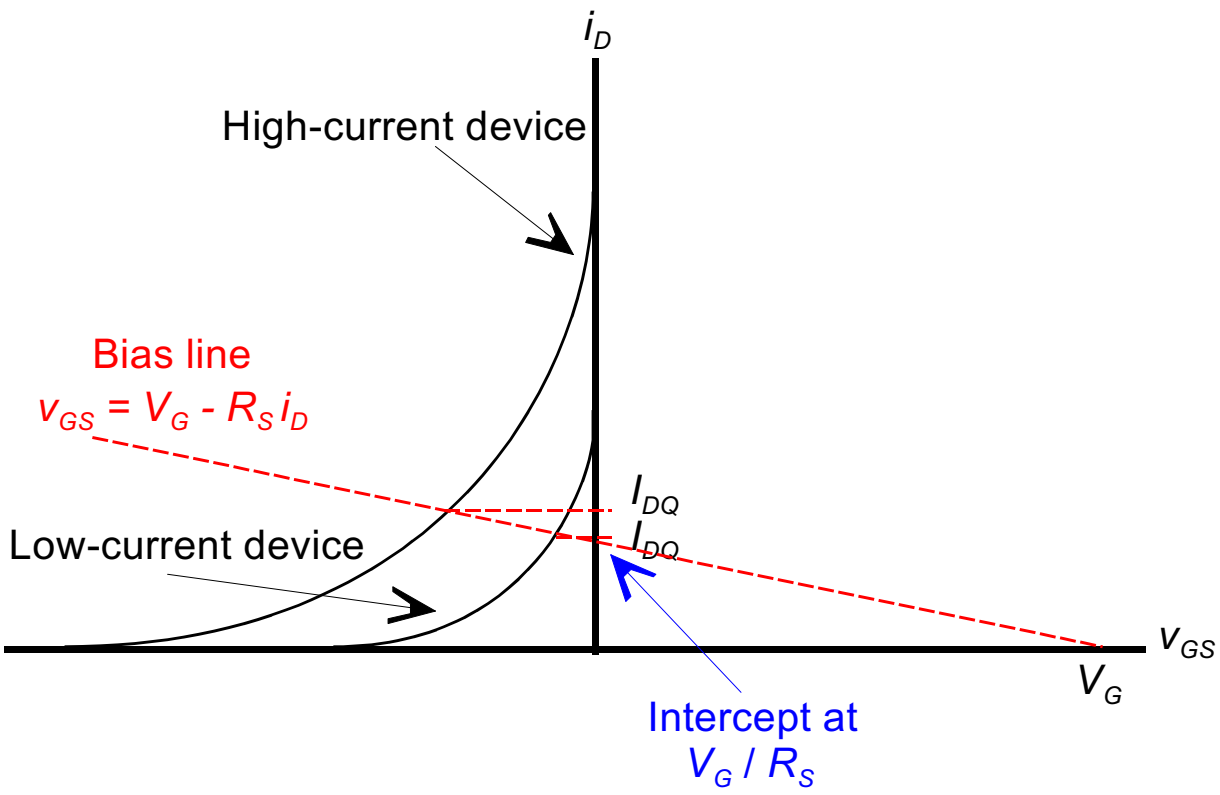

Fig. 184. Graphical solution to fixed + self bias circuit.

- Note that bias stability can be much improved over that obtained with self-bias.

  The degree of stability increases as V_G or R_S increases.

  Rule of thumb: let $V_{R_D} = V_{DS} = V_{R_S} = \frac{1}{3} V_{DD}$

- Other considerations:

  Because $I_G = 0$, R_1 and R_2 can be very large (e.g., MΩ).

  Because V_G can be > 0, this circuit can be used with any FET, including enhancement MOSFETs.

Design of Discrete BJT Bias Circuits

In the next few sections we shall look at biasing circuits in somewhat greater detail.

Concepts of Biasing

We want *bias stability* because we generally desire to keep the *Q*-point within some region:

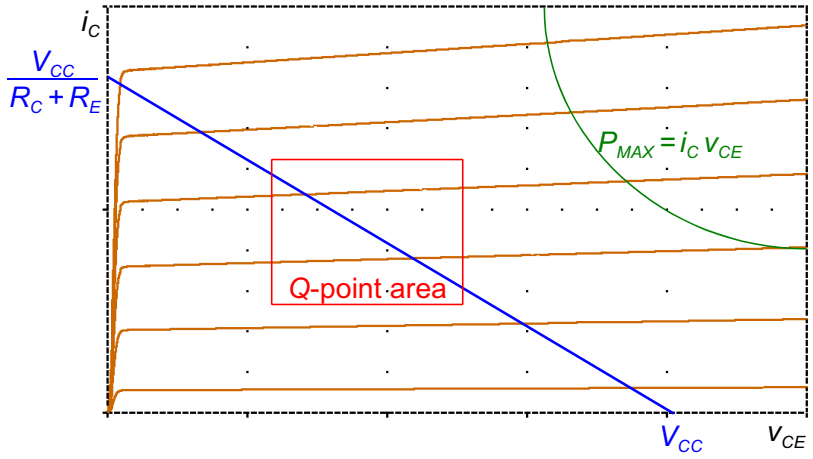

Fig. 185. Typical BJT output characteristics.

In addition to voltage gain, we must consider and compromise among the following:

- *Signal Swing*: If V_{CEQ} is too small the device will saturate. If I_{CQ} is too small the device will cut off.
- *Power Dissipation*: V_{CEQ} and I_{CQ} must be below certain limits.
- *Input Impedance*: We can increase Z_{in} with high R values.
- *Output Impedance*: We can decrease Z_{out} with low R values.
- *Bias Stability*: We can increase stability with low R values.
- *Frequency Response*: A higher V_{CEQ} lowers junction C and improves response. A specific I_{CQ} maximizes f_t.

Design of the Four-Resistor BJT Bias Circuit

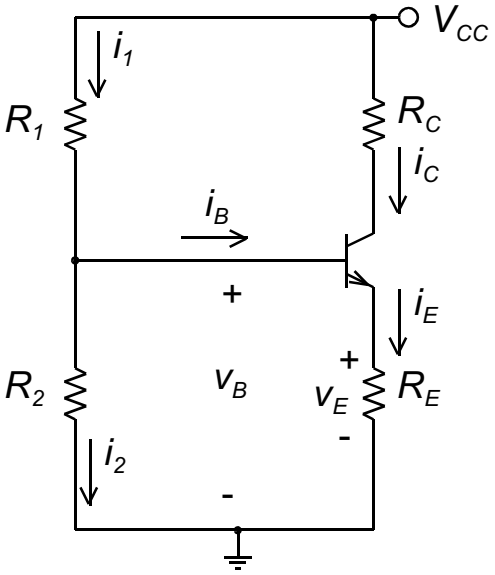

Fig. 186. Four-resistor bias circuit, revisited.

We begin where we are most familiar, by revisiting the four-resistor bias circuit.

Assume that I_{CQ}, V_{BEQ}, V_{CC}, β_{min} and β_{max} are known. This amounts to little more than having chosen the device and the *Q*-point.

Now, recall this result from a KVL equation around the base-emitter loop:

$$I_{CQ} = \frac{\beta\left(V_{BB} - V_{BEQ}\right)}{R_B + \left(\beta + 1\right)R_E} \qquad \textbf{(156)}$$

Design Procedure

- First, we decide how V_{CC} divides among V_{R_C}, V_{CE}, V_E. For temperature stability we want V_E >> temperature variation in V_{BE}. Recall the "one-third" rule of thumb. Then:

$$R_C = \frac{V_{R_C}}{I_{CQ}} \quad \text{and} \quad R_E = \frac{V_E}{I_{EQ}} \approx \frac{V_E}{I_{CQ}} \qquad \textbf{(157)}$$

- Then we choose I_2 (larger $I_2 \Rightarrow$ lower $R_B \Rightarrow$ better bias stability $\Rightarrow$ lower Z_{in}).

  Recall the rule of thumb: $I_2 = 10\, I_{BQ\,max}$. Then:

$$R_2 = \frac{V_E + V_{BEQ}}{I_2} \quad \text{and} \quad R_1 = \frac{V_{CC} - \left(V_E + V_{BEQ}\right)}{I_2 + I_{BQ}} \qquad \textbf{(158)}$$

Design of the Dual-Supply BJT Bias Circuit

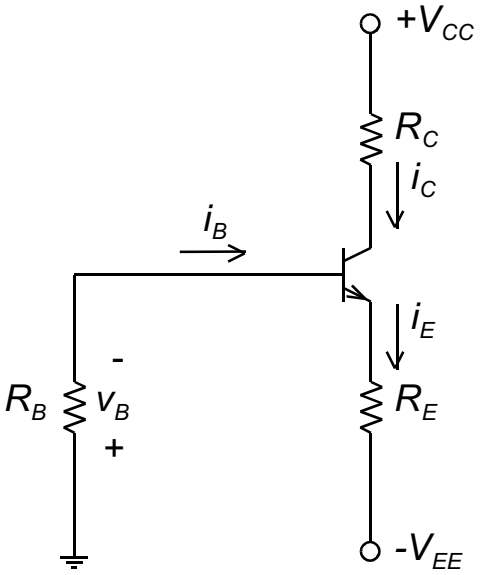

Fig. 187. Dual-supply bias ckt.

This is essentially the same as the four-resistor bias circuit. Only the reference point (ground) has changed.

We begin with the same assumptions as for the previous circuit.

Because its important that you *understand the principles* used to obtain these equations, verify that the following results from a KVL equation around the base-emitter loop:

$$I_{CQ} = \frac{\beta(V_{EE} - V_{BEQ})}{R_B + (\beta + 1)R_E} \qquad \textbf{(159)}$$

Design Procedure

- Allocate a fraction of V_{EE} for V_B. For bias stability we would like the voltage across R_E to be << $|V_B|$ (i.e., $R_B << \beta R_E$).

  A starting point, i.e., a rule of thumb is $|V_B| = V_{EE} / 20$. Then:

$$R_B = \frac{V_{;B}}{I_{BQ}} = \frac{\beta V_B}{I_{CQ}} \quad \text{and} \quad R_E \approx \frac{V_{EE} - V_B - V_{BEQ}}{I_{CQ}} \qquad \textbf{(160)}$$

- Choose V_{CEQ}. Here a rule of thumb is: $V_{CEQ} \approx V_{CC}/2$. Then:

$$R_C = \frac{V_{CC} - V_{CEQ} - \left[-\left(V_B + V_{BEQ}\right)\right]}{I_{CQ}} = \frac{V_{CC} - V_{CEQ} + V_B + V_{BEQ}}{I_{CQ}} \qquad \textbf{(161)}$$

Note: Smaller $V_{CEQ} \Rightarrow$ larger $R_C \Rightarrow$ larger $A_v \Rightarrow$ larger Z_{out}

Design of the Grounded-Emitter BJT Bias Circuit

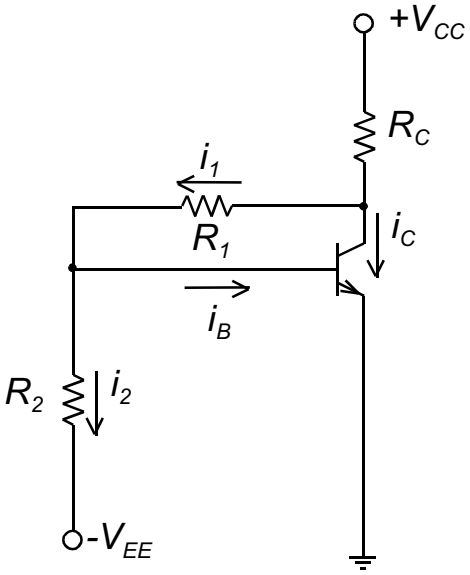

Fig. 188. Grounded-emitter bias circuit.

Grounding the emitter directly lowers inductance in the emitter lead, which increases high-frequency gain.

Bias stability is obtained by connecting base to collector through R_1.

Verifying this approximate equation is difficult; a derivation is provided on the following pages:

$$I_{CQ} \approx \frac{\beta\left[V_{CC} - \frac{R_1}{R_2}\left(V_{EE} + V_{BEQ}\right)\right]}{R_1 + \beta R_C} \qquad \textbf{(162)}$$

Design Procedure

- Allocate V_{CC} between V_{Rc} and V_{CEQ}. With supply voltage split between only two elements the rule of thumb becomes:

$$V_{CEQ} \approx V_{CC}/2 \qquad \textbf{(163)}$$

- Choose I_2. To have $R_1 << \beta R_C$, we want $I_2 >> I_B$. The rule of thumb is:

$$I_2 \approx 10 I_{BQ\,\max} \qquad \textbf{(164)}$$

- Then:

$$R_2 = \frac{V_{EE} + V_{BEQ}}{I_2} \qquad R_1 = \frac{V_{CEQ} - V_{BEQ}}{I_2 + I_{BQ}} \qquad R_C = \frac{V_{CC} - V_{VEQ}}{I_{CQ} + I_1} \qquad \textbf{(165)}$$

Analysis of the Grounded-Emitter BJT Bias Circuit

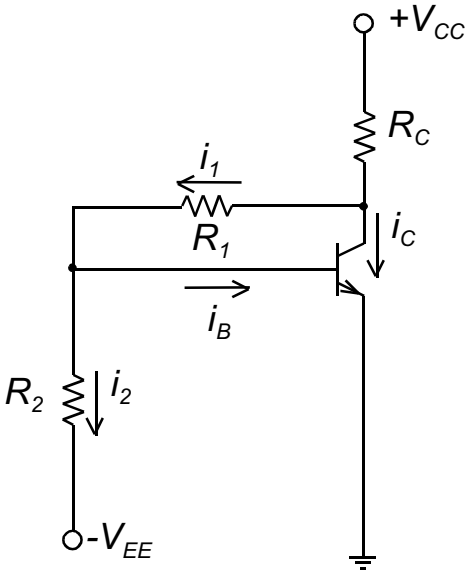

Fig. 189. Grounded-emitter bias circuit (Fig. 188 repeated).

Q. How do we obtain this equation?

$$I_{CQ} \approx \frac{\beta\left[V_{CC} - \frac{R_1}{R_2}\left(V_{EE} + V_{BEQ}\right)\right]}{R_1 + \beta R_C} \quad \textbf{(166)}$$

A. We begin by noting that :

$$I_1 = I_2 + I_B \quad \textbf{(167)}$$

and

$$I_{R_C} = I_1 + I_C = I_2 + (\beta + 1)I_B \quad \textbf{(168)}$$

Then we find I_2 with a KVL equation around the base-emitter loop:

$$I_2 = \frac{V_{EE} + V_{BEQ}}{R_2} \quad \textbf{(169)}$$

Now we sum voltage rises from ground to V_{CC}:

$$V_{CC} = V_{BEQ} + (I_2 + I_B)R_1 + \left[I_2 + (\beta + 1)I_B\right]R_C \quad \textbf{(170)}$$

Substituting (169) into (170):

$$V_{CC} = V_{BEQ} + \frac{R_1}{R_2}\left(V_{EE} + V_{BEQ}\right) + I_B R_1 + \frac{R_C}{R_2}\left(V_{EE} + V_{BEQ}\right) + (\beta + 1)I_B R_C \quad \textbf{(171)}$$

Repeating eq. (171) from the bottom of the previous page:

$$V_{CC} = V_{BEQ} + \frac{R_1}{R_2}\left(V_{EE} + V_{BEQ}\right) + I_B R_1 + \frac{R_C}{R_2}\left(V_{EE} + V_{BEQ}\right) + \left(\beta + 1\right) I_B R_C \quad \textbf{(172)}$$

The next step is to collect terms:

$$V_{CC} - V_{BEQ} - \frac{R_1}{R_2}\left(V_{EE} + V_{BEQ}\right) - \frac{R_C}{R_2}\left(V_{EE} + V_{BEQ}\right) = I_B\left[R_1 + \left(\beta + 1\right) R_C\right] \quad \textbf{(173)}$$

Finally, if we apply the following approximations:

$$V_{CC} - V_{BEQ} \approx V_{CC} \qquad R_C / R_2 \approx 0 \qquad \beta + 1 \approx \beta$$

we obtain our objective, the original approximation:

$$I_{CQ} = \frac{\beta\left[V_{CC} - \frac{R_1}{R_2}\left(V_{EE} + V_{BEQ}\right)\right]}{R_1 + \beta R_C} \quad \textbf{(174)}$$

Bipolar IC Bias Circuits

Introduction

Integrated circuits present special problems that must be considered before circuit designs are undertaken.

For our purposes here, the most important consideration is *real estate*. Space on an IC wafer is at a premium. *Anything* that takes up too much space is a liability. Consider the following:

- *Resistors* are very inefficient when it comes to real estate. The area required is directly proportional to the value of resistance (remember $R = \rho L / A$?).

  As a result, use of resistances in ICs is avoided, if possible. And resistances greater than 100 kΩ are extremely rare.

  When used, it is quite difficult to control resistance values with accuracy unless each resistor is laser-trimmed. Tolerances are as large as 50% are not unusual.

  Because all resistors are fabricated at the same time, all resistors are "off" by the same amount. This means that resistors that are intended to be equal will essentially be equal.

- *Capacitors* are also liabilities. Capacitance values greater than 100 pF are virtually unheard of.

- *Inductors* only recently became integrable. Their use is quite limited.

- *BJTs* are *very* efficient. And while β values suffer the same 3:1 to 5:1 variation found in discrete transistors, *all BJTs on an IC wafer are essentially identical* (if intended to be).

This latter point is most important, and drives *all* IC circuit design. We begin to examine this on the following pages.

The Diode-Biased Current Mirror

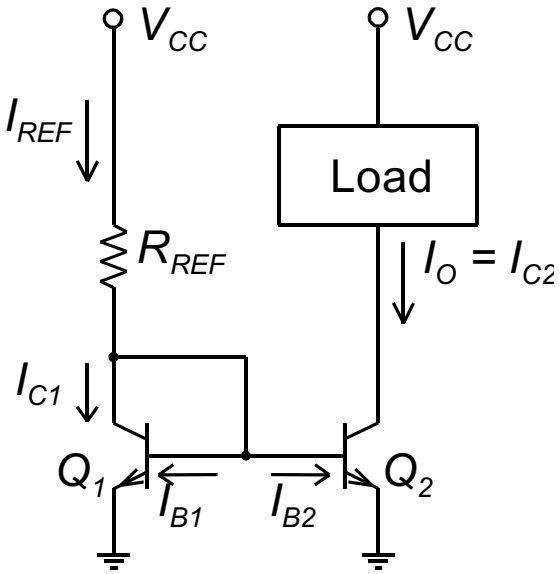

Fig. 190. Diode-biased current mirror.

Current Ratio:

This is the most simple of all IC bias circuit techniques.

The key here is that the BJTs are identical !!! Because $V_{BE1} = V_{BE2}$, this means that $I_{B1} = I_{B2} = I_B$.

Note that $V_{CB1} = 0$, thus Q_1 is *active* (at the edge of saturation).

If we assume Q_2 is also active, we have $I_{C1} = I_{C2} = I_C$.

From this point the analysis proceeds straightforwardly . . .

$$I_O = I_{C2} = I_{C1} = I_C = \beta I_B \tag{175}$$

And from a KCL equation at the collector of Q_1:

$$I_{REF} = I_{C1} + I_{B1} + I_{B2} = \beta I_B + 2I_B = (\beta + 2)I_B \tag{176}$$

Dividing (175) by (176):

$$\frac{I_O}{I_{REF}} = \frac{\beta I_B}{(\beta + 2)I_B} = \frac{\beta}{\beta + 2} = \frac{1}{1 + \frac{2}{\beta}} \tag{177}$$

Thus, *as long as Q_2 remains active*, for large β, $I_O \approx I_{REF}$, i.e., I_O reflects the current I_{REF} (hence "mirror"), *regardless of the load!!!*

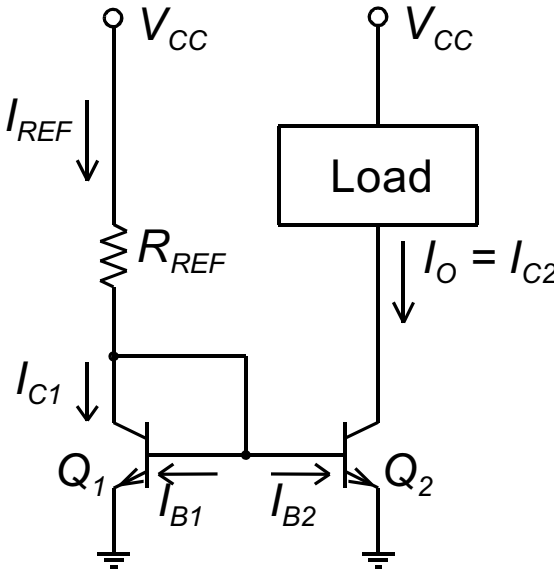

Fig. 191. Diode-biased current mirror (Fig. 190 repeated.

Reference Current:

I_{REF} is set easily, by choosing R_{REF}:

$$I_{REF} = \frac{V_{CC} - V_{BE}}{R_{REF}} \approx \frac{V_{CC} - 0.7\,\text{V}}{R_{REF}} \quad \textbf{(178)}$$

Output Resistance:

Finally, the output resistance seen by the load is just the output resistance of Q_2:

$$r_o = \left[\frac{\partial i_{C2}}{\partial v_{CE2}}\right]^{-1} \quad \textbf{(179)}$$

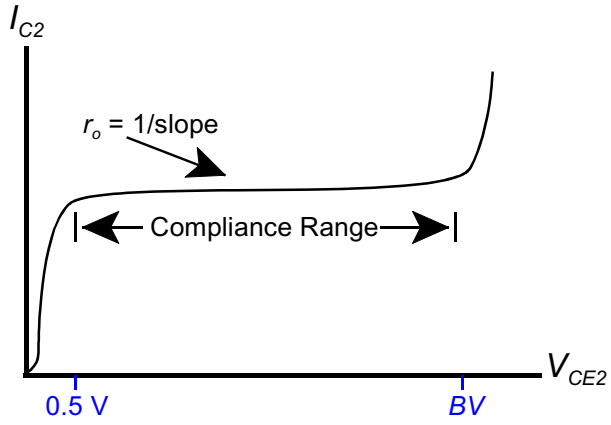

Fig. 193. Example of the compliance range of a current mirror. The diode-biased mirror is represented in this figure.

Compliance Range

This is defined as the range of voltages over which the mirror circuit functions as intended.

For the diode-biased mirror, this is the range where Q_2 remains active.

Using a Mirror to Bias an Amplifier

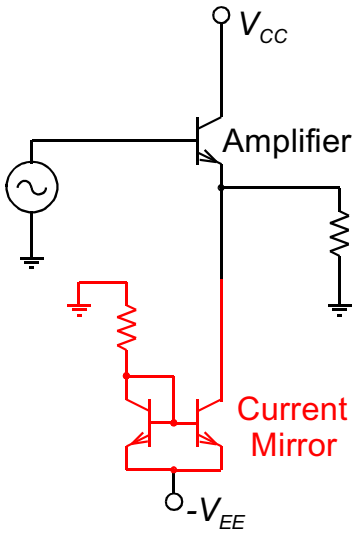

Fig. 194. Follower biased with a current nirror.

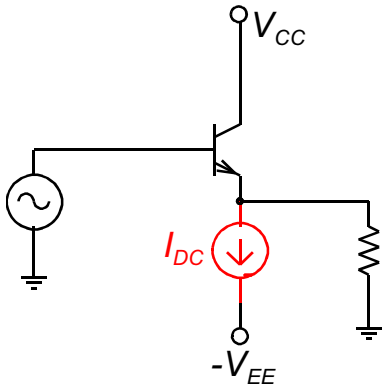

Fig. 195. Representation of the mirror circuit of Fig. 194.

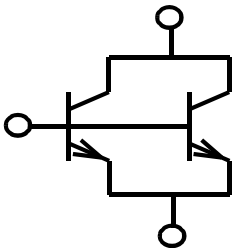

Fig. 192.

Changing transistor areas gives mirror ratios other than unity, which is useful to obtain small currents without using large *R* values. The schematic technique used to show integer ratios other than unity is shown.

Wilson Current Mirror

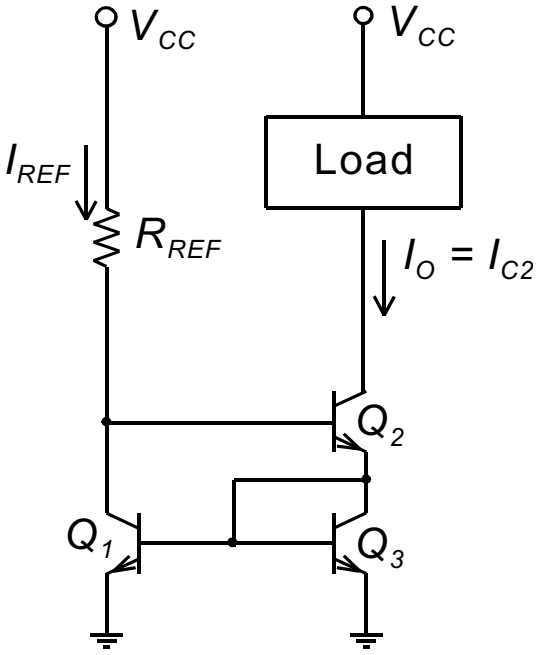

Fig. 196. Wilson current mirror.

Current Ratio:

The addition of another transistor creates a mirror with an output resistance of $\approx \beta r_{o2}$ (*very large!!!*)

Because $V_{BE1} = V_{BE3}$ we know that $I_{B1} = I_{B3} = I_B$.

Because $V_{CB3} = 0$, Q_3 is *active*.

Because $V_{CB1} = V_{BE2}$, Q_1 is active.

Thus we know that $I_{C1} = I_{C3} = \beta I_B$.

We assume also that Q_2 is active.

We proceed with the mathematical derivation without further comment.

$$I_{E2} = I_{C3} + 2I_B = (\beta + 2)I_B \tag{180}$$

$$I_O = I_{C2} = \frac{\beta}{\beta + 1} I_{E2} = \frac{\beta(\beta + 2)}{\beta + 1} I_B \tag{181}$$

$$I_{B2} = \frac{1}{\beta + 1} I_{E2} = \frac{\beta + 2}{\beta + 1} I_B \tag{182}$$

$$I_{REF} = I_{C1} + I_{B2} = \beta I_B + \frac{\beta + 2}{\beta + 1} I_B \tag{183}$$

$$\frac{I_O}{I_{REF}} = \frac{\frac{\beta(\beta+2)}{\beta+1} I_B}{\beta I_B + \frac{\beta+2}{\beta+1} I_B} = \frac{\frac{\beta(\beta+2)}{\beta+1}}{\frac{\beta(\beta+1)}{\beta+1} + \frac{\beta+2}{\beta+1}} = \frac{\beta(\beta+2)}{\beta(\beta+1)+(\beta+2)} \quad (184)$$

$$\frac{I_O}{I_{REF}} = \frac{\beta^2+2\beta}{\beta^2+2\beta+2} = \frac{1}{1+\frac{2}{\beta^2+2\beta}} \approx \frac{1}{1+\frac{2}{\beta^2}} \approx 1 \quad (185)$$

Thus the Wilson mirror ratio is much closer to unity than the ratio of the simple diode-biased mirror.

Reference Current:

The reference current can be found by summing voltages rises from ground to V_{CC}:

$$I_{REF} = \frac{V_{CC} - V_{BE2} - V_{BE3}}{R_{REF}} \approx \frac{V_{CC} - 1.4\,\text{V}}{R_{REF}} \quad (186)$$

Output Resistance:

The output resistance of the Wilson can be shown to be βr_{o2}.

However, the derivation of the output resistance is a sizable endeavor and will not be undertaken here.

Widlar Current Mirror

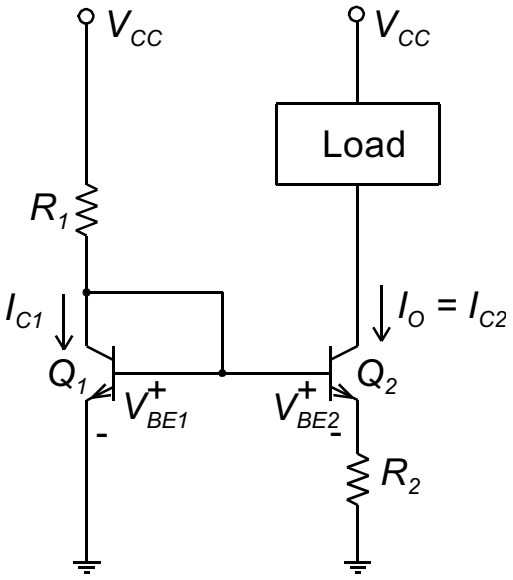

Fig. 197. Widlar mirror.

If very small currents are required, the resistances in the previous mirror circuits become prohibitively large.

The Widlar mirror solves that problem Though it uses two resistors, the *total* resistance required by this circuit is reduced substantially.

The circuit's namesake is Bob Widlar (wide' lar) of Fairchild Semiconductor and National Semiconductor.

The analysis is somewhat different than our previous two examples.

Current Relationship:

Recall the Shockley transistor equations for forward bias:

$$i_C = I_S \exp\left(\frac{v_{BE}}{V_T}\right) \quad \text{and} \quad v_{BE} = V_T \ln\left(\frac{i_C}{I_S}\right) \tag{187}$$

Thus we may write:

$$V_{BE1} = V_T \ln\left(\frac{i_{C1}}{I_S}\right) \quad \text{and} \quad V_{BE2} = V_T \ln\left(\frac{i_{C2}}{I_S}\right) \tag{188}$$

Note that V_T and I_S are the same for both transistors because they are *identical* (and assumed to be at the same temperature).

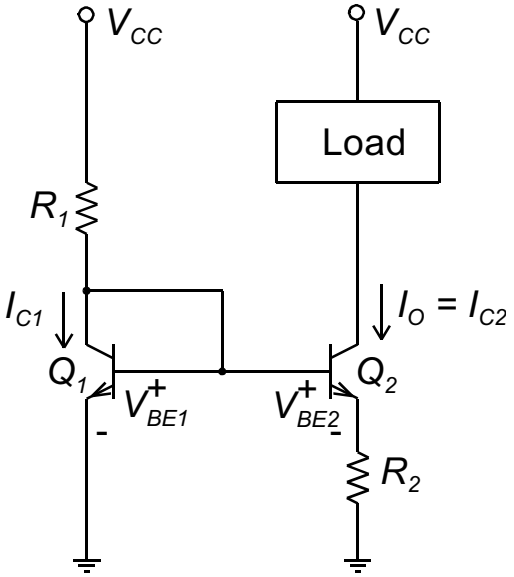

Fig. 198. Widlar mirror (Fig. 197 repeated).

Continuing with the derivation from the previous page . . .

From a KVL equation around the base-emitter loop:

$$V_{BE1} = V_{BE2} + R_2 I_{E2} \approx V_{BE2} + R_2 I_{C2} \quad \textbf{(189)}$$

Rearranging:

$$V_{BE1} - V_{BE2} = \Delta V_{BE} \approx R_2 I_{C2} \quad \textbf{(190)}$$

Substituting the base-emitter voltages from eq. (188) into eq. (190):

$$V_T \ln\left(\frac{I_{C1}}{I_S}\right) - V_T \ln\left(\frac{I_{C2}}{I_S}\right) \approx R_2 I_{C2} \quad \Rightarrow \quad V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right) \approx R_2 I_{C2} \quad \textbf{(191)}$$

Where the last step results from a law of logarithms.

This is a transcendental equation. It must be solved *iteratively*, or with a spreadsheet, etc. The form of the equation to use depends on whether we're interested in analysis or design:

Analysis: $\frac{V_T}{R_2} \ln\left(\frac{I_{C1}}{I_{C2}}\right) = I_{C2}$ Design: $R_2 = \frac{V_T}{I_{C2}} \ln\left(\frac{I_{C1}}{I_{C2}}\right)$ **(192)**

where:

$$I_{C1} \approx I_{REF} = \frac{V_{CC} - V_{BE1}}{R_1} \quad \textbf{(193)}$$

Multiple Current Mirrors

In typical integrated circuits multiple current mirrors are used to provide various bias currents. Usually, though, there is only *one reference current*, so that the total resistance on the chip may be minimized.

The figure below illustrates the technique of multiple current mirrors, as well as mirrors constructed with *pnp* devices:

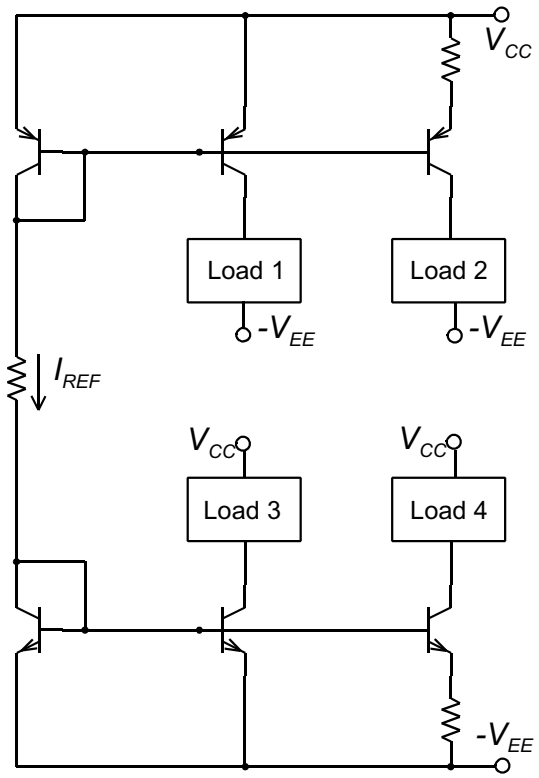

Fig. 199. Multiple current mirrors.

FET Current Mirrors

The same techniques are used in CMOS ICs (except, of course, the devices are MOSFETs). The details of these circuits are not discussed here.

Linear Small-Signal Equivalent Circuits

- In most amplifiers (and many other circuits):

  We use dc to bias a nonlinear device . . .

  At an *operating point* (*Q-point*) where the nonlinear device characteristic is relatively straight, i.e., *almost* linear . . .

  And then *inject* the signal to be amplified (the *small signal*) into the circuit.

- The circuit analysis is split into two parts:

  DC analysis, which must consider the nonlinear device characteristics to determine the operating point.

  Alternatively, we can substitute an accurate model, such as a piecewise-linear model, for the nonlinear device.

  AC analysis, but because injected signal is *small*, only a small region of the nonlinear device characteristic need be considered.

  This small region is *almost* linear, so we assume it is linear, and construct a *linear small-signal equivalent circuit*.

- After analysis, the resulting dc and ac values may be recombined, if necessary or desired.

Diode Small-Signal Equivalent Circuit

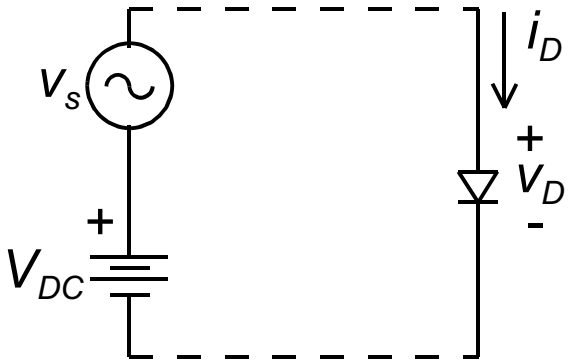

Fig. 200. Generalized diode circuit.

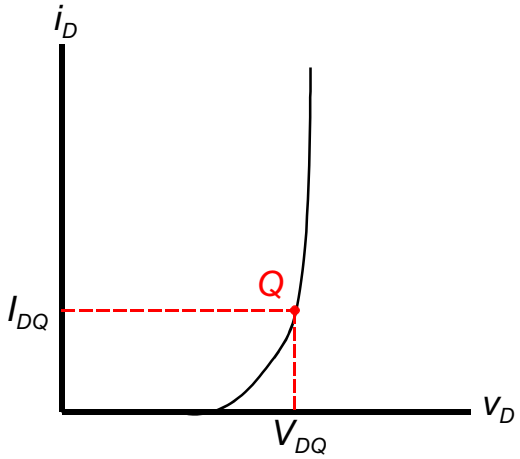

Fig. 201. Diode characteristic.

The Concept

First, we allow v_s to be zero. The circuit is now *dc only*, and has a specific *Q*-point shown.

We can find the *Q*-point analytically with the Shockley equation, or with a diode model such as the ideal, constant-voltage-drop, or piecewise-linear model.

Now, we allow v_s to be nonzero, but *small*.

The *instantaneous* operating point moves slightly above and below the *Q*-point. If signal is small enough, we can approximate the diode curve with a straight line.

The Equations

This straight-line approximation allows us to write a *linear* equation relating the *changes* in diode current (around the *Q*-pt.) to the *changes* in diode voltage:

$$\Delta i_D = K\,\Delta v_D \qquad \textbf{(194)}$$

Repeating the linear equation from the previous page:

$$\Delta i_D = K\,\Delta v_D \tag{195}$$

The coefficient K is the slope of the straight-line approximation, and must have units of Ω^{-1}.

We can choose *any* straight line we want. The *best* choice (in a least-squared error sense) is a *line tangent at pt. Q !!!*

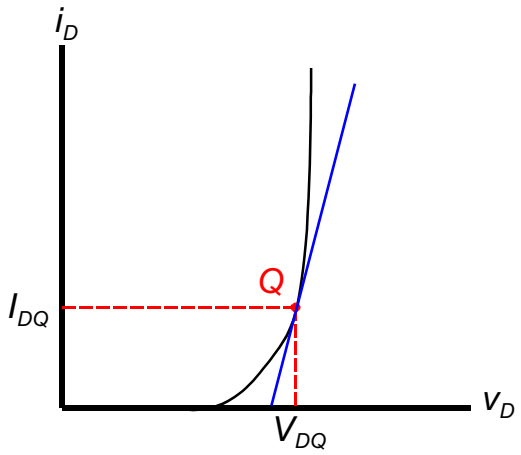

Fig. 202. Diode curve with tangent at Q-point.

We rewrite eq. (195) with changes in notation.

K becomes $1/r_d$, Δi_D becomes i_d, and Δv_D becomes v_d:

$$i_d = \frac{1}{r_d} v_d \tag{196}$$

This is merely Ohm's Law*!!!*

r_d is the *dynamic resistance* or *small-signal resistance* of the diode.

i_d and v_d are the *signal current* and the *signal voltage*, respectively.

Diode Small-Signal Resistance

We need only to calculate the value of r_d, where $1/r_d$ is the slope of a line tangent at pt. *Q*, i.e.,

$$\frac{1}{r_d} = \left.\frac{\partial i_D}{\partial v_D}\right|_{Q-point} \tag{197}$$

We use the diode forward-bias approximation:

$$i_D = I_S\left[\exp\left(\frac{v_D}{nV_T}\right) - 1\right] \approx I_S \exp\left(\frac{v_D}{nV_T}\right) \tag{198}$$

Thus:

$$\frac{\partial}{\partial v_D}\left[I_S \exp\left(\frac{v_D}{nV_T}\right)\right]_{Q-point} = \frac{I_S}{nV_T}\exp\left(\frac{V_{DQ}}{nV_T}\right) \tag{199}$$

But, notice from (198):

$$I_{DQ} \approx I_S \exp\left(\frac{V_{DQ}}{nV_T}\right) \tag{200}$$

So:

$$\left.\frac{\partial i_D}{\partial v_D}\right|_{Q-point} \approx \frac{I_{DQ}}{nV_T} \quad \Rightarrow \quad r_d \approx \frac{nV_T}{I_{DQ}} \tag{201}$$

Notes:

1. The calculation of r_d is easy, once we know I_{DQ} *!!!*
2. I_{DQ} can be estimated with simple diode models *!!!*
3. Diode small-signal resistance r_d varies with *Q*-point.
4. *The diode small-signal model is simply a resistor !!!*

Notation

The following notation is standard:

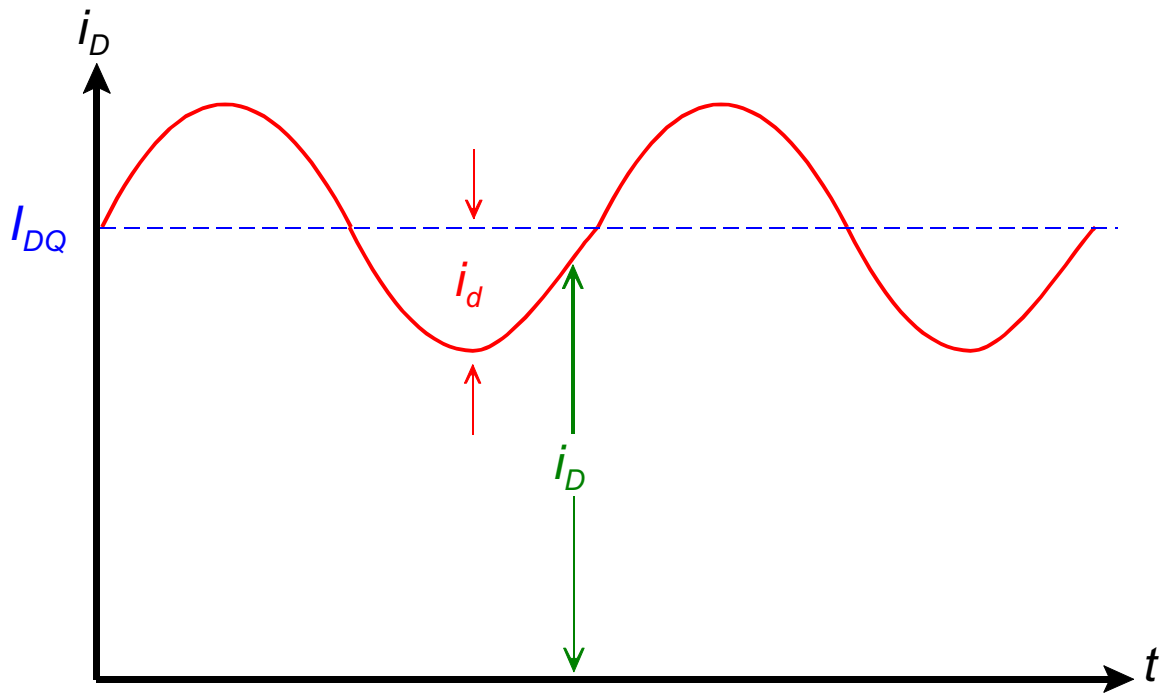

Fig. 203. Illustration of various currents.

v_D, i_D — This is the *total instantaneous quantity*. (dc + ac, or bias + signal)

V_D, I_D — This is the *dc quantity*. (i.e., the average value)

v_d, i_d — This is the *ac quantity*. (This is the total instantaneous quantity with the average removed)

V_d, I_d — If a vector, this is a *phasor quantity*. If a scalar it is an *rms* or *effective* value.

BJT Small-Signal Equivalent Circuit

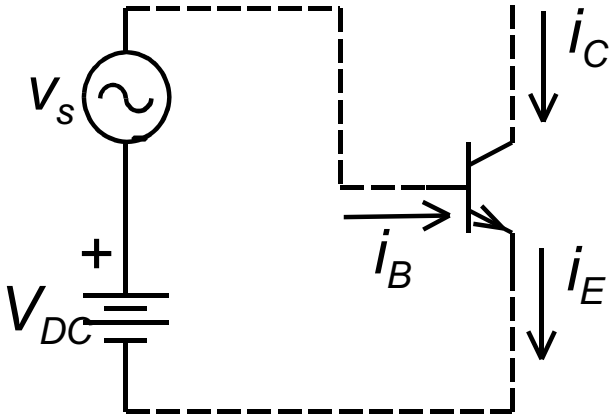

Fig. 204. Generalized BJT circuit.

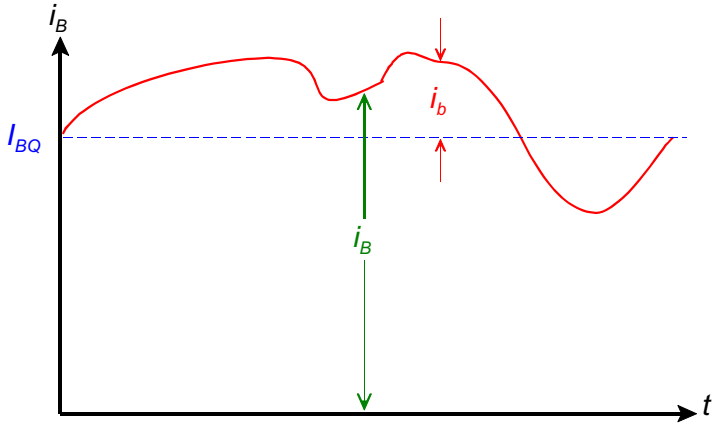

Fig. 205. Generalized base current waveform.

First, note the total base current (bias + signal): $i_B = I_{BQ} + i_b$

This produces a total base-emitter voltage: $v_{BE} = V_{BEQ} + v_{be}$

Now, let the *signal* component be *small*: $|i_b| << I_{BQ}$

With the signal sufficiently small, v_{be} and i_b will be approximately related by the slope of the BJT input characteristic, at the *Q*-point.

This is identical to the diode small-signal development *!!!* Thus, the equations will have the same form:

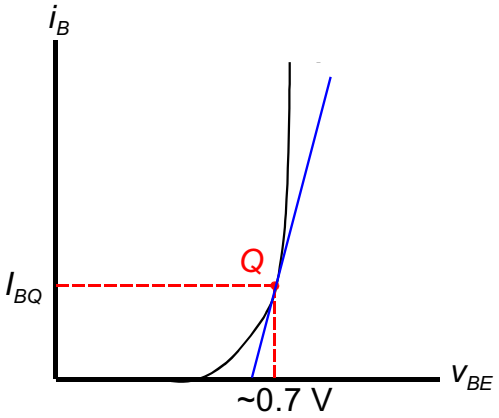

Fig. 206. BJT input characteristic.

$$i_b = \left[\left. \frac{\partial i_B}{\partial v_{BE}} \right|_{Q-point} \right] v_{be} = \frac{1}{r_\pi} v_{be} \qquad \textbf{(202)}$$

$$\text{where} \quad r_\pi \approx \frac{V_T}{I_{BQ}} \qquad \textbf{(203)}$$

With r_π determined, we can turn our attention to the output (collector) side.

If the BJT is in its active region, we have a simple current relationship:

$$i_C = \beta i_B \quad \Rightarrow \quad i_c = \beta i_b \tag{204}$$

Combining eqs. (202) through (204) we can construct the *BJT small-signal equivalent circuit*:

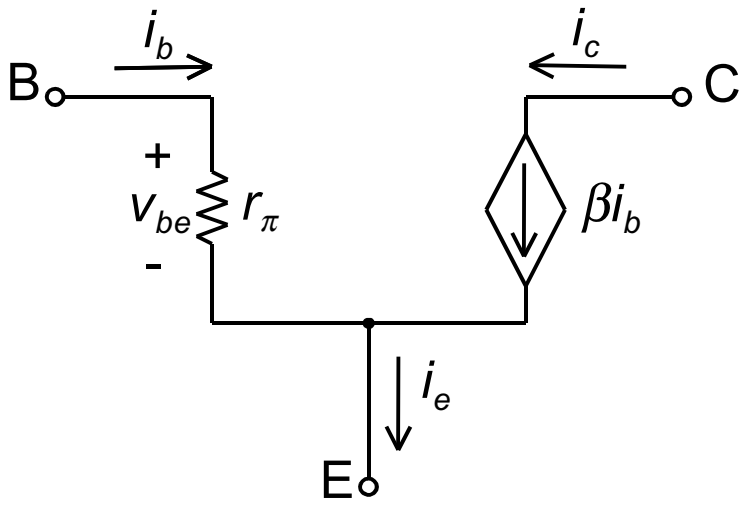

Fig. 207. BJT small-signal equivalent circuit.

Because the bias point is "accounted for" in the calculation of r_π, this model applies identically to *npn* and to *pnp* devices.

The Common-Emitter Amplifier

Introduction

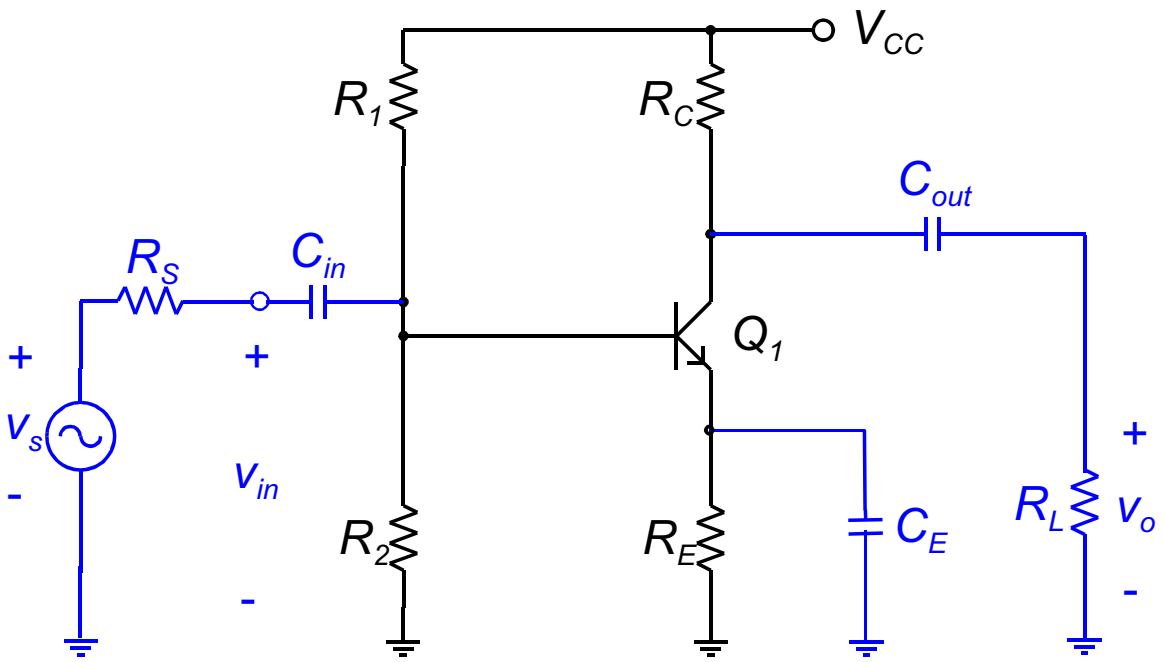

Fig. 208. Standard common emitter amplifier circuit.

The typical four-resistor bias circuit is shown in black. . .capacitors are *open circuits* at dc, so only signal currents can flow in the blue branches.

Capacitors are chosen to appear as short circuits at frequencies contained in the signal (called *midband frequencies*).

C_{in} and C_{out} couple the signal into, and out of, the amplifier. C_E provides a short circuit around R_E for signal currents only (dc currents cannot flow through C_E.

A standard dc analysis of the four-resistor bias circuit provides the *Q-point*, and from that we obtain the value of r_π.

Constructing the Small-Signal Equivalent Circuit

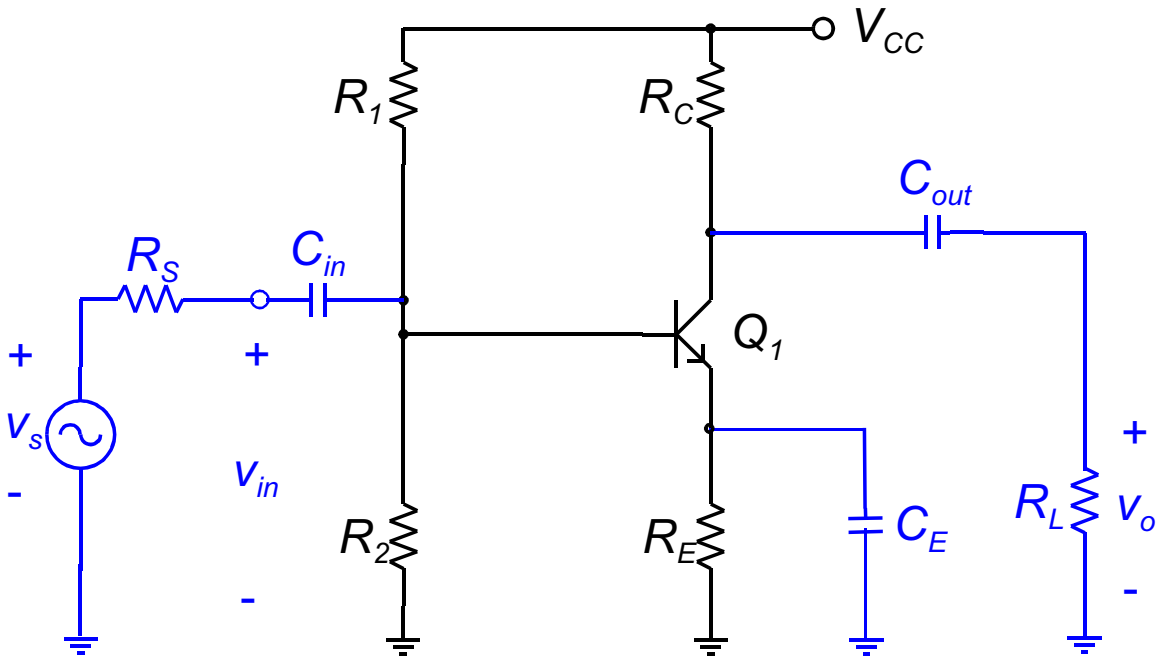

Fig. 209. Standard common emitter. (Fig. 208 repeated)

To construct small-signal equivalent circuit for entire amplifier, we:

1. Replace the BJT by its small-signal model.
2. Replace all capacitors with short circuits.
3. Set all *dc* sources to zero, *because they have zero signal component!!!*

The result is the small-signal equivalent circuit of the amplifier:

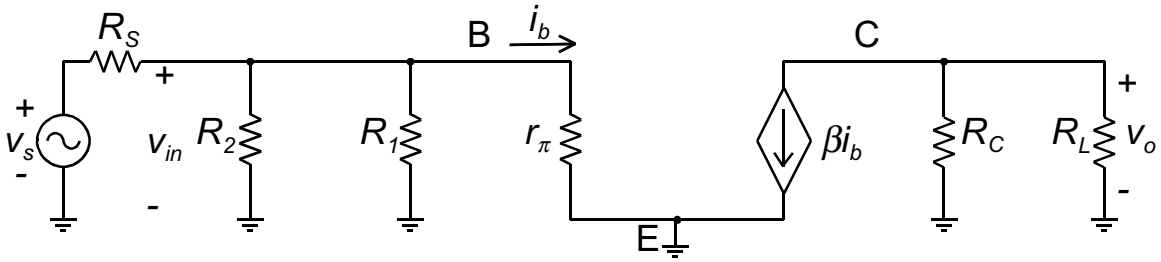

Fig. 210. Small signal equivalent circuit of common emitter amplifier.

For convenience we let $R_1 \parallel R_2 = R_B$, and $R_C \parallel R_L = R_L'$:

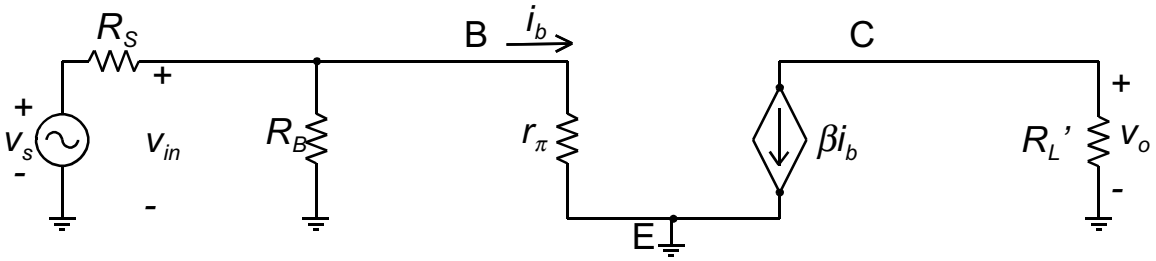

Fig. 211. Simplified small signal equivalent of common emitter amplifier.

Voltage Gain

Our usual focus is $A_v = v_o/v_{in}$, or $A_{vs} = v_o/v_s$. We concentrate on the former. Because i_b is the only parameter common to both sides of the circuit, we can design an approach:

1. We write an equation on the input side to relate v_{in} to i_b.
2. We write an equation on output side to relate v_o to i_b.
3. We combine equations to eliminate i_b.

Thus:

$$v_{in} = v_{be} = i_b r_\pi \tag{205}$$

$$v_o = -\beta i_b R_L' \tag{206}$$

And:

$$A_v = \frac{v_o}{v_{in}} = \frac{-\beta i_b R_L'}{i_b r_\pi} = \frac{-\beta R_L'}{r_\pi} \tag{207}$$

With R_L removed (an *open-circuit load*), we define the *open-circuit voltage gain*, A_{vo}:

$$A_{vo} = \frac{v_o}{v_{in}} = \frac{-\beta R_C}{r_\pi} \tag{208}$$

Input Resistance

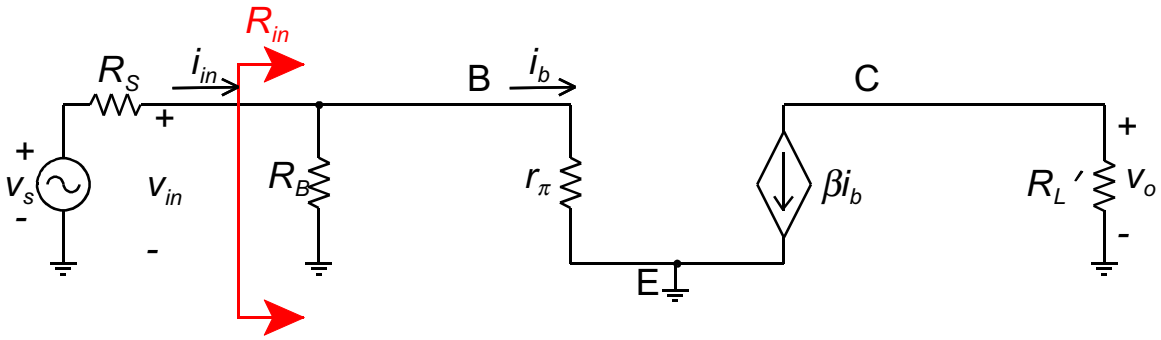

Fig. 212. Input resistance of common emitter amplifier.

By definition, $R_{in} = v_{in}/i_{in}$. We can find this simply by inspection:

$$R_{in} = R_B \| r_\pi \tag{209}$$

Output Resistance

Recall that to find R_o, we must remove the load, and set all *independent* sources to zero, but *only* independent sources. *We do not set dependent sources to zero!!!*

Thus:

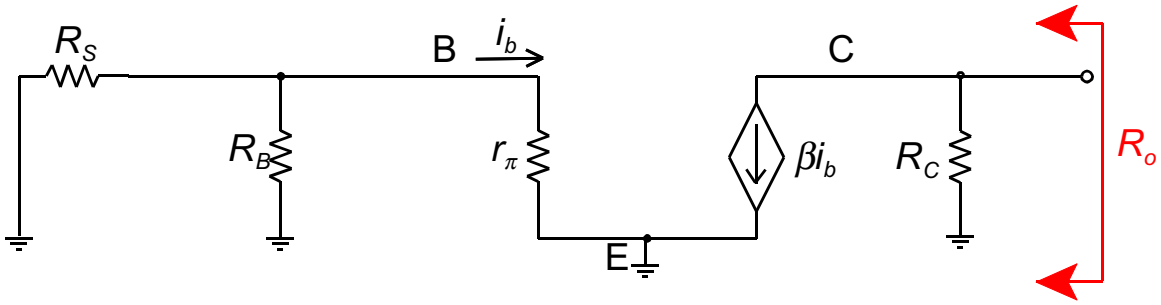

Fig. 213. Output resistance of common emitter amplifier.

Now, because $i_b = 0$, the dependent source $\beta i_b = 0$ also,and:

$$R_o = R_C \tag{210}$$

The Emitter Follower (Common Collector Amplifier)

Introduction

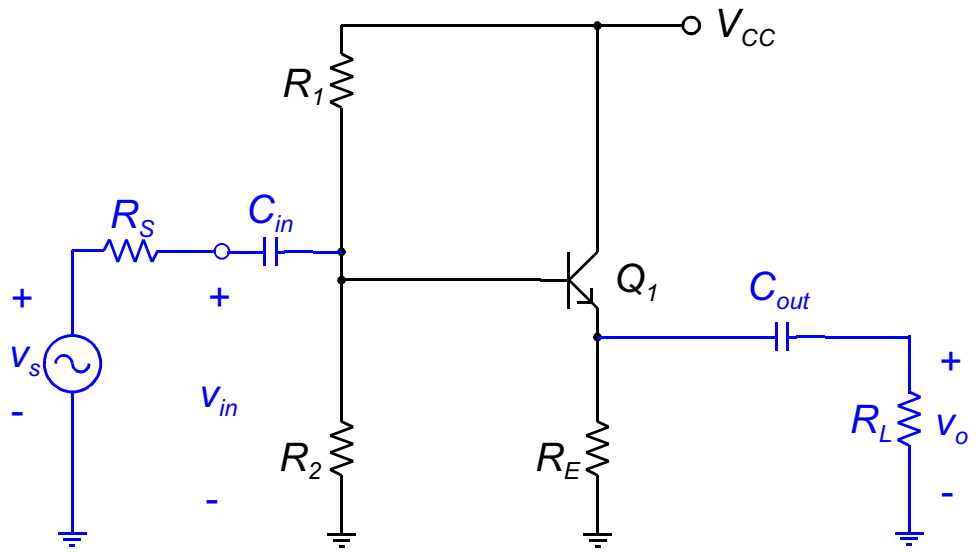

Fig. 214. Standard emitter follower circuit.

We have a four-resistor bias network, with $R_C = 0$.

Unlike the common-emitter amplifier, v_o is taken from the emitter.

The small-signal equivalent is derived as before:

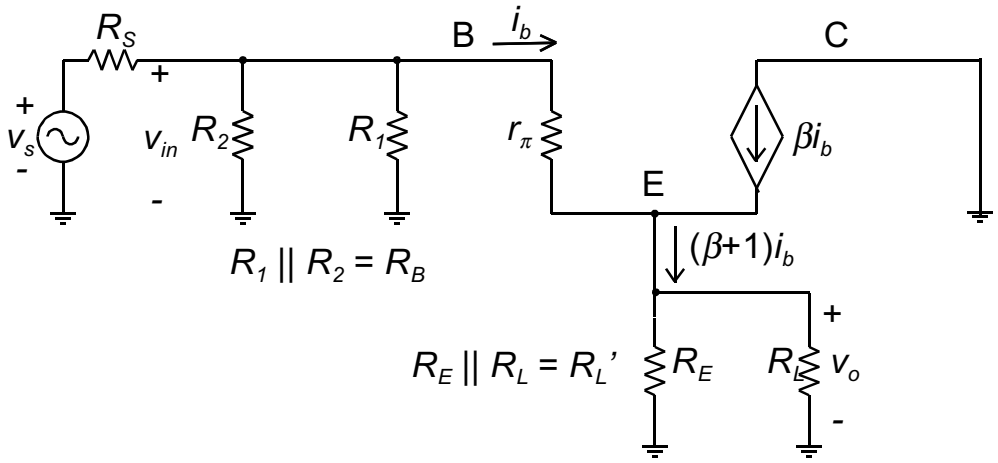

Fig. 215. Emitter follower small-signal equivalent circuit. The collector terminal is grounded, or *common*, hence the alternate name Common Collector Amplifier.

Voltage Gain

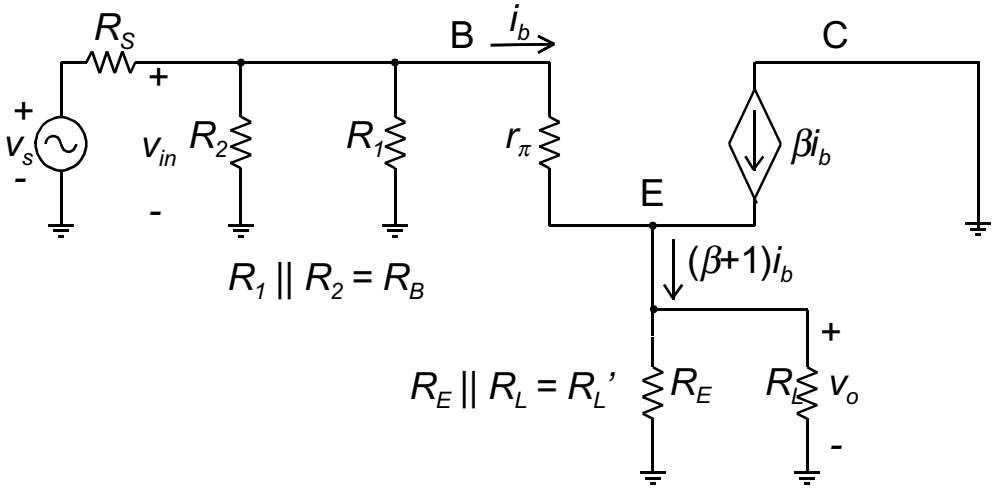

Fig. 216. Emitter follower small-signal equivalent (Fig. 215 repeated).

Gain, $A_v = v_o / v_{in}$, is found using the same approach described for the common-emitter amplifier. We write two equations of i_b - one on the input side, one on the output side - and solve:

$$v_{in} = i_b r_\pi + (\beta + 1) i_b R_L' \tag{211}$$

$$v_o = (\beta + 1) i_b R_L' \tag{212}$$

$$A_v = \frac{v_o}{v_{in}} = \frac{(\beta + 1) R_L'}{r_\pi + (\beta + 1) R_L'} \tag{213}$$

Typical values for A_v range from 0.8 to unity. The emitter (output) voltage *follows* the input voltage, hence the name *emitter follower*.

The feature of the follower is not voltage gain, but power gain, high input resistance and low output resistance, as we see next . . .

Input Resistance

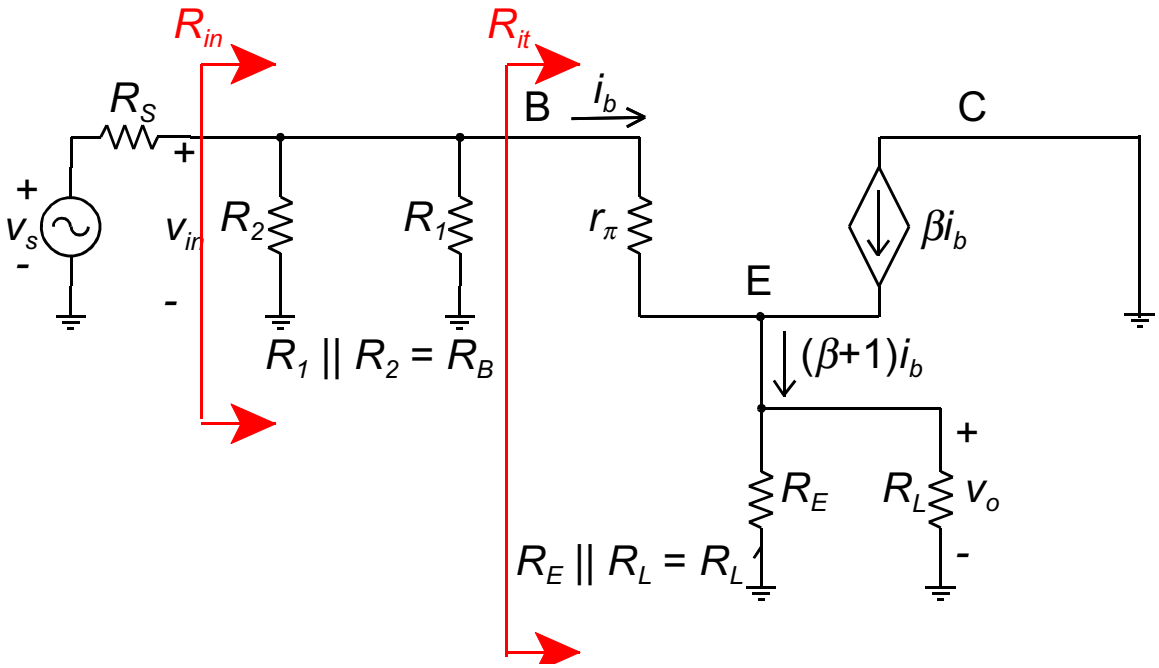

Fig. 217. Calculating the input resistance of the emitter follower.

Note that :

$$R_{in} = \frac{v_{in}}{i_{in}} = R_B \| R_{it}, \quad \text{where } R_{it} = \frac{v_{in}}{i_b} \tag{214}$$

We've already written the equation we need to find R_{it}. It's equation (211), from which:

$$R_{it} = r_\pi + (\beta + 1) R_L' \tag{215}$$

Thus

$$R_{in} = R_B \| \left[r_\pi + (\beta + 1) R_L' \right] \tag{216}$$

Compare this to the common emitter input resistance, which is generally *much* lower, at $R_{in} = R_B \| r_\pi$.

Output Resistance

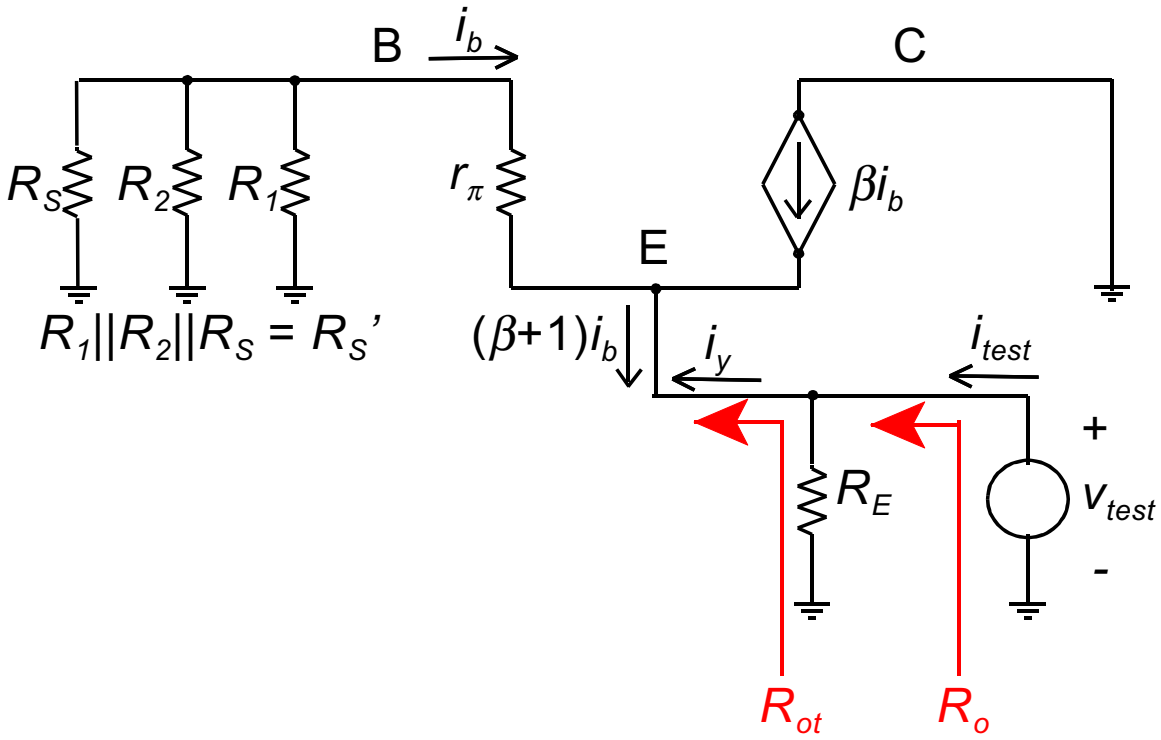

Fig. 218. Circuit for calculating follower output resistance.

Notice that we have set the independent source to zero, and replaced R_L by a test source. From the definition of output resistance:

$$R_o = \frac{v_{test}}{i_{test}} = R_E || R_{ot}, \quad \text{where } R_{ot} = \frac{v_{test}}{i_y} = \frac{v_{test}}{-(\beta+1)i_b} \tag{217}$$

But

$$v_{test} = -i_b\left(R_S' + r_\pi\right) \quad \therefore \quad R_{ot} = \frac{R_S' + r_\pi}{\beta + 1} \tag{218}$$

Compare this to the common emitter input resistance, which is *much* higher, at R_C.

Review of Small Signal Analysis

It's presumed that a dc analysis has been completed, and r_π is known.

1. Draw the small-signal equivalent circuit.
   - **A.** Begin with the transistor small signal model.
   - **B.** For midband analysis, coupling and bypass capacitors replaced by short circuits.
   - **C.** Set *independent* dc sources to zero.
2. Identify variables of interest.
3. Write appropriate independent circuit equations.

   (This usually requires an equation on the "input" side and an equation on the "output" side of the small-signal equivalent circuit.)
4. Solve.
5. *Check units!!!*

FET Small-Signal Equivalent Circuit

The Small-Signal Equivalent

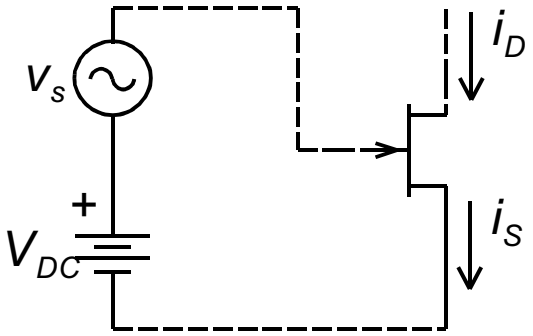

Fig. 219. Generalized FET circuit.

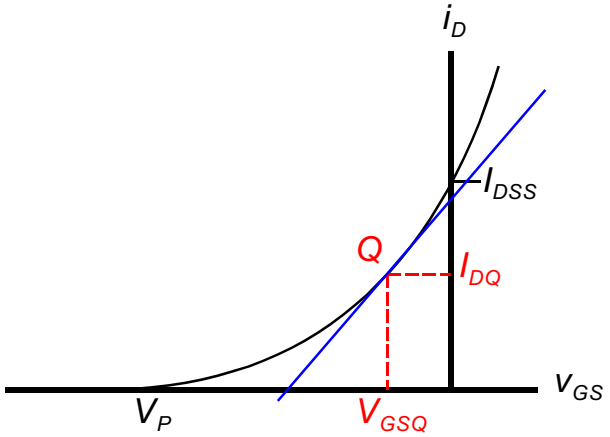

Fig. 220. FET transfer characteristic.

We restrict operation to the pinch-off region and note that the dc source and the circuit determine the Q-point.

For *small* v_s, the instantaneous operating pt. stays very near Q, and the transfer curve can be approximated with a line tangent at Q.

Both v_{GS} and i_D have dc and ac components:

$$v_{GS} = V_{GSQ} + v_{gs} \quad \text{and} \quad i_D = I_{DQ} + i_d \tag{219}$$

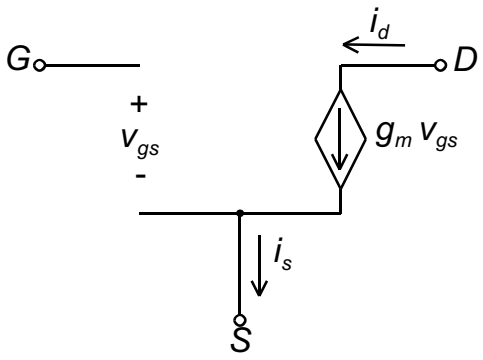

Fig. 221. FET sm. sig. model.

V_{GSQ} and I_{DQ} are related by the second-order FET characteristic, but if $|v_s|$ is *small* enough, v_{gs} and i_d are related (almost) linearly:

$$i_d = g_m v_{gs} \tag{220}$$

g_m, is called the *transconductance*.

This leads immediately to the model at left.

Transconductance

The coefficient g_m is the slope of the tangent :

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q \qquad \textbf{(221)}$$

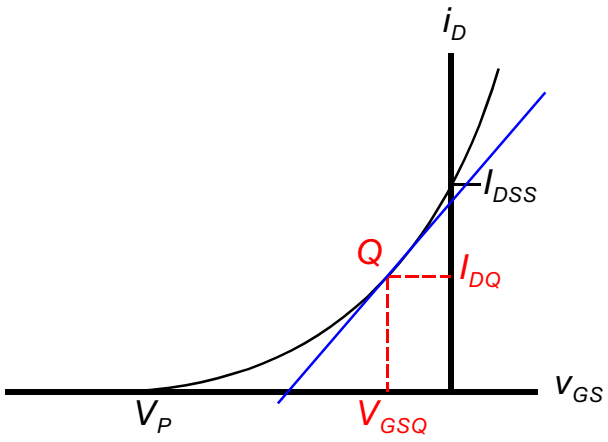

Fig. 222.FET transfer characteristic.

From the pinch-off region equation:

$$i_D = K\left(v_{GS} - V_P\right)^2 \qquad \textbf{(222)}$$

We obtain:

$$g_m = \frac{\partial}{\partial v_{GS}}\left[K\left(v_{GS} - V_P\right)^2\right]_Q = 2K\left(V_{GSQ} - V_P\right) \qquad \textbf{(223)}$$

But also from eq. (222) we have

$$V_{GSQ} - V_P = \sqrt{\frac{I_{DQ}}{K}} \qquad \textbf{(224)}$$

Substituting this into eq. (223), we see that the transconductance can also be written as:

$$g_m = 2\sqrt{KI_{DQ}} \qquad \textbf{(225)}$$

Or, finally, because $K = I_{DSS}/V_P^2$ we can write:

$$g_m = 2\frac{\sqrt{I_{DSS}I_{DQ}}}{|V_P|} \qquad \textbf{(226)}$$

FET Output Resistance

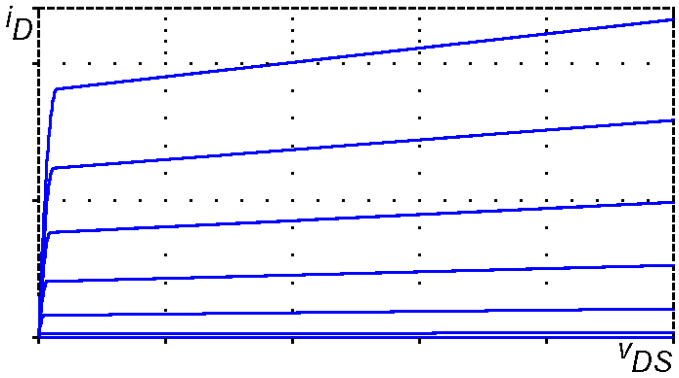

Fig. 223. FET output characteristics.

Recall that FET output characteristics have upward slope. This means that i_d is not dependent only on v_{gs}, but also on v_{ds}.

We can account for both dependencies by writing:

$$i_d = \left[\frac{\partial i_D}{\partial v_{GS}}\bigg|_Q\right] v_{gs} + \left[\frac{\partial i_D}{\partial v_{DS}}\bigg|_Q\right] v_{ds} = g_m v_{gs} + \frac{v_{ds}}{r_d} \qquad \textbf{(227)}$$

where

$$\frac{\partial i_D}{\partial v_{DS}}\bigg|_Q = \frac{1}{r_d} = \text{ slope of output char. at } Q \qquad \textbf{(228)}$$

A single addition to the small-signal model accounts for r_d:

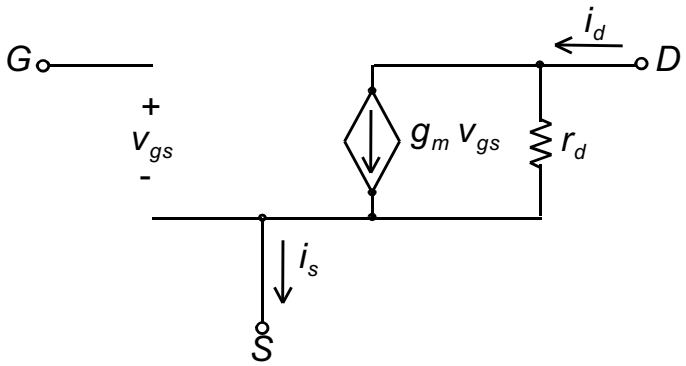

Fig. 224. FET small-signal model including FET output resistance.

Output resistance is more noticeable in FETs than in BJTs.

But it is also observed in BJTs and can be included in the BJT small-signal model, where the notation r_o is used for output resistance.

The Common Source Amplifier

The Small-Signal Equivalent Circuit

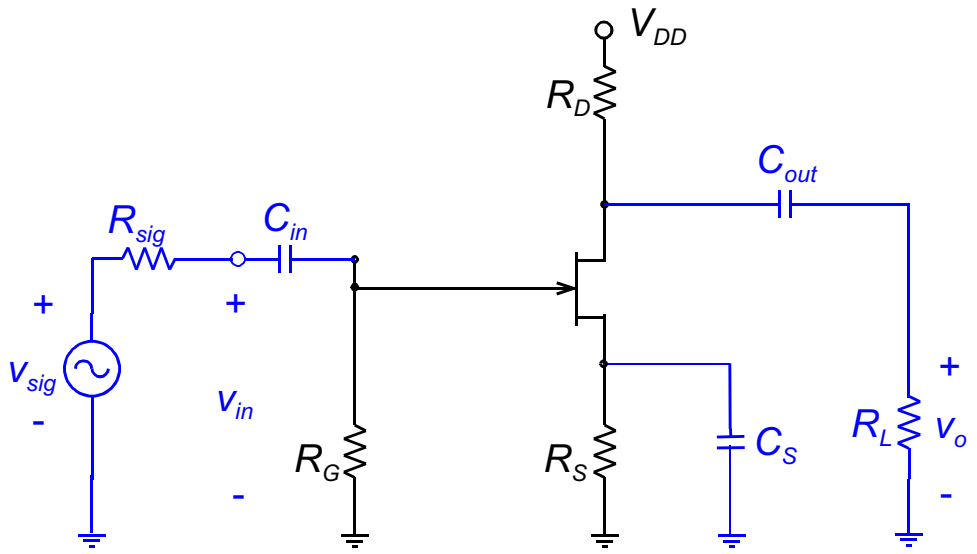

Fig. 225. Standard common source amplifier circuit.

The self-bias circuit is shown in black.

Capacitors are *open circuits* at dc, so only signal currents flow in the blue branches.

A standard dc analysis provides the value of g_m.

The small-signal equivalent is constructed in the standard manner:

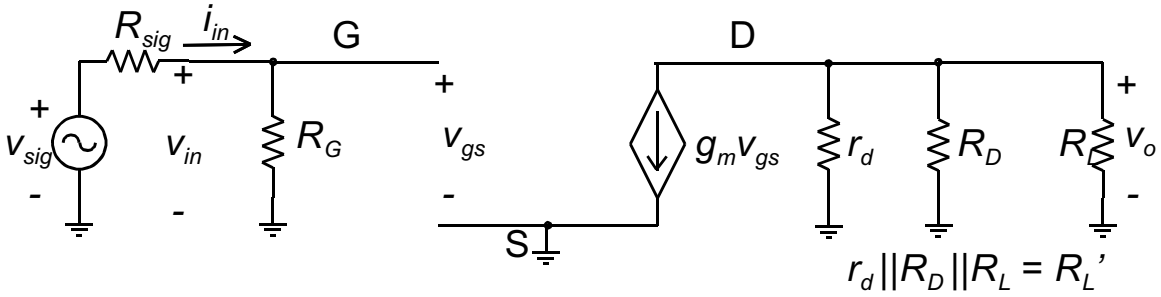

Fig. 226. Small-signal equivalent circuit for the common source amplifier.

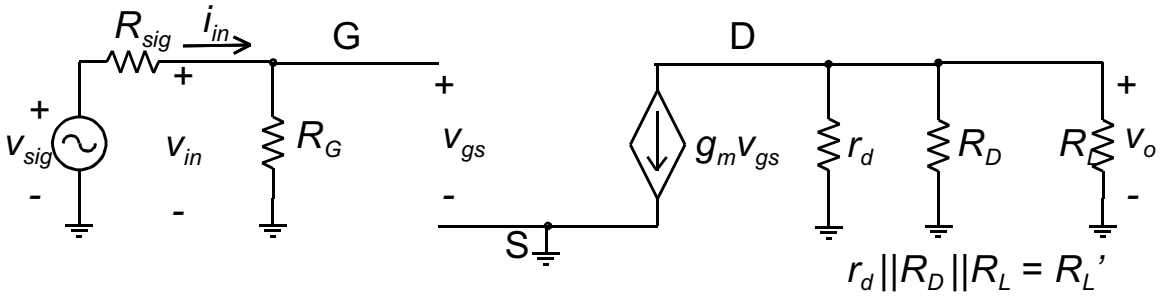

Fig. 227. Common source small signal equivalent (Fig. 226 repeated).

Voltage Gain

$$v_{in} = v_{gs} \qquad \text{and} \qquad v_o = -g_m v_{gs} R_L' \tag{229}$$

Thus:

$$A_v = \frac{v_o}{v_{in}} = -g_m R_L' \tag{230}$$

Input Resistance

$$R_{in} = \frac{v_{in}}{i_{in}} = R_G \tag{231}$$

Because no dc current flows through R_G it can be *extremely* large.

Output Resistance

Remember, we must remove R_L, and set all independent sources to zero. For this circuit we can determine R_o by inspection:

$$R_o = r_d || R_D \tag{232}$$

The Source Follower

Small-Signal Equivalent Circuit

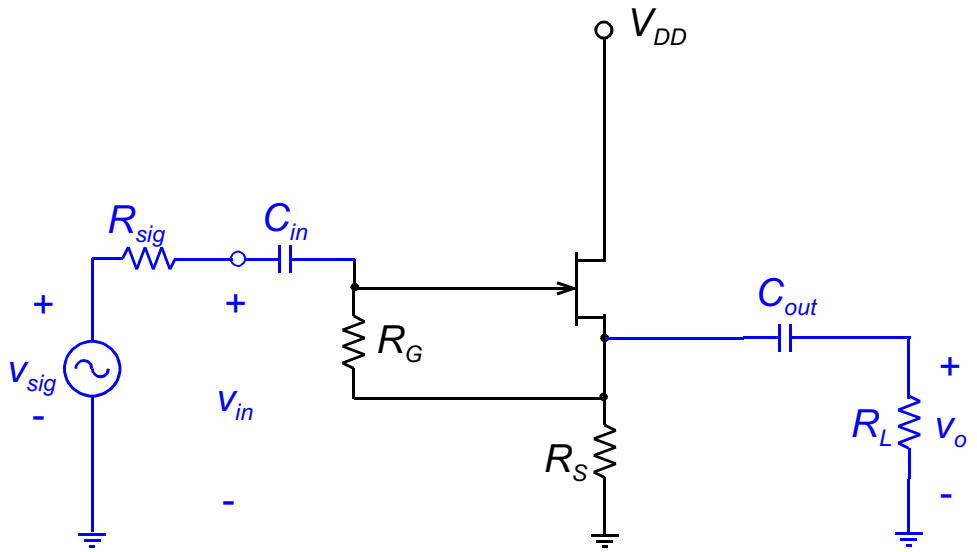

Fig. 228. Source follower circuit.

This follower uses *fixed bias*: $I_G = 0 \Rightarrow V_{GSQ} = 0 \Rightarrow I_D = I_{DSS}$

Tremendously large R_{in} is obtained by sacrificing bias stability, which isn't very important in this circuit anyway, as we shall see.

The small-signal equivalent is constructed in the usual manner:

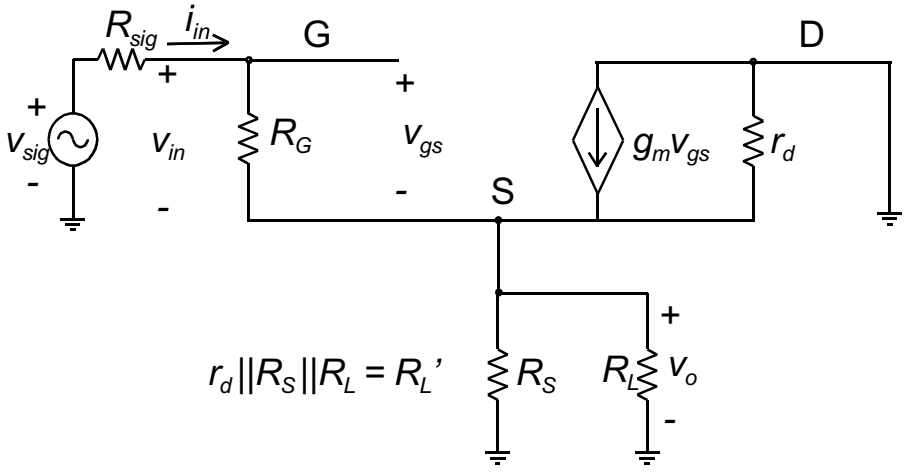

Fig. 229. Source follower small-signal equivalent circuit.

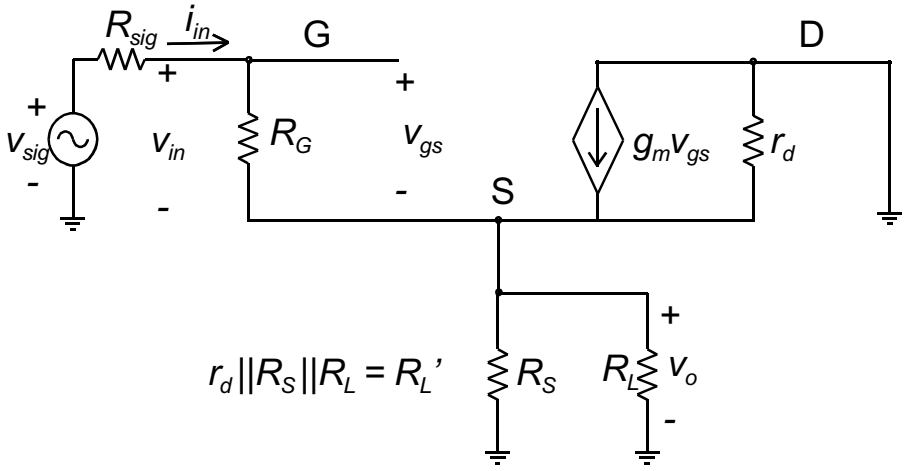

Fig. 230. Source follower small-signal equivalent circuit (Fig. 229 repeated).

Voltage Gain

This one requires a little more algebra. Beginning with:

$$v_{in} = v_{gs} + v_o \quad \Longrightarrow \quad v_{gs} = v_{in} - v_o \tag{233}$$

and

$$v_o = \left(g_m v_{gs} + i_{in}\right)R_L' = \left(g_m v_{gs} + \frac{v_{gs}}{R_G}\right)R_L' = v_{gs}\left(g_m + \frac{1}{R_G}\right)R_L' \tag{234}$$

We replace v_{gs} in eq. (234) with eq. (233), and solve for v_o/v_{in}:

$$v_o = \left(v_{in} - v_o\right)\left(g_m + \frac{1}{R_G}\right)R_L' \tag{235}$$

$$\left[1 + \left(g_m + \frac{1}{R_G}\right)R_L'\right]v_o = v_{in}\left(g_m + \frac{1}{R_G}\right)R_L' \tag{236}$$

$$A_v = \frac{v_o}{v_{in}} = \frac{\left(g_m + \frac{1}{R_G}\right)R_L'}{1 + \left(g_m + \frac{1}{R_G}\right)R_L'} = 0.5 \text{ to } 0.8 \text{ typically} \tag{237}$$

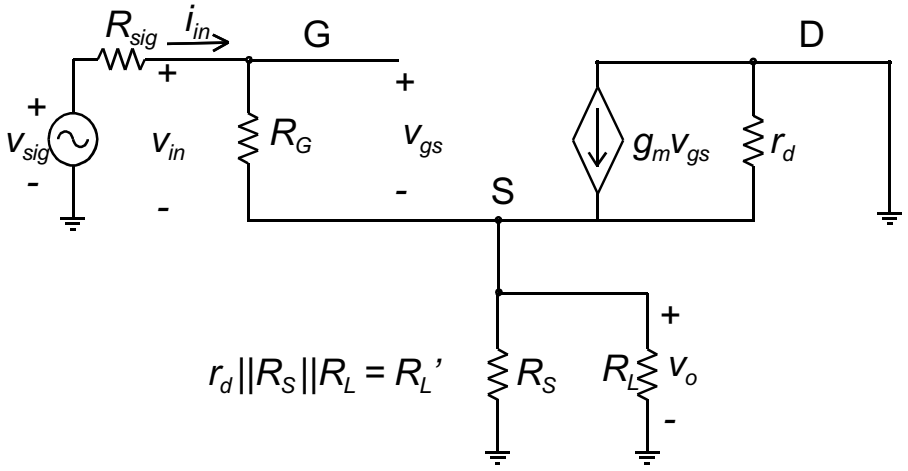

Fig. 231. Source follower small-signal equivalent circuit (Fig. 229 repeated).

Input Resistance

Replacing v_o in eq. (233) with eq. (234):

$$v_{in} = v_{gs} + v_o = v_{gs} + v_{gs}\left(g_m + \frac{1}{R_G}\right)R_L' \tag{238}$$

But $v_{gs} = i_{in} R_G$:

$$v_{in} = i_{in}R_G + i_{in}R_G\left(g_m + \frac{1}{R_G}\right)R_L' \tag{239}$$

Solving for v_{in}/i_{in} :

$$R_{in} = \frac{v_{in}}{i_{in}} = R_G + (1 + g_m R_G)R_L' \tag{240}$$

Because I_G = 0, R_G can be *several* MΩ. With the additional multiplying factor of R_L', R_{in} can become *extremely large!!!*

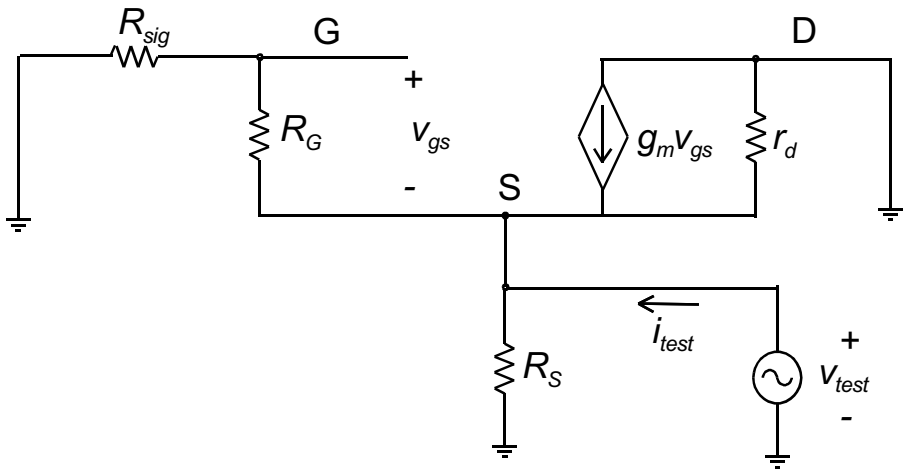

Fig. 232. Determining output resistance of the source follower.

Output Resistance

This calculation is a little more involved, so we shall be more formal in our approach.

We remove R_L, apply a test source, v_{test}, and set the independent source to zero.

From a KCL equation at the source node:

$$i_{test} = \frac{v_{test}}{R_S} + \frac{v_{test}}{r_d} + \frac{v_{test}}{R_G + R_{sig}} - g_m v_{gs} \tag{241}$$

But R_G and R_{sig} form a voltage divider:

$$v_{gs} = -\frac{R_G}{R_G + R_{sig}} v_{test} \tag{242}$$

Substituting eq. (242) into eq. (241):

$$i_{test} = v_{test}\left(\frac{1}{R_S} + \frac{1}{r_d} + \frac{1}{R_G + R_{sig}} + \frac{g_m R_G}{R_G + R_{sig}}\right) \tag{243}$$

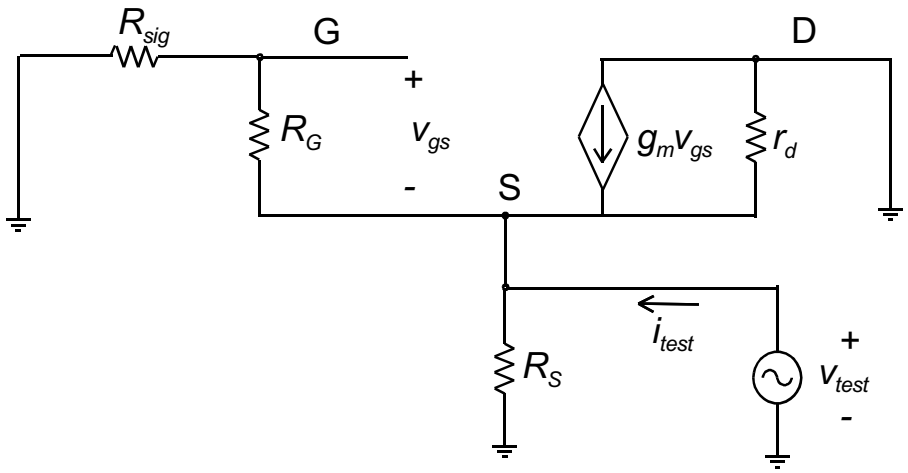

Fig. 233. Determining output resistance of the source follower (Fig. 232 repeated).

Thus:

$$R_o = \frac{v_{test}}{i_{test}} = \frac{1}{\frac{1}{R_S} + \frac{1}{r_d} + \frac{1}{R_G + R_{sig}} + \frac{g_m R_G}{R_G + R_{sig}}} \quad \textbf{(244)}$$

Finally, we recognize this form as that of resistances in parallel:

$$R_o = R_S \| r_d \| \left(R_G + R_{sig}\right) \| \left(\frac{R_G + R_{sig}}{g_m R_G} \right) \quad \textbf{(245)}$$

Review of Bode Plots

Introduction

The emphasis here is *review*. Please refer to an appropriate text if you need a more detailed treatment of this subject.

Let us begin with a generalized transfer function:

$$A_v(f) = \frac{\left(j\frac{f}{f_{Z1}}\right)\left(1+j\frac{f}{f_{Z2}}\right)\cdots}{\left(1+j\frac{f}{f_{P1}}\right)\cdots} \qquad \textbf{(246)}$$

We presume the function is limited to certain features:

- Numerator and denominator can be factored.
- Numerator factors have only one of the two forms shown.
- Denominator factors have only the form shown.

Remember:

- Bode plots are *not the actual curves, but only asymptotes to the actual curves*.
- Bode magnitude plots are not based on the transfer function itself, but on the logarithm of the transfer function - actually, on 20 log A_v.
- The total Bode response for $A_v(f)$ consists of the *magnitude response* and the *phase response*. Both of these consist of the sum of the responses to each numerator and denominator factor.

The Bode Magnitude Response

Now, let's review the Bode magnitude response of each term:

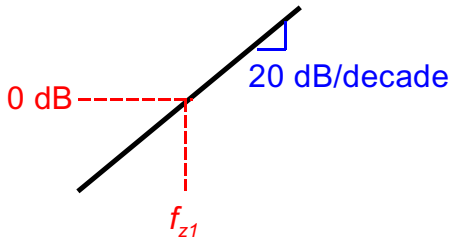

Fig. 234. Bode magnitude response for jf/f_{Z1}.

The numerator term $j\frac{f}{f_{Z1}}$:

The magnitude response increases 20 dB per decade for all *f*.

For $f = f_{Z1}$ the term has a magnitude of 1. Thus the magnitude response has an amplitude of 0 dB at f_{Z1}.

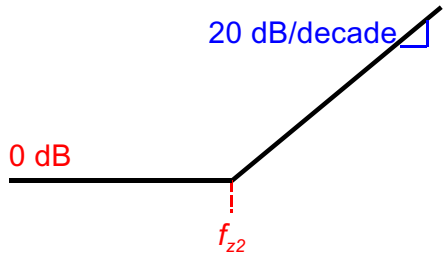

Fig. 235. Bode magnitude response for $1 + jf/f_{Z2}$.

The numerator term $1+j\frac{f}{f_{Z2}}$:

For $f << f_{Z2}$ the imaginary term is negligible; the magnitude is just 0 dB.

For $f >> f_{Z2}$ the imaginary term dominates, thus the magnitude increases 20 db per decade.

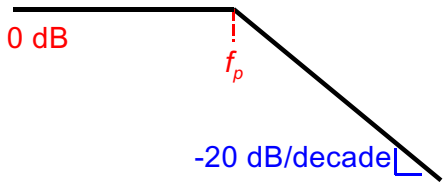

Fig. 236. Bode magnitude response for $1 + jf/f_{P1}$.

The denominator term $1+j\frac{f}{f_{P1}}$:

For $f << f_{P1}$ the imaginary term is negligible; the magnitude is just 0 dB.

For $f >> f_{P1}$ the imaginary term dominates, thus the magnitude decreases 20 db per decade (because the term is in the denominator).

The Bode Phase Response

Now, let's review the Bode phases response of each term:

Fig. 237. Bode phase response for jf/f_{Z1}.

The numerator term $j\frac{f}{f_{Z1}}$:

The phase response is simply 90° for all f.

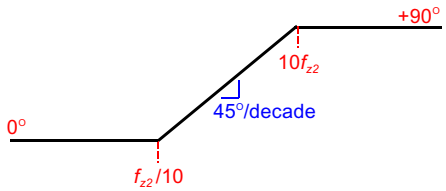

Fig. 238. Bode phase response for $1 + jf/f_{Z2}$.

The numerator term $1+j\frac{f}{f_{Z2}}$:

For $f << f_{Z2}$ the imaginary term is negligible; the phase is just 0°.

For $f >> f_{Z2}$ the imaginary term dominates, thus the phase is 90°.

At $f = f_{Z2}$, the term is $1 + j1$; its phase is 45°.

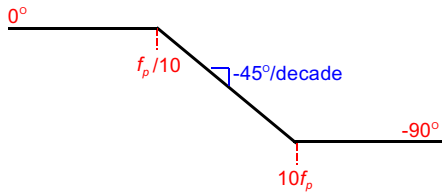

Fig. 239. Bode phase response for $1 + jf/f_{P1}$.

The denominator term $1+j\frac{f}{f_{P1}}$:

For $f << f_{Z2}$ the imaginary term is negligible; the phase is just 0°.

For $f >> f_{Z2}$ the imaginary term dominates, thus the phase is -90°.

At $f = f_{Z2}$, the term is $1 + j1$; its phase is -45°.

Single-Pole Low-Pass RC

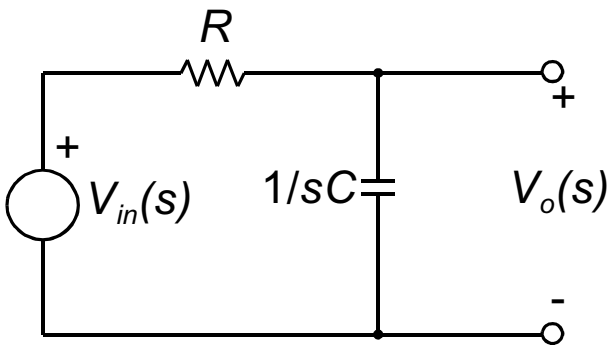

Fig. 240. Single-pole low-pass *RC* circuit,

The review of the details of the Bode response of a single-pole low-pass *RC* circuit begins with the s-domain transfer function:

$$A_v = \frac{V_o}{V_{in}} = \frac{\frac{1}{sC}}{R + \frac{1}{sC}} = \frac{1}{sRC + 1} \quad \textbf{(247)}$$

Note that there is a pole at $s = -1/RC$ and zero at $s = \infty$.

For the sinusoidal steady state response we substitute $j2\pi f$ for s:

$$A_v = \frac{1}{1 + j(2\pi RC)f} = \frac{1}{1 + j\frac{f}{f_b}} \quad \text{where} \quad f_b = \frac{1}{2\pi RC} \quad \textbf{(248)}$$

This fits the generalized single-pole form from the previous page, except we're using "f_b" instead of "f_P." The term f_b is called the *half-power* frequency, the *corner* frequency, the *break* frequency, or the *3-dB* frequency.

Gain Magnitude in dB:

From:

$$|A_v| = \frac{1}{\sqrt{1^2 + \left(\frac{f}{f_b}\right)^2}} \quad \textbf{(249)}$$

We obtain:

$$|A_v|_{dB} = 20\log\frac{1}{\sqrt{1^2+\left(\frac{f}{f_b}\right)^2}} = 20\log(1) - 20\log\sqrt{1^2+\left(\frac{f}{f_b}\right)^2} \quad \textbf{(250)}$$

$$= -20\log\sqrt{1^2+\left(\frac{f}{f_b}\right)^2} = -10\log\left[1+\left(\frac{f}{f_b}\right)^2\right]$$

Bode Magnitude Plot:

From eq. (250), at *low* frequencies ($f/f_b << 1$):

$$|A_v|_{dB} = -10\log(1) = 0 \text{ dB} \quad \textbf{(251)}$$

And, at *high* frequencies ($f/f_b >> 1$):

$$|A_v|_{dB} = -10\log\left(\frac{f}{f_b}\right)^2 = -20\log\left(\frac{f}{f_b}\right) \quad \textbf{(252)}$$

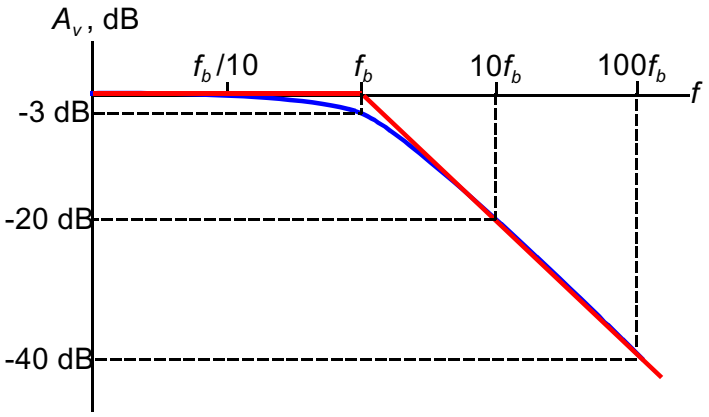

Fig. 241. Bode magnitude plot for single-pole low-pass, in red. The actual curve is shown in blue.

Note that the latter equation decreases 20 dB for each factor of 10 increase in frequency (i.e., -20 db per *decade*).

Bode Phase Plot:

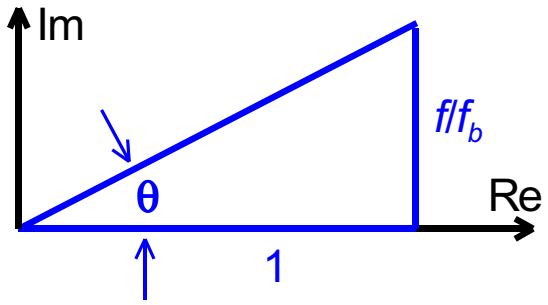

Fig. 242. Trigonometric representation of transfer function phase angle.

From the transfer function:

$$A_v = \frac{1}{1 + j\dfrac{f}{f_b}} \qquad \textbf{(253)}$$

The transfer function phase angle is:

$$\theta_{A_v} = -\arctan\frac{f}{f_b} \qquad \textbf{(254)}$$

The Bode phase plot shows the characteristic shape of this inverse tangent function:

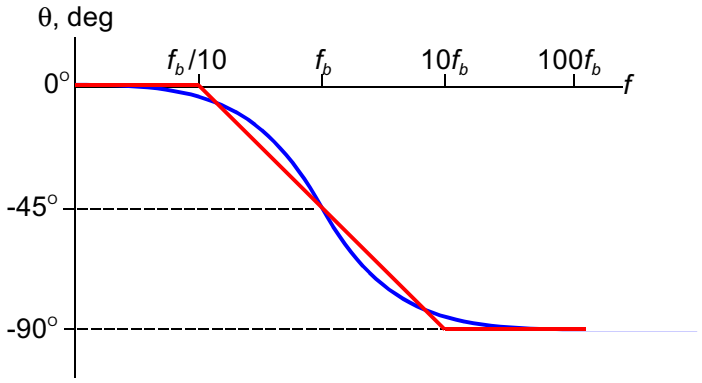

Fig. 243. Bode phase plot for single-pole low-pass, shown in red. The actual curve is shown in blue.

Single-Pole High-Pass RC

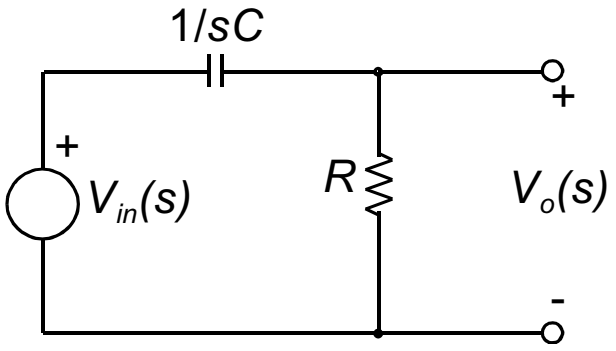

Fig. 244. Single-pole high-pass RC circuit.

The s-domain transfer function:

$$A_v = \frac{R}{\frac{1}{sC}+R} = \frac{sRC}{sRC+1} \qquad (255)$$

Note there is a pole at $s = -1/RC$, and a zero at $s = 0$.

For the sinusoidal steady state response we substitute $j2\pi f$ for s:

$$A_v = \frac{j(2\pi RC)f}{1+j(2\pi RC)f} = \frac{j\frac{f}{f_b}}{1+j\frac{f}{f_b}} \quad \text{where} \quad f_b = \frac{1}{2\pi RC} \qquad (256)$$

Bode Magnitude Plot:

Because this is a review, we go directly to the resulting gain equation:

$$|A_v|_{dB} = 20\log\left(\frac{f}{f_b}\right) - 20\log\sqrt{1+\left(\frac{f}{f_b}\right)^2} \qquad (257)$$

Recall from Fig. (234) that the first term is a straight line, with +20 dB/dec slope, passing through 0 dB at f_b.

The last term is *the same term* from the low pass example, which has the form of Fig. (236).

The total Bode magnitude response is merely the sum of these two responses.

Adding the two individual responses gives:

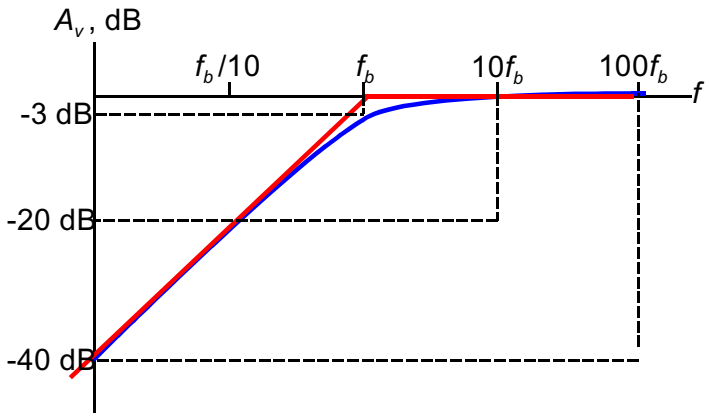

Fig. 245. Bode magnitude plot for single-pole high pass, in red. The actual curve is shown in blue.

Bode Phase Plot:

The transfer function leads to the following phase equation:

$$\theta_{A_v} = 90° - \arctan\frac{f}{f_b} \qquad \textbf{(258)}$$

This is just the low-pass phase plot shifted upward by 90°:

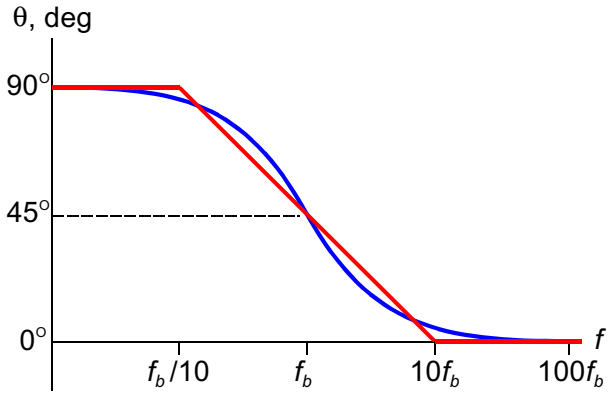

Fig. 246. Bode phase plot for single-pole high-pass, in red. The actual curve is shown in blue.

Coupling Capacitors

Effect on Frequency Response

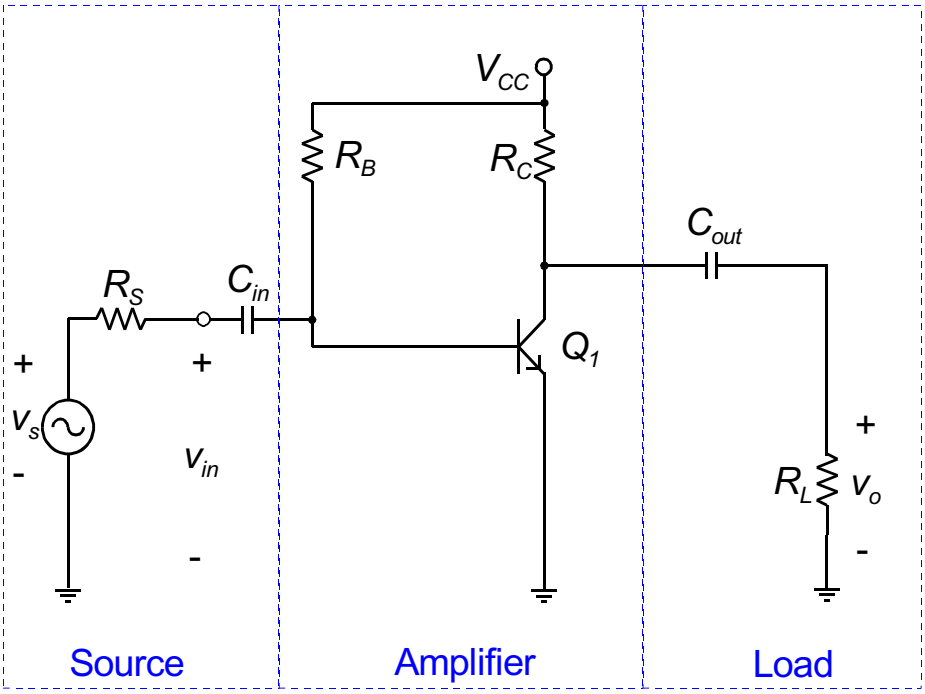

Fig. 247. Representative amplifier circuit, split into sections.

In our *midband amplifier analysis*, we assumed the capacitors were short circuits, drew the small-signal equivalent, and analyzed it for overall gain (or other parameters). This time, though:

(1) we can draw the sm. sig. eq. ckt. of the amplifier section *only*,

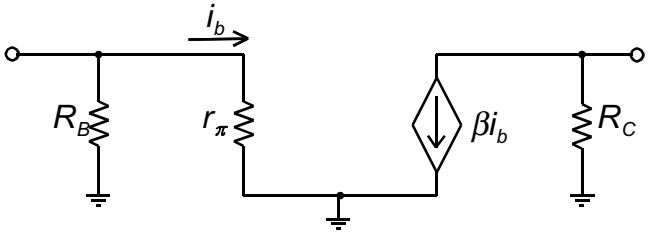

Fig. 248. Amplifier sm. sig. eq. ckt.

(2) analyze it, determine the its model parameters, and . . .

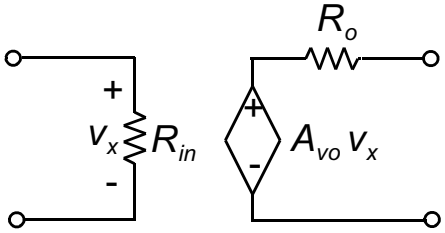

Fig. 249. Model equivalent to amplifier section.

. . . (3) redraw the *entire* circuit (Fig. 247) as shown:

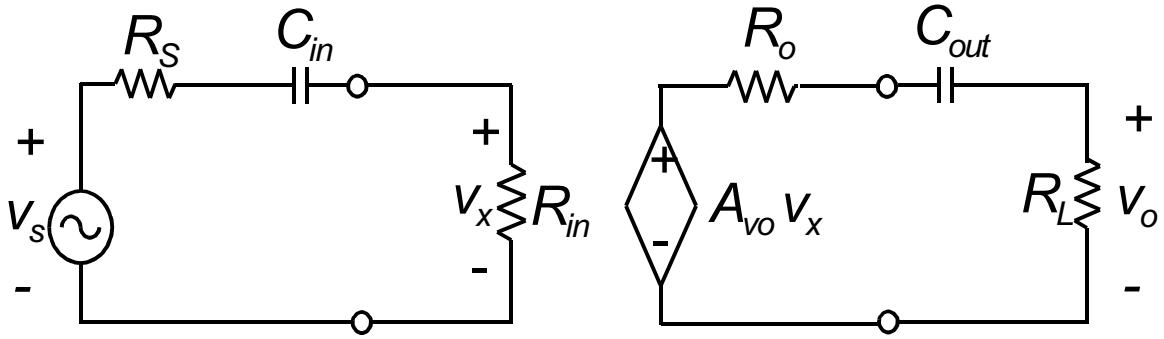

Fig. 250. Complete circuit redrawn with amplifier section replaced by its model.

Note that both sides are identical topologically, and are *single-pole, high-pass circuits*:

On the left:	On the right:
$f_1 = \dfrac{1}{2\pi C_{in}\left(R_S + R_{in}\right)}$ **(259)**	$f_2 = \dfrac{1}{2\pi C_{out}\left(R_o + R_L\right)}$ **(260)**

At frequencies above f_1 and f_2, the Bode magnitude plots from these high-pass circuits are simply horizontal lines at 0 dB, which add to become a single horizontal line at 0 dB. Of course, the amplifier (and resistive dividers) will shift this horizontal line (hopefully upward, because we probably want $A_v > 1$). .

Suppose we begin somewhere *above* f_1 and f_2 - *at midband* . . . we already know how to find the midband gain, which will become $20\log A_{v_{mid}}$ on the Bode magnitude plot.

Now let's work our way *lower* in frequency. . . when we get to the first of the two pole frequencies, our Bode magnitude plot begins to drop at 20 dB/decade. . . when we get to the second pole, the plot drops at 40 dB/decade. . . see the illustration on the next page.

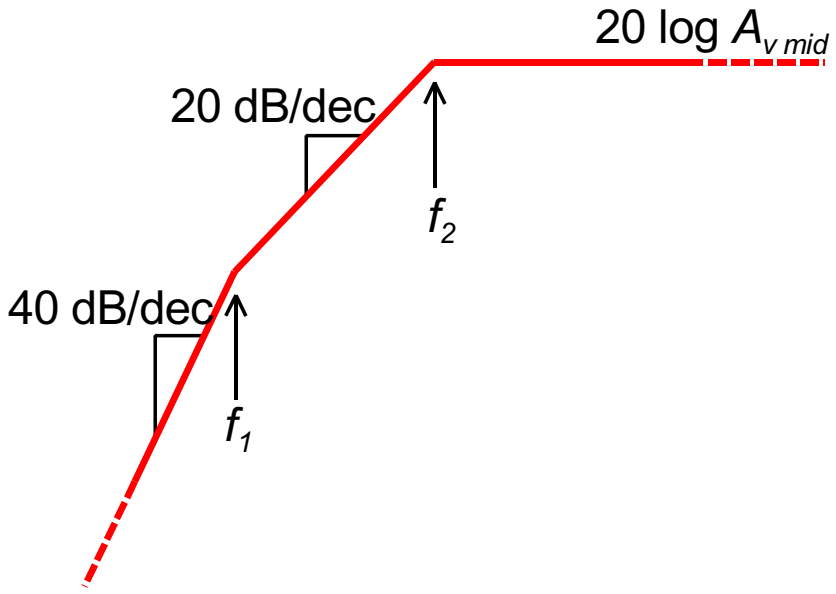

Fig. 251. Generalized Bode magnitude plot of an amplifier with coupling capacitors. Here f_1 is assumed to be lower than f_2.

Note that the presence of f_1 moves the overall half-power frequency above f_2.

Constructing the Bode Magnitude Plot for an Amplifier

1. Analyze the circuit with the coupling capacitors replaced by short circuits to find the midband gain.

2. Find the break frequency due to each coupling capacitor.

3. Sketch the Bode magnitude plot by beginning in the midband range and moving toward lower frequencies.

Design Considerations for *RC*-Coupled Amplifiers

1. *RC*-Coupled amplifiers:

Coupling capacitors - capacitors cost $

Direct-Coupled amplifiers:

No capacitors - bias circuits interact - more difficult design, but preferable.

2. Determine Thevenin resistance "seen" by each coupling capacitor.

Larger resistances mean smaller and cheaper capacitors.

3. Choose f_b for each *RC* circuit to meet overall -3 dB requirement.

Judicious choice can reduce overall cost of capacitors.

4. Calculate required capacitance values.

5. Choose C values somewhat larger than calculated (approximately 1.5 times larger).

Some C tolerances are as much as -20%, +80 %. Vales can change $\pm$10 % with time and temperature.

Low- & Mid-Frequency Performance of CE Amplifier

Introduction

We begin with two of the most common topologies of common-emitter amplifier:

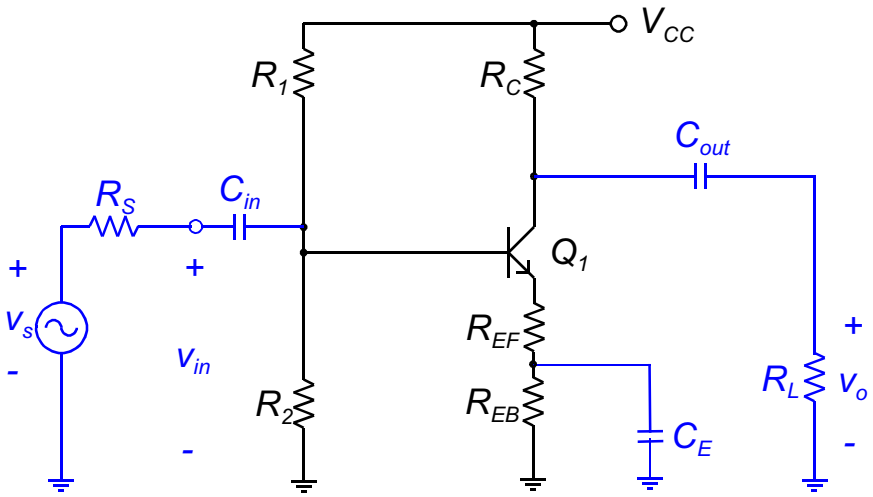

Fig. 252. Generic single-supply common emitter ckt.
(Let $R_B = R_1 \parallel R_2$, $R_L' = R_L \parallel R_C$, $R_E = R_{EF} + R_{EB}$)

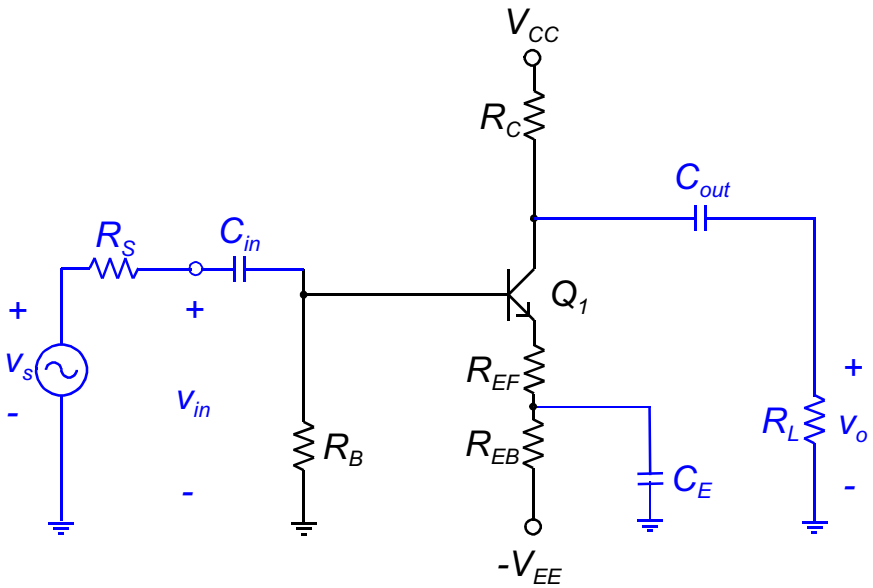

Fig. 253. Generic dual-supply common emitter ckt.
(Let $R_L' = R_L \parallel R_C$, $R_E = R_{EF} + R_{EB}$)

Both common-emitter topologies have the same small-signal equivalent circuit:

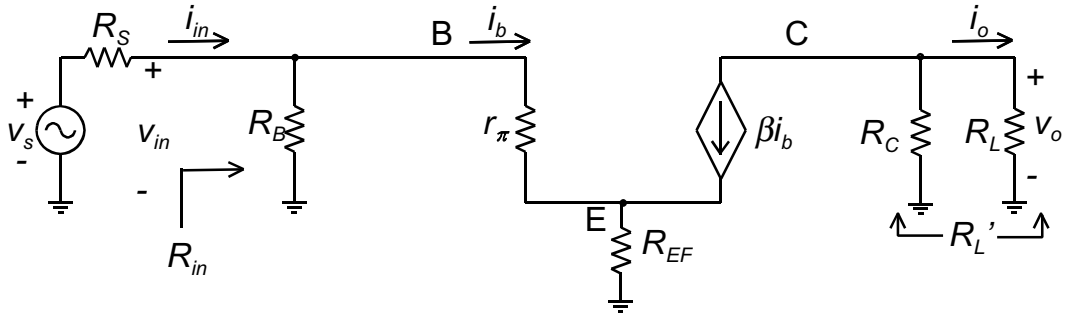

Fig. 254. Generic small-signal equivalent of common emitter amplifier.

Midband Performance

$$A_v = \frac{v_o}{v_{in}} = \frac{-\beta R_L'}{r_\pi + (\beta+1)R_{EF}} \approx \frac{-R_L'}{R_{EF}}, \quad \text{if } \beta >> 1 \tag{261}$$

$$A_{v_s} = \frac{v_o}{v_s} = A_v \frac{R_{in}}{R_S + R_{in}} \tag{262}$$

$$R_{in} = \frac{v_{in}}{i_{in}} = R_B \| \left[r_\pi + (\beta+1)R_{EF} \right] \tag{263}$$

For the equivalent circuit shown, $R_o = R_C$, but if we include the BJT output resistance r_o in the equivalent circuit, the calculation of R_o becomes much more involved. We'll leave this topic with the assumption that $R_o \approx R_C$.

The focus has been A_v, but we can determine A_i also:

$$A_i = \frac{i_o}{i_{in}} = \frac{v_o / R_L}{v_{in} / R_{in}} = A_v \frac{R_{in}}{R_L} = -\beta \frac{R_C}{R_C + R_L} \frac{R_B}{R_B + R_X} \tag{264}$$

where $R_X = r_\pi + (\beta + 1)R_{EF}$.

Design Considerations

- In choosing a device we should consider:

  Frequency performance

  Noise figure

  Power Dissipation

  Device choice may not be critical. . .

- Design Tradeoffs:

  1. R_B large for high R_{in} and high A_i
     R_B small for bias (Q-pt.) stability
  2. R_C large for high A_v and A_i
     R_C small for low R_o , low signal swing, high frequency response
  3. R_{EF} small (or zero) for maximum A_v and A_i
     $R_{EF} > 0$ for larger R_{in} , *gain stability*, improved high and low frequency response, reduced distortion

- Gain Stability:

  Note from eq. (261), as R_{EF} increases, $A_v \approx -R_L'/R_{EF}$, i.e., gain becomes independent of β *!!!*

The Effect of the Coupling Capacitors

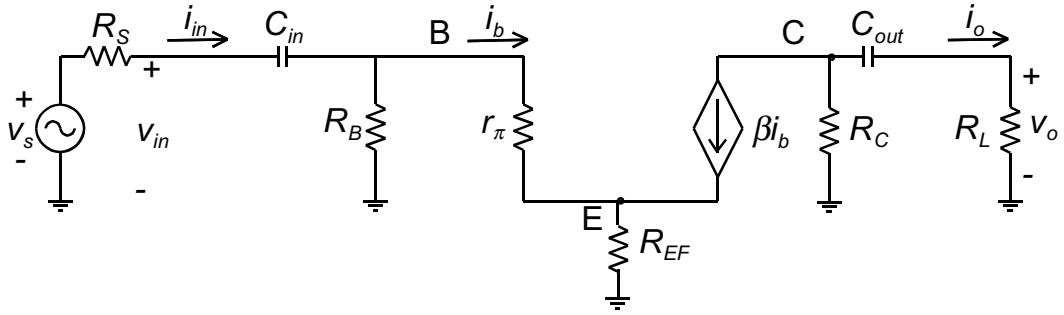

Fig. 255.Approximate sm. sig. equivalent of the CE amplifier at low frequencies. The effect of C_E is ignored by replacing it with a short circuit. C_{in} and C_{out} remain so that their effect can be determined.

To determine the effect of the coupling capacitors, we approximate the small-signal equivalent as shown. C_{in} and C_{out} are then a part of independent single-pole high-pass circuits, with break frequencies of:

$$f_b = \frac{1}{2\pi R_{Thevenin} C} \tag{265}$$

Thus the effect of C_{out} is:

$$f_{out} = \frac{1}{2\pi\left(R_C + R_L\right)C_{out}} \tag{266}$$

And the effect of C_{in} is:

$$\text{for } A_v = \frac{v_o}{v_{in}} \qquad f_{in} = \frac{1}{2\pi R_{in} C_{in}} \tag{267}$$

$$\text{for } A_v = \frac{v_o}{v_s} \qquad f_{in} = \frac{1}{2\pi\left(R_S + R_{in}\right)C_{in}} \tag{268}$$

Equations for f_{in} are approximate, because the effects of C_{in} and C_E interact slightly. The interaction is almost always negligible.

The Effect of the Emitter Bypass Capacitor C_E

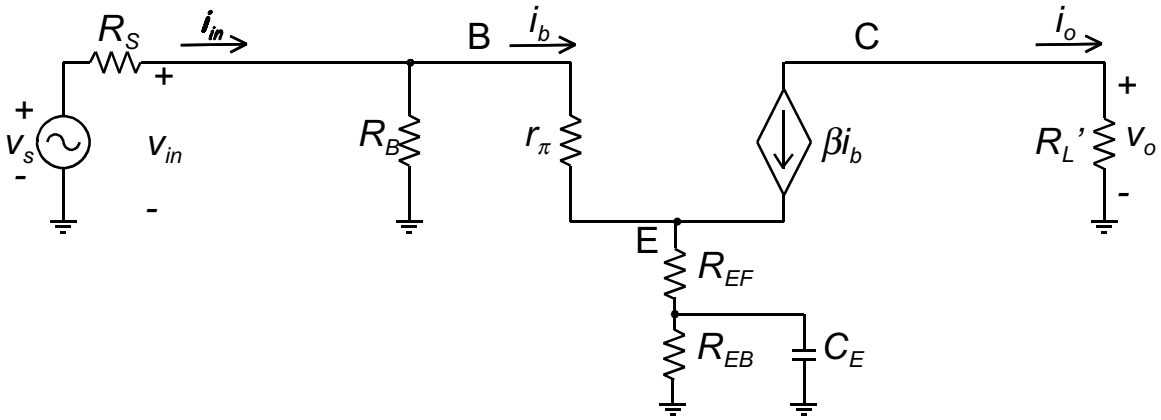

Fig. 256. Approximate common emitter sm. sig. equivalent at low frequencies. Only the effect of C_E is accounted for in this circuit.

Consider the following:

At sufficiently high frequencies, C_E appears as a short circuit. Thus the total emitter resistance is at its lowest, and A_v is at its highest. This appears like, and is, the standard single-pole high-pass effect.

At sufficiently low frequencies C_E appears as an open circuit. The total emitter resistance is at its highest, and A_v is at its lowest, *but A_v is not zero!!!* Thus, there is not just a single-pole high-pass effect. *There must also be a zero at a frequency other than f = 0*, as shown below:

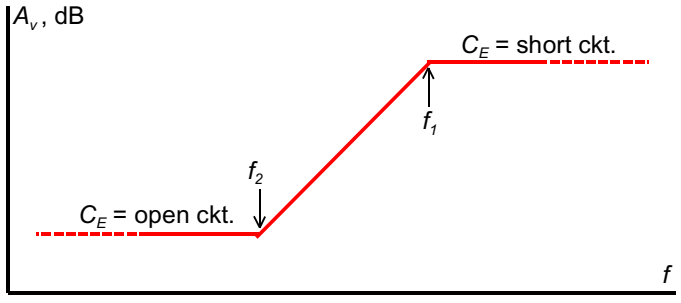

Fig. 257. Bode magnitude plot showing the effect of C_E only.

To find the pole frequency f_1 we need the Thevenin resistance "seen" by C_E:

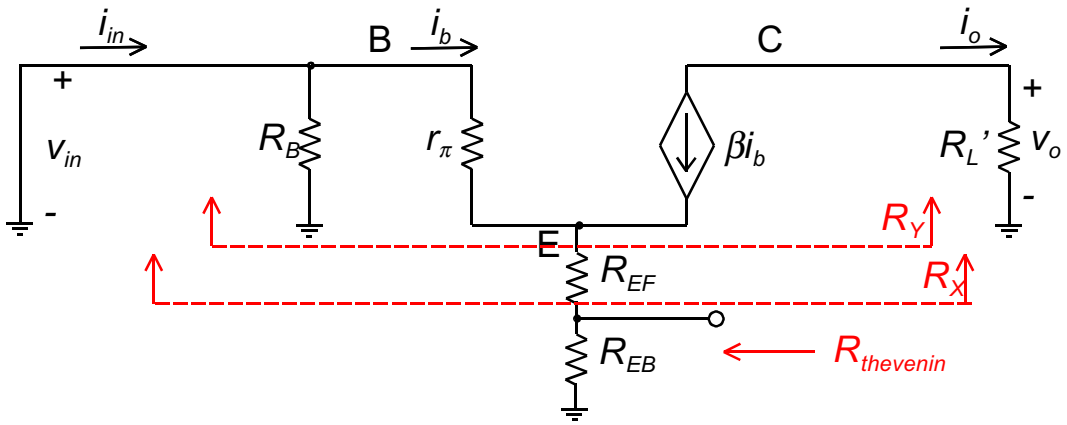

Fig. 258. Finding Thevenin R "seen" by C_E, assuming we are interested in v_o/v_{in}, i.e., assuming $R_S = 0$.

From inspection we should see that:

$$R_{Thevenin} = R_{EB} || R_X = R_{EB} || (R_{EF} + R_Y) \tag{269}$$

The difficulty is finding R_Y, which is undertaken below:

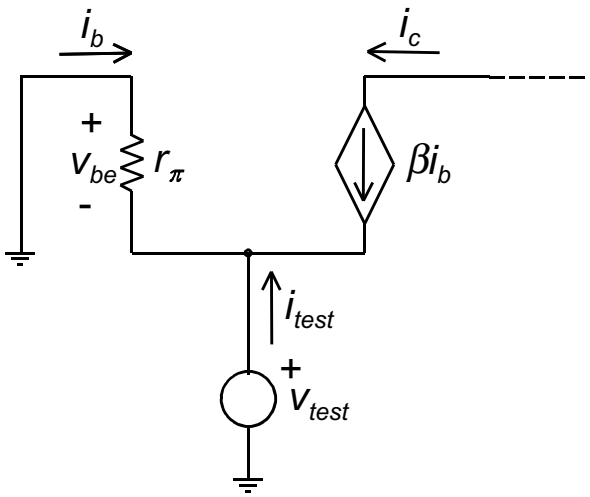

Fig. 259. Finding R_Y.

$$i_b = \frac{v_{be}}{r_\pi} = -\frac{v_{test}}{r_\pi} \tag{270}$$

$$i_{test} = -(\beta + 1) i_b \tag{271}$$

$$R_Y = \frac{v_{test}}{i_{test}} = \frac{r_\pi}{\beta + 1} \tag{272}$$

If $R_S \neq 0$, then R_Y becomes:

$$R_Y = \frac{(R_B || R_S) + r_\pi}{\beta + 1} \tag{273}$$

Thus, for $A_v = v_o/v_{in}$:

$$f_1 = \frac{1}{2\pi C_E\left[R_{EB}\|\left(R_{EF} + \frac{r_\pi}{\beta+1}\right)\right]} \quad \textbf{(274)}$$

Or, for $A_v = v_o/v_s$:

$$f_1 = \frac{1}{2\pi C_E\left[R_{EB}\|\left(R_{EF} + \frac{r_\pi + (R_B\|R_S}{\beta+1}\right)\right]} \quad \textbf{(275)}$$

The zero f_2 is the frequency where $Z_E(jf_2) = R_E\|\frac{1}{jf_2C_E} = \infty$:

$$f_2 = \frac{1}{2\pi C_E R_{EB}} \quad \textbf{(276)}$$

The mathematical derivation of eq. (276) is not a focus of this course; it is left for your own endeavor.

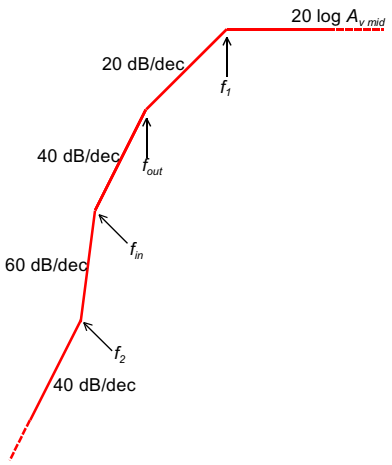

Fig. 260. One example of the Bode plot of a CE amplifier.

The Bode magnitude plot of a common emitter amplifier is the summation of the effects of poles f_{in}, f_{out}, f_1, and the zero f_2.

One of many possible examples is shown at left.

The Miller Effect

Introduction

Before we can examine the high frequency response of amplifiers, we need some additional tools. The Miller Effect is one of them. Consider:

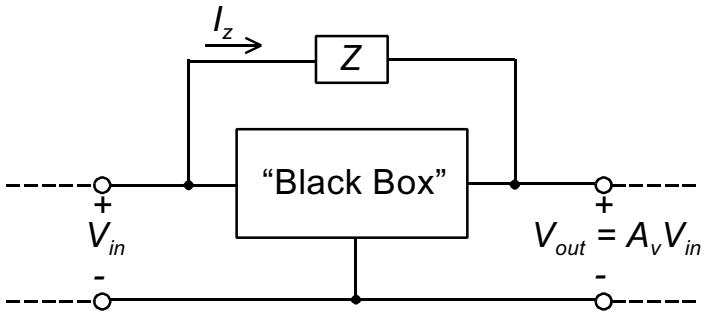

Fig. 261. Circuit with feedback impedance *Z*. The black box is usually an amplifier, but can be any network *with a common node*.

It is difficult to analyze a circuit with a feedback impedance, so we wish to find a circuit that is equivalent at the input & output ports:

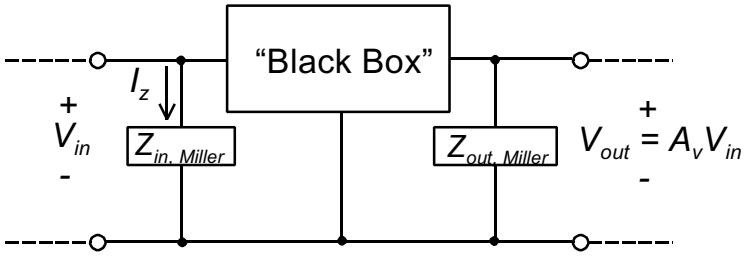

Fig. 262. Circuit to be made equivalent to the previous figure.

If we can choose $Z_{in.\ Miller}$ so that I_z is the same in both circuits, the input port won't "know" the difference - the circuits will be equivalent at the input port.

Deriving the Equations

From Fig. 261:

$$I_Z = \frac{V_{in} - V_o}{Z} = \frac{V_{in} - A_v V_{in}}{Z} = \frac{V_{in}(1 - A_v)}{Z} \quad \textbf{(277)}$$

And from Fig. 262:

$$I_Z = \frac{V_{in}}{Z_{in,\,Miller}} \quad \textbf{(278)}$$

Setting eqs. (277) and (278) equal, and solving:

$$Z_{in,\,Miller} = \frac{Z}{1 - A_v} \quad \textbf{(279)}$$

Using a similar approach, the circuits can be made equivalent at the output ports, also, if:

$$Z_{out,\,Miller} = Z\frac{A_v}{A_v - 1} = Z\frac{1}{1 - \frac{1}{A_v}} \quad \textbf{(280)}$$

Notes:

1. Though not explicitly shown in the derivation, A_v and all the impedances can be complex (i.e., *phasors*).

2. If $|A_v|$ is, say, 10 or larger, then $Z_{out,\,Miller} \approx Z$.

3. If $A_v > 1$ and real, then $Z_{in,\,Miller}$ is *negative!!!* This latter phenomenon is used, among other things, to construct oscillators.

The Hybrid-π BJT Model

The Model

This is another tool we need before we examine the high frequency response of amplifiers.

The hybrid-π BJT model includes elements that are negligible at low frequencies and midband, but cannot be ignored at higher frequencies of operation:

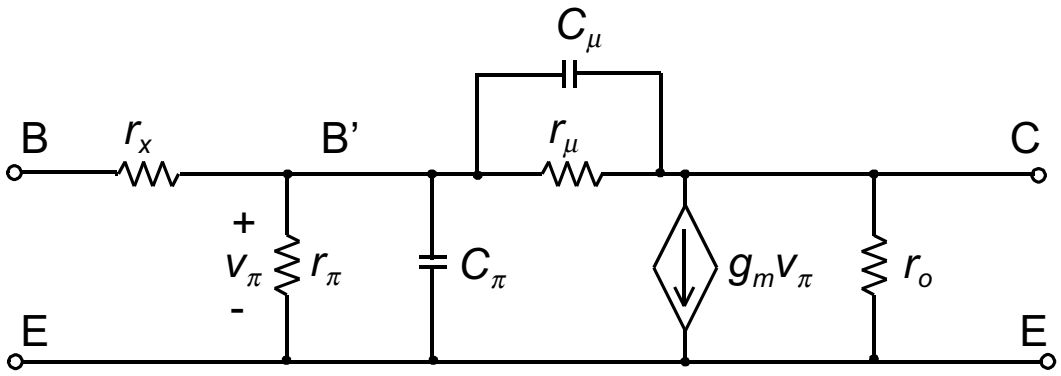

Fig. 263. Hybrid-π model of BJT.

r_x = ohmic resistance of base region, $\approx$ a few tens of ohms

r_π = dynamic resistance of base region, as described previously

r_o = collector resistance of BJT, as described previously

r_μ, C_μ represent the characteristics of the reverse-biased collector-base junction:

$r_\mu \approx$ several Megohms $\qquad C_\mu \approx$ 1 pF to 10 pF

C_π = diffusion capacitance of b-e junction, $\approx$ 100 pF to 1000 pF

g_m = BJT transconductance; we can show that $g_m = \beta/r_\pi = I_{CQ}/V_T$

Effect of C_π and C_μ

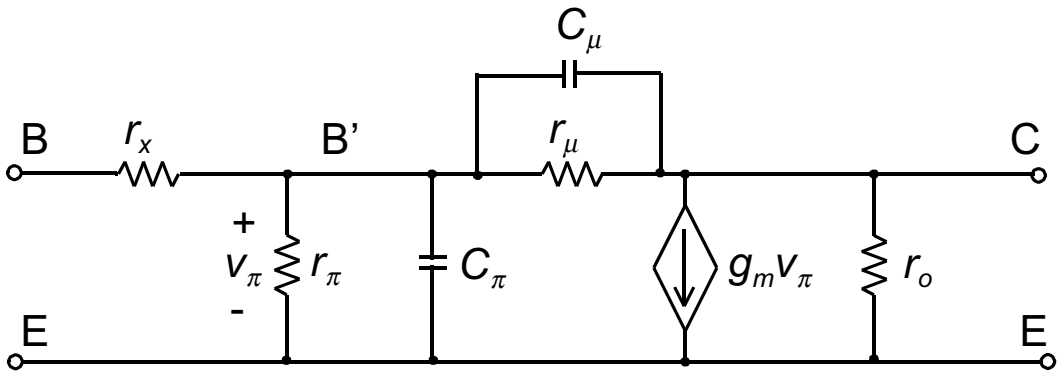

Fig. 264. Hybrid-π model of BJT (Fig. 263 repeated).

Notice the small values of C_π and C_μ, especially when compared to typical values of C_{in}, C_{out}, and C_E.

At low and midband frequencies, C_π and C_μ appear as open circuits.

At high frequencies, where C_π and C_μ have an effect, C_{in}, C_{out}, and C_E appear as short circuits.

To focus our attention, we'll assume $r_x \approx 0$ and $r_\mu \approx \infty$, and we'll use the Miller Effect to replace C_μ:

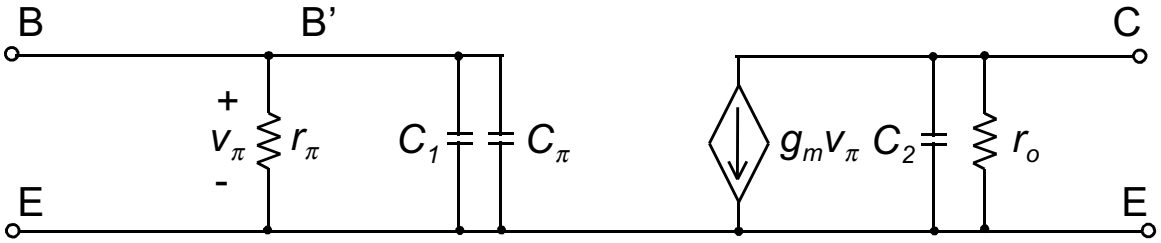

Fig. 265. Simplified hybrid-π BJT model using the Miller Effect and the other assumptions described in the text..

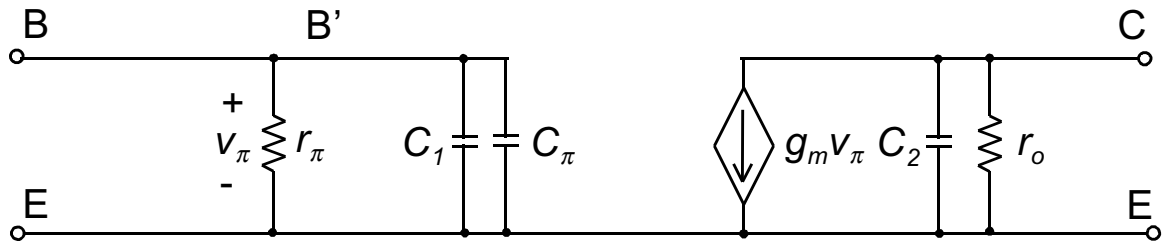

Fig. 266. Miller Effect applied to hybrid-π model (Fig. 265 repeated).

From the Miller Effect equations, (279) and (280):

$$C_1 = C_\mu (1 - A_v) \approx |A_v| C_\mu \qquad \textbf{(281)}$$

$$C_2 = C_\mu \left(1 - \frac{1}{A_v}\right) \approx C_\mu \qquad \textbf{(282)}$$

Individually, all *C*s in Fig. 266 have a *single-pole low-pass effect*. As frequency increases they become short circuits, and v_o approaches zero .

Thus there are two low-pass poles with the mathematical form:

$$f_b = \frac{1}{2\pi C_{eq} R_{Thevenin}} \qquad \textbf{(283)}$$

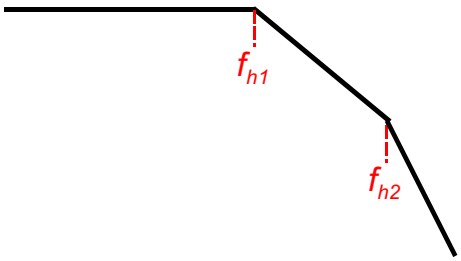

Fig. 267. Typical amplifier response in the midband and high-frequency regions. f_{h1} is normally due to $C_1 + C_\pi$, and f_{h2} is normally due to C_2.

Because $C_1 + C_\pi >> C_2$, the pole due to $C_1 + C_\pi$ will dominate. The pole due to C_2 is usually negligible, especially when R_L' is included in the circuit.

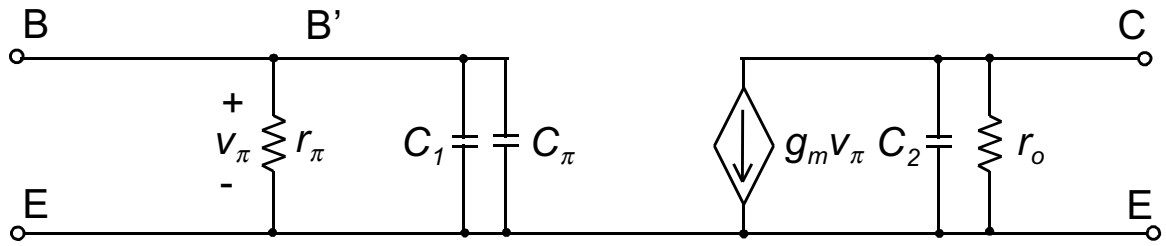

Fig. 268. Miller Effect applied to hybrid-π model (Fig. 265 repeated).

The overall half-power frequency, then, is usually due to $C_1 + C_\pi$:

$$f_H \approx f_{h1} = \frac{1}{2\pi\left(C_1 + C_\pi\right)R_{Thevenin}} \qquad \textbf{(284)}$$

For typical transistors, $C_1 > C_\pi$. For a moment, let us be *very* approximate and presume that C_π is negligibly small. Then:

$$f_H \approx \frac{1}{2\pi C_1 R_{Thevenin}} \approx \frac{1}{2\pi \left|A_v\right| C_\mu R_{Thevenin}} \qquad \textbf{(285)}$$

i.e., *f_H is approximately inversely proportional to $|A_v|$!!!*

Amplifiers are sometimes rated by their *Gain-Bandwidth Product*, which is approximately constant. This is especially true for high gains where C_1 dominates.

High-Frequency Performance of CE Amplifier

The Small-Signal Equivalent Circuit

We now have the tools we need to analyze (actually, *estimate*) the high-frequency performance of an amplifier circuit. We choose the common-emitter amplifier to illustrate the techniques:

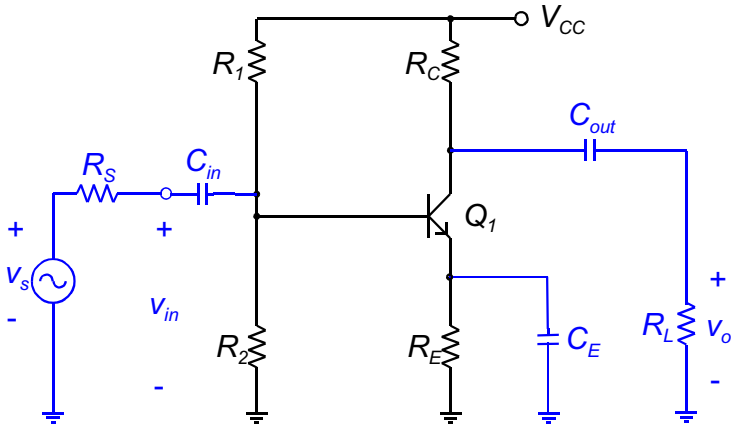

Fig. 269. Standard common emitter amplifier (Fig. 208 repeated).

Now we use the hybrid-π equivalent for the BJT and construct the small-signal equivalent circuit for the amplifier:

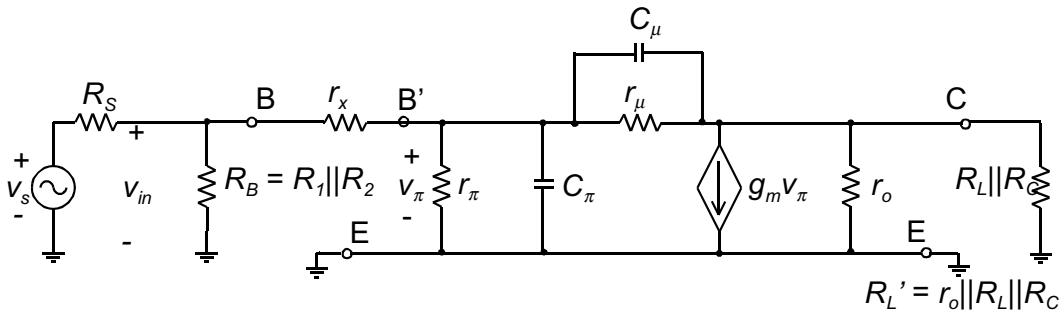

Fig. 270. Amplifier small-signal equivalent circuit using hybrid-π BJT model.

High-Frequency Performance

We can simplify the circuit further by using a Thevenin equivalent on the input side, and by assuming the effect of r_μ to be negligible:

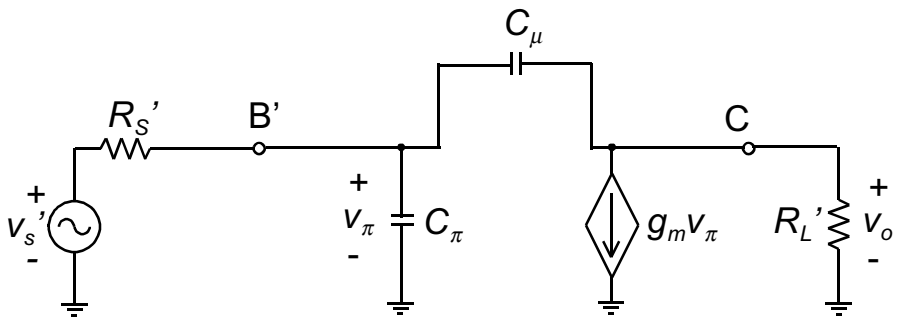

Fig. 271. Modified small-signal equivalent, using a Thevenin equivalent on the input side, and assuming r_μ is infinite.

Note that the Thevenin resistance $R_s' = r_\pi \,||\, [r_x + (R_B||R_S)]$

Recognizing that the dominant high-frequency pole occurs on the input side, we endeavor only to calculate f_{h1}. Thus we ignore the effect of C_μ on the output side, calculate the voltage gain, and apply the Miller Effect on the input side only.

$$A_v = \frac{v_o}{v_\pi} \approx -g_m R_L' \qquad \textbf{(286)}$$

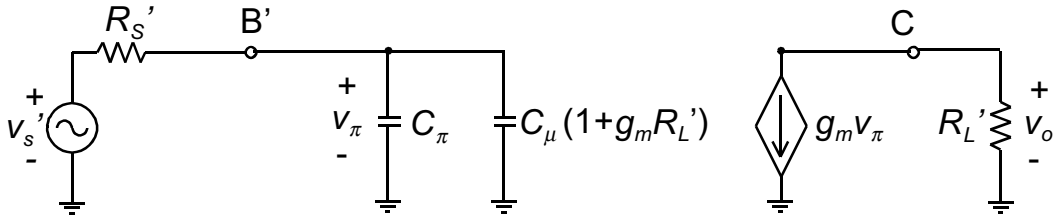

Fig. 272. Final (approximate) equivalent after applying the Miller Effect.

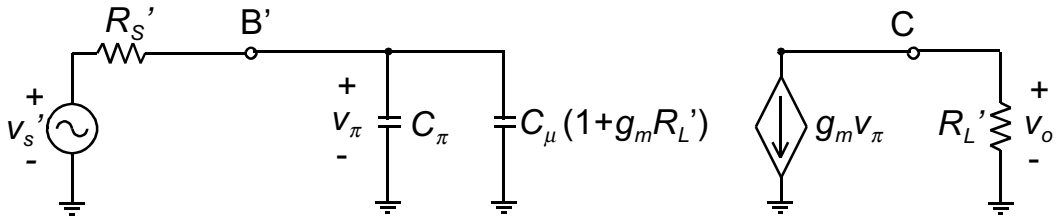

Fig. 273. Final (approximate) equivalent after applying the Miller Effect (Fig. 272 repeated).

So we have

$$f_{h1} = \frac{1}{2\pi R_S' C_{total}} \tag{287}$$

where

$$C_{total} = C_\pi + C_\mu\left(1 + g_m R_L'\right) \tag{288}$$

and

$$R_S' = r_\pi \| \left[r_x + \left(R_B \| R_S \right) \right] \tag{289}$$

The CE Amplifier Magnitude Response

Finally, we can estimate the entire Bode magnitude response of an amplifier. . . an example:

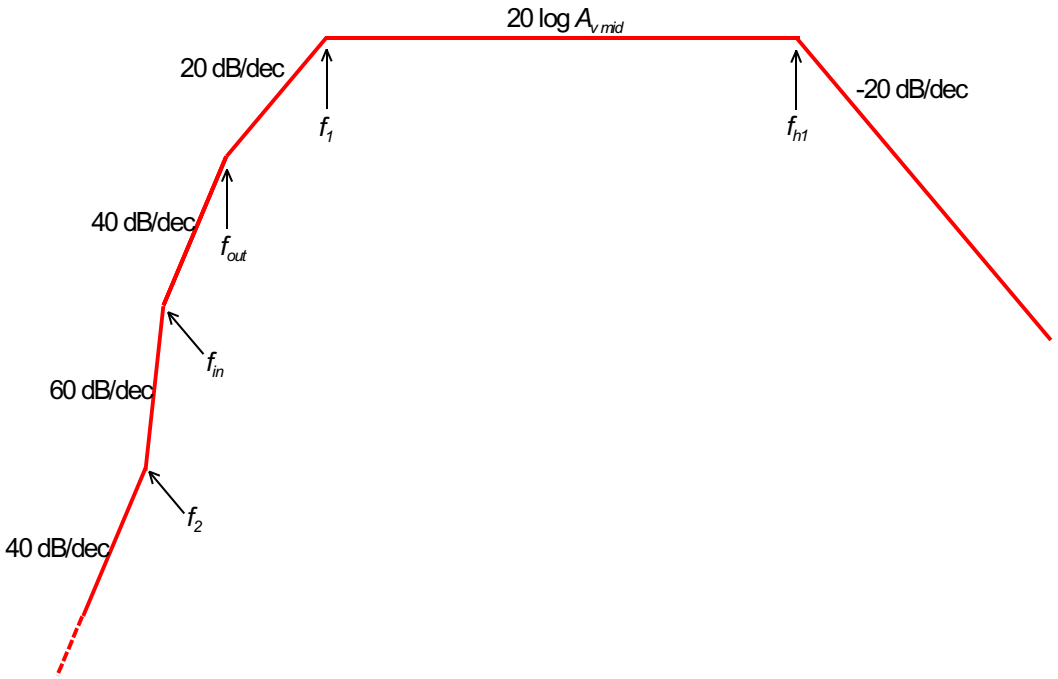

Fig. 274. One example of the entire Bode magnitude response of a common emitter amplifier.

Of this plot, the lower and upper 3-dB frequencies are the most important, as they determine the *bandwidth* of the amplifier:

$$BW = f_H - f_L \approx f_{h1} - f_1 \qquad \textbf{(290)}$$

where the latter approximation assumes that adjacent poles are far away.

We've estimated the frequency response of *only* one amplifier configuration, the common-emitter. The techniques, though, can be applied to any amplifier circuit.

Nonideal Operational Amplifiers

In addition to operational voltage amplifiers, there are operational current amplifiers and operational transconductance amplifiers (OTAs). This discussion is limited to voltage amplifiers.

Linear Imperfections

Input and Output Impedance:

Ideally, $R_{in} = \infty$ and $R_{out} = 0$.

Realistically, R_{in} ranges from $\approx$ 1 MΩ in BJT op amps to $\approx$ 1 TΩ in FET op amps.

R_{out} ranges from less than 100 Ω in general purpose op amps, to several kΩ in low power op amps.

Gain and Bandwidth:

Ideally, $A_v = \infty$ and BW = ∞.

Realistically, A_v ranges from 80 dB (10^4) to 140 dB (10^7).

Many *internally-compensated* op amps have their BW restricted to prevent oscillation, producing the Bode magnitude plot shown:

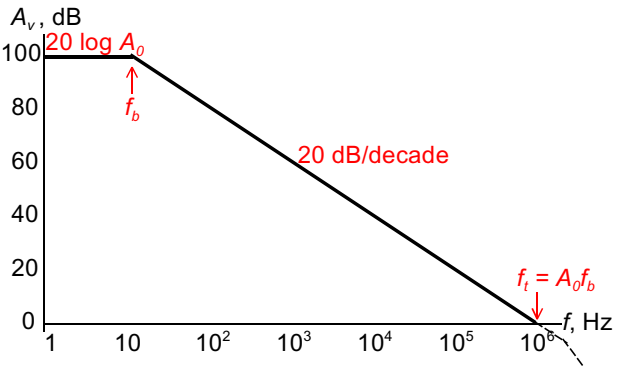

Fig. 275. Typical op amp Bode magnitude response.

The transfer function, then, has a single-pole, low-pass form:

$$A(s) = \frac{A_0}{\frac{s}{2\pi f_b} + 1} \qquad \textbf{(291)}$$

And gain-bandwidth product is constant:

$$f_t = A_0 f_b = A_{of} f_{bf} \qquad \textbf{(292)}$$

Nonlinear Imperfections

Output Voltage Swing:

BJT op amp outputs can swing to within $2V_{BE}$ of $\pm V_{SUPPLY}$.

FET op amp outputs an swing to within a few mV of $\pm V_{SUPPLY}$.

Output Current Limits:

Of course, currents must be limited to a "safe" value. Some op amps have internal current limit protection.

General purpose op amps have output currents in the range of tens of mA. For examples, the LM741 has an output current rating of ± 25 mA, while the LM324 can source 30 mA and sink 20 mA.

Slew-Rate Limiting:

This is the maximum rate at which v_O can change, $\left|\frac{dv_o}{dt}\right| \leq SR$. It is caused by a current source driving the compensation capacitor. As an example, the LM741 has a SR of ≈ 0.5 V/μs.

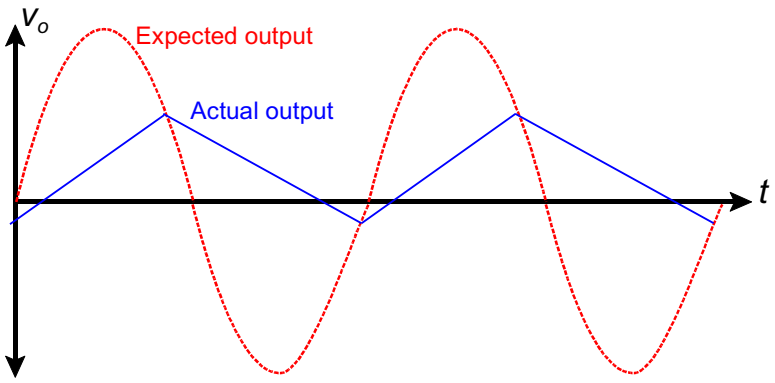

Fig. 276. Illustration of op amp *slew-rate limiting*.

Full-Power Bandwidth:

This is defined as the highest frequency for which an undistorted sinusoidal output is obtainable at maximum output voltage:

$$v_o(t) = V_{OM}\sin\omega t \quad \Rightarrow \quad \left.\frac{dv_o}{dt}\right|_{\max} = SR = \omega V_{OM} = 2\pi f V_{OM} \tag{293}$$

Solving for *f* and giving it a special notation:

$$f_{FP} = \frac{SR}{2\pi V_{OM}} \tag{294}$$

DC Imperfections:

Many of the concepts in this section are rightly credited to Prof. D.B. Brumm.

Input Offset Voltage, V_{IO}:

v_O is not exactly zero when v_I = 0. The input offset voltage V_{IO} is defined as the value of an externally-applied differential input voltage such that v_O = 0. It has a polarity as well as a magnitude.

Input Currents:

Currents into noninverting and inverting inputs are not exactly zero, but consist of base bias currents (BJT input stage) or gate leakage currents (FET input stage):

I_I^+, current *into* noninverting input

I_I^-, current *into* inverting input

These also have a polarity as well as a magnitude.

In general, $I_I^+ \neq I_I^-$, so we define the *input bias current* as the average of these, and the *input offset current* as the difference:

$$I_B = \frac{I_I^+ + I_I^-}{2} \qquad \text{and} \qquad I_{IO} = I_I^+ - I_I^- \tag{295}$$

Data sheets give maximum magnitudes of these parameters.

Modeling the DC Imperfections

The definitions of

- *input offset voltage*, V_{IO}
- *input bias current*, I_B
- and, *input offset current*, I_{IO}

lead to the following dc error model of the operational amplifier:

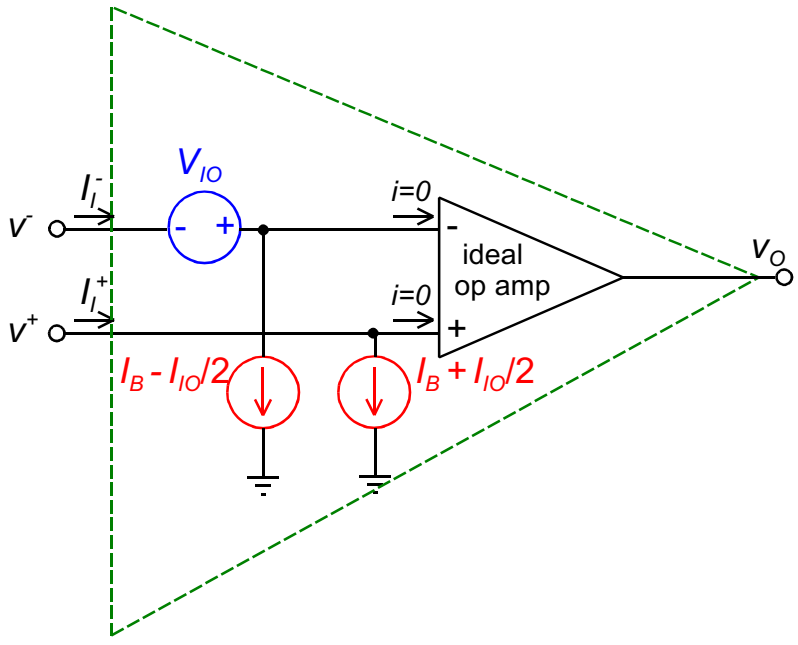

Fig. 277. DC error model of operational amplifier.

Using the DC Error Model

Recall the standard noninverting and inverting operational amplifier configurations. Note the presence of the resistor R^+. It is often equal to zero, especially if dc error does not matter.

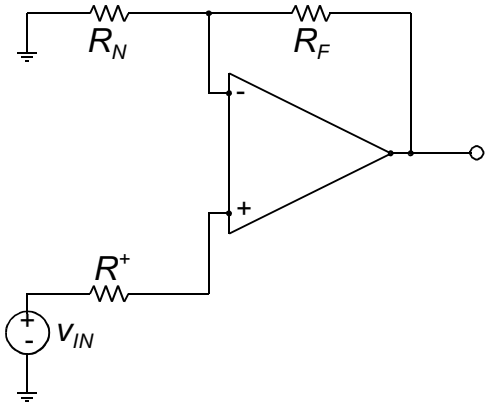

Fig. 278. Noninverting op amp configuration.

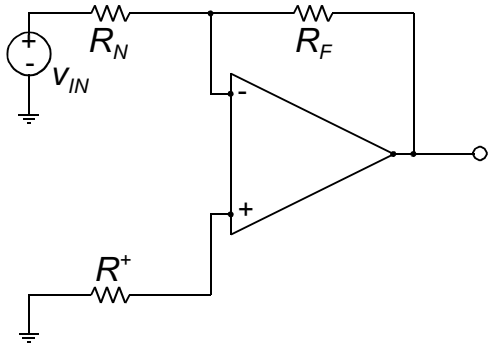

Fig. 279. Inverting op amp configuration.

Notice *that these circuits become identical* when we set the independent sources to zero:

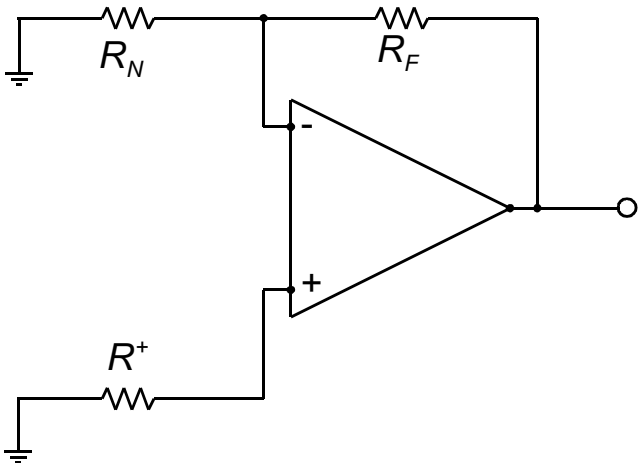

Fig. 280. Identical circuits result when the sources of Figs. 278 and 279 are set to zero.

Now, recall the dc error op amp model:

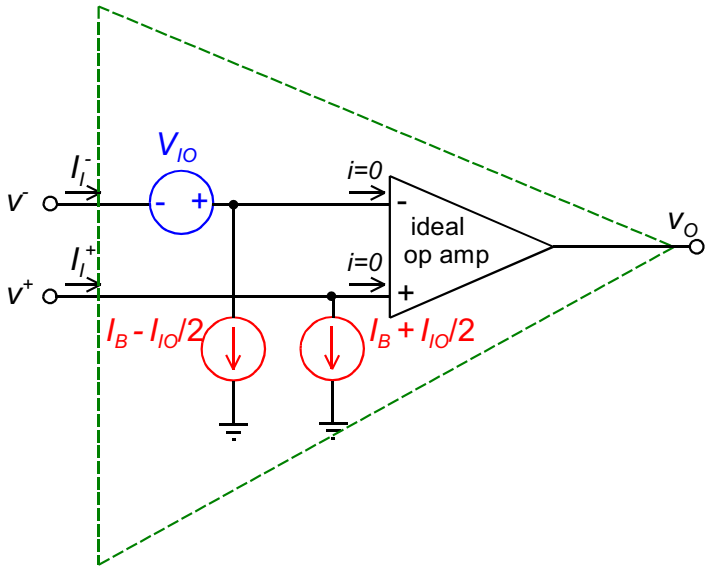

Fig. 281. DC error op amp model (Fig. 277 repeated).

And replace the ideal op amp of Fig. 280 with this model:

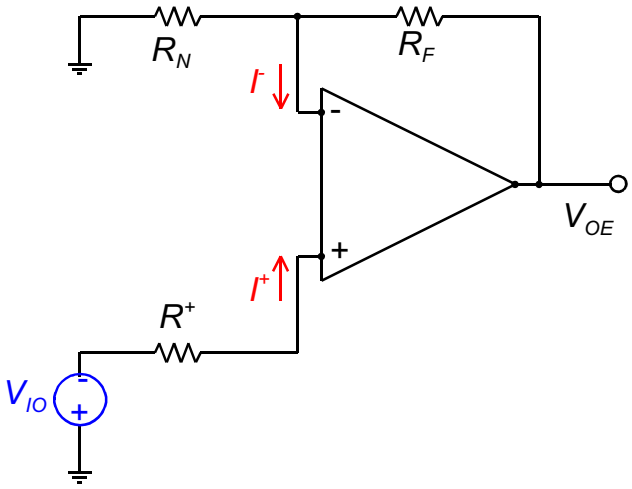

Fig. 282. Op amp noninverting and inverting amplifiers, external source set to zero, using dc error model.

With the help of Thevenin equivalents, *virtually all op amp circuits reduce to Fig. 282 when the external sources are set to zero* !!!

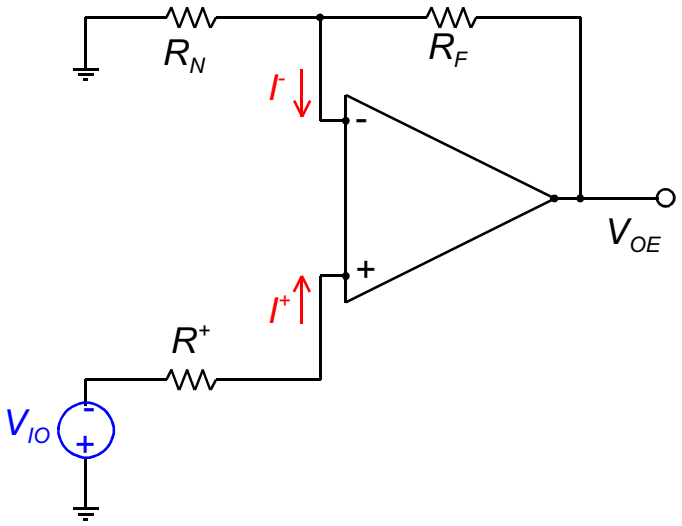

Fig. 283. Op amp configurations, with external source set to zero, using dc error model. (Fig. 282 repeated)

Note that the source V_{IO} can be "slid" in series anywhere in the input loop.

Also note carefully the polarity of V_{IO}.

And, finally, note that the dc error current sources have been omitted for clarity. Currents resulting from these sources are shown in red.

We can now determine the dc output error for virtually <u>any</u> op amp configuration. We have already noted the dc output error as $\boldsymbol{V_{OE}}$.

Using superposition, we'll first set I^- to zero. The voltage at the noninverting input is

$$v^+ = -V_{IO} - R^+ I^+ \tag{296}$$

This voltage is simply the input to a noninverting amplifier, so the dc output error, from these two error components alone, is:

$$V_{OE,\text{ Part A}} = -\left(1 + \frac{R_F}{R_N}\right)\left(V_{IO} + R^+ I^+\right) \tag{297}$$

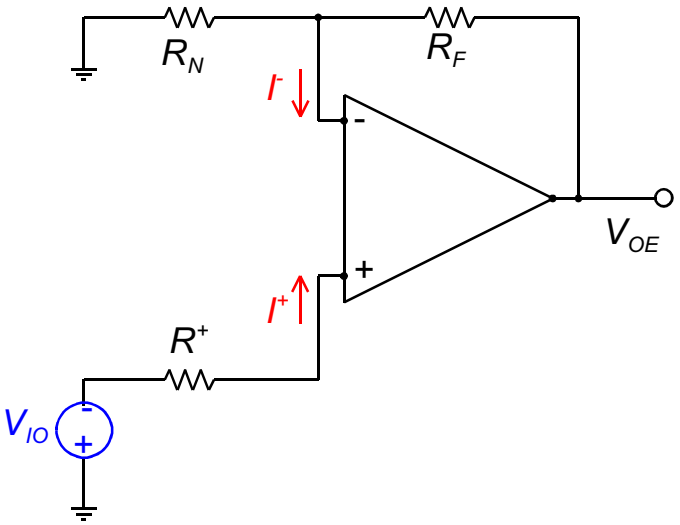

Fig. 284. Op amp configurations, with external source set to zero, using dc error model. (Fig. 282 repeated)

Next, we consider just I^-, i.e., we let $V_{IO} = 0$ and $I^+ = 0$.

Now $v^+ = v^- = 0$, so there is no current through R_N.

The current I^- must flow through R_F, creating the dc output error component:

$$V_{OE,\text{ Part B}} = R_F I^- \qquad \textbf{(298)}$$

Now we make use of a mathematical "trick." To permit factoring, we write (298) as:

$$V_{OE,\text{ Part B}} = \frac{R_N + R_F}{R_N}\frac{R_N}{R_N + R_F} R_F I^- = \left(1 + \frac{R_F}{R_N}\right) R^- I^- \qquad \textbf{(299)}$$

where

$$R^- = \frac{R_N}{R_N + R_F} R_F = R_F \| R_N \qquad \textbf{(300)}$$

And, finally, we combine (297) and (299) to obtain the totally general result:

$$V_{OE} = -\left(1 + \frac{R_F}{R_N}\right)\left(V_{IO} + R^+ I^+ - R^- I^-\right) \qquad \textbf{(301)}$$

DC Output Error Example

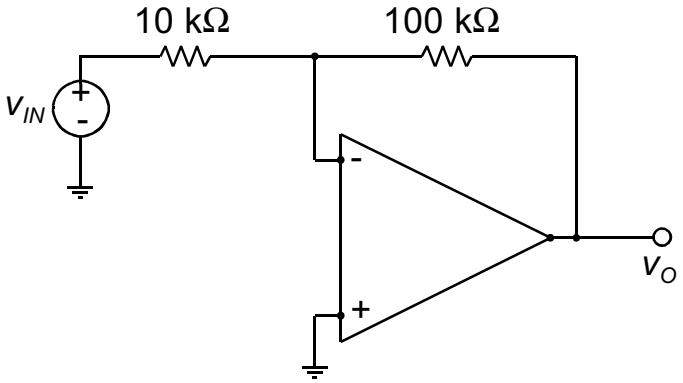

Fig. 285. DC output error example.

The maximum bias current is 100 nA, i.e.,

$$I_B \in [0, 100]\,\text{nA} \tag{302}$$

A positive value for I_B means *into* the chip.

The maximum offset current *magnitude* is 40 nA, i.e.,

$$I_{IO} \in [-40, 40]\,\text{nA} \tag{303}$$

Note that the polarity of I_{IO} is unknown.

The maximum offset voltage *magnitude* is 2 mV, i.e.,

$$V_{IO} \in [-2, 2]\,\text{mV} \tag{304}$$

Note also that the polarity of V_{IO} is unknown.

Finding Worst-Case DC Output Error:

- Setting v_{IN} to 0, and comparing to Fig. 282 and eq. (301):

$$V_{OE} = -\left(1 + \frac{R_F}{R_N}\right)\left(V_{IO} - R^- I^-\right) \tag{305}$$

where $(1 + R_F/R_N) = 11$, and $R^- = 9.09\ \text{k}\Omega$.

Note the missing term because $R^+ = 0$.

- The term (V_{IO} - $R^- I^-$) takes its largest positive value for V_{IO} = +2 mV and I^- = 0 (we cannot reverse the op amp input current so the lowest possible value is zero):

  Thus, from eq. (305):

$$V_{OE} = -(11)(2\text{ mV} - 0) = -22\text{ mV} \quad \textbf{(306)}$$

- The term (V_{IO} - $R^- I^-$) takes its largest negative value for V_{IO} = -2 mV and I^- = 100 nA **+** 40 nA/2 = 120 nA.

  Thus from eq. (305):

$$V_{OE} = -(11)\left[-2\text{ mV} - (9.09\text{ k}\Omega)(120\text{ nA})\right] = +34\text{ mV} \quad \textbf{(307)}$$

- Thus we know V_{OE} will lie between -22 mV and +34 mV.

Without additional knowledge, e.g., measurements on a *particular* chip, we can not determine error with any higher accuracy.

Canceling the Effect of the Bias Currents:

Consider the complete dc error equation (301), repeated below:

$$V_{OE} = -\left(1+\frac{R_F}{R_N}\right)\left(V_{IO} + R^+ I^+ - R^- I^-\right) \tag{308}$$

If we knew the *exact* values of I^+ and I^- we could choose the resistances R^+ and R^- so that these terms canceled. However, we can't know these values in general.

We do however know the value of input bias current, I_B.

Rewriting (308) to show the effect of the bias currents:

$$V_{OE} = -\left(1+\frac{R_F}{R_N}\right)\left[V_{IO} + R^+\left(I_B + \frac{I_{IO}}{2}\right) - R^-\left(I_B - \frac{I_{IO}}{2}\right)\right]$$

$$= -\left(1+\frac{R_F}{R_N}\right)\left[V_{IO} + \left(R^+ - R^-\right)I_B + \left(R^+ + R^-\right)\frac{I_{IO}}{2}\right] \tag{309}$$

Thus, we can eliminate the effect of I_B if we select

$$R^+ = R^- = R_F \| R_N \tag{310}$$

This makes the average error due to currents be zero.

Instrumentation Amplifier

Introduction

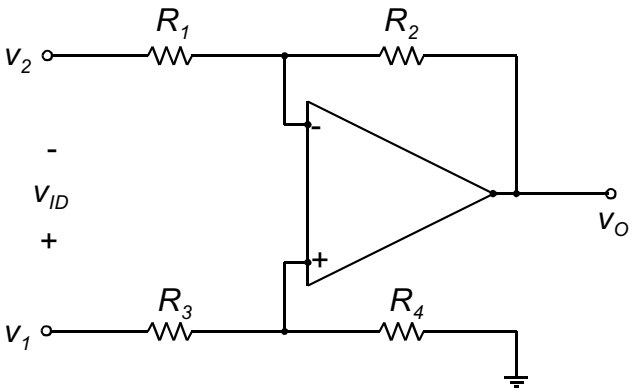

Fig. 286. Difference amplifier.

Recall the basic op amp difference amplifier:

$$v_O = \frac{R_2}{R_1}(v_1 - v_2) \qquad \textbf{(311)}$$

only if: $\frac{R_4}{R_3} = \frac{R_2}{R_1}$

To obtain high *CMRR*, R_4/R_3 and R_2/R_1 must be *very closely matched*. But this is impossible, in general, as we usually don't know the internal resistances of v_1 and v_2 with certainty or predictability.

The solution is an *instrumentation-quality differential amplifier!!!*

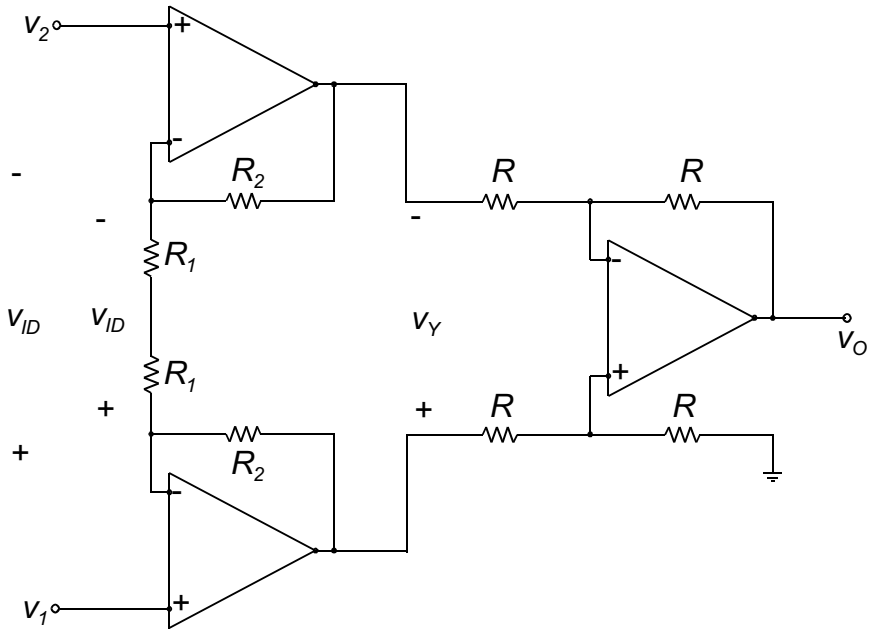

Fig. 287. Instrumentation amplifier.

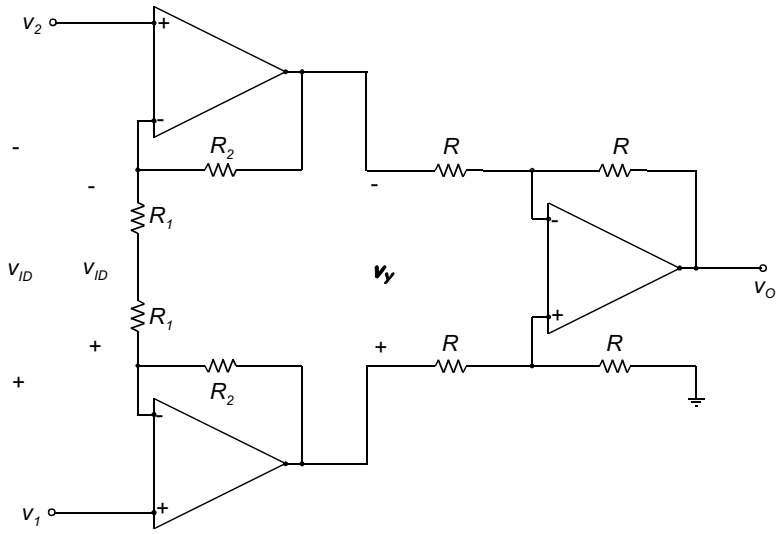

Fig. 288. Instrumentation amplifier (Fig. 287 repeated).

Simplified Analysis

The input op amps present infinite input impedance to the sources, thus the internal resistances of v_1 and v_2 are now negligible.

Because the op amps are ideal v_{ID} appears across the series R_1 resistances. Current through these resistances is:

$$i_{R_1} = \frac{v_{ID}}{2R_1} \tag{312}$$

This current also flows through R_2. The voltage v_Y is the sum of voltages across the R_1 and R_2 resistances, and the 2nd stage is a difference amplifier with unity gain. Thus:

$$v_O = v_Y = \left(1 + \frac{R_2}{R_1}\right)(v_1 - v_2) \tag{313}$$

Instrumentation amplifiers are available in integrated form, both with and without the R_1 resistances built-in.

Noise

We can define "noise" in two different ways:

1. *Any* undesired component in the signal (e.g., radio-frequency interference, crosstalk, etc.)
2. Random inherent mechanisms.

Johnson Noise

This is noise generated across a resistor's terminals due to random thermal motion of electrons.

Johnson noise is *white noise*, meaning it has a flat frequency spectrum - the same noise power in each Hz of bandwidth:

$$p_n = 4kTB \tag{314}$$

where, k = Boltzmann's constant = 1.38 x 10^{-23} J/K,
T = resistor temperature in kelvins
B = measurement bandwidth in Hz.

The open-circuit *rms* noise voltage across a resistor R is:

$$e_r = \sqrt{4kTRB} \tag{315}$$

From eq. (315), at T_{room} = 293 K:

$$\sqrt{4kTR} = 0.127\sqrt{R}\ \frac{\text{nV}}{\sqrt{\text{Hz}}} \tag{316}$$

This means that, if we have a perfect, noiseless BPF with BW = 10 kHz, and V_{in} is the noise voltage of a 10 kΩ resistance at T_{room}, we would measure an output voltage V_{OUT} of 1.27 μV with an ideal (noiseless) true-*rms* voltmeter.

Johnson noise is *random*. The instantaneous amplitude is unpredictable and must be described probabilistically.

It follows a Gaussian distribution with a mean value of zero. This amplitude distribution has a flat spectrum with very "sharp" fluctuations.

Johnson Noise Model:

A voltage source e_r in series with a resistance R.

The significance of Johnson noise is that it sets a lower bound on the noise voltage present in any amplifier, signal source, etc.

Shot Noise

Shot noise arises because electric current flows in discrete charges, which results in statistical fluctuations in the current.

The *rms* fluctuation is a dc current I_{DC} is given by:

$$I_r = \sqrt{2qI_{DC}B} \qquad \textbf{(317)}$$

where, q = electron charge = 1.60×10^{-19} C

B = measurement bandwidth in Hz.

Shot Noise, 10 kHz measurement bandwidth, from eq. (317)		
I_{DC}	I_r	% fluctuation
1 A	57 nA	0.0000057%
1 μA	57 pA	0.0057% (-85 dB)
1 pA	57 fA	5.6%

Eq. (317) assumes that the charge carriers act independently.

This is true for charge carriers crossing a barrier (e.g., a junction diode).

This is false for current in metallic conductor (e.g. a simple resistive circuit). For this latter case, actual noise is less than that given in eq. (317), i.e., the model gives a pessimistic estimate for design purposes.

1/f Noise (Flicker Noise)

This is additional, or excess, noise found in real devices, caused by various sources.

1/*f* noise is *pink noise* - it has a 1/*f* spectrum, which means equal power per *decade* of bandwidth, rather than equal power per Hz.

As an example, let's look at 1/f noise in resistors:

Fluctuations in resistance result in an additional noise voltage which is proportional to the current flowing in the resistance.

The amount of additional noise depends on resistor construction.

The table below lists the excess noise for various resistor types. The entries are given in *rms* voltage, per volt applied across the resistor, and measured over one decade of bandwidth:

Carbon-composition	0.10 μV/V to 3 μV/V
Carbon-film	0.05 μV/V to 0.3 μV/V
Metal-film	0.02 μV/V to 0.2 μV/V
Wire-wound	0.01 μV/V to 0.2 μV/V

Other mechanisms producing 1/f noise:

- Base current noise in transistors.
- Cathode current noise in vacuum tubes.
- Speed of ocean currents.
- Flow of sand in an hourglass.
- Yearly flow of the Nile (measured over past 2000 years).
- Loudness of a piece of classical music vs. time.

Interference

In this case any interfering signal or unwanted “stray” pickup constitutes a form of noise.

The frequency spectrum and amplitude characteristics depend on type of interference:

Sharp spectrum, relatively constant amplitude:

- 60 Hz interference.
- Radio and television stations.

Broad spectrum, probabilistic amplitude:

- Automobile ignition noise.
- Lightning.
- Motors, switches, switching regulators, etc.

Some circuits, detectors, cables, etc., are *microphonic*:

- Noise voltage or current is generated as a result of vibration.

Amplifier Noise Performance

Terms, Definitions, Conventions

Any noisy amplifier can be completely specified for noise in terms of two noise generators, e_n and i_n:

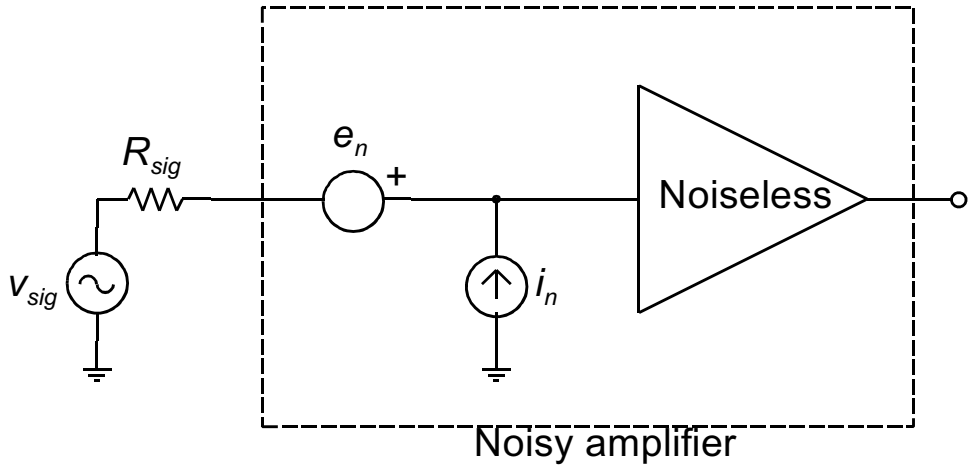

Fig. 289. Noise model of an amplifier.

Amplifier Noise Voltage:

Amplifier noise voltage is more properly called the *equivalent short-circuit input rms noise voltage*.

e_n is the noise voltage that *appears* to be present at an amplifier input if the input terminals are shorted. It is equivalent to a noisy offset voltage, and is expressed in $\text{nV}/\sqrt{\text{Hz}}$ at a specific frequency.

It is measured by:

- shorting the amplifier input,
- measuring the *rms* noise output,
- dividing by amplifier gain (and further dividing by $\sqrt{B}$).

e_n increases at lower frequencies, so it appears as 1/f noise.

Amplifier Noise Current:

Amplifier noise current is more properly called the *equivalent open-circuit input rms noise current*.

i_n is the apparent noise current at an amplifier input. It is equivalent to a noisy bias current, and is expressed in pA / $\sqrt{\text{Hz}}$ at a specific frequency.

It is measured by:

- shunting the amplifier input with a resistor,
- measuring the *rms* noise output,
- dividing by amplifier gain (and further dividing by $\sqrt{B}$),
- "subtracting" noise due to e_n and the resistor (we discuss adding and subtracting noise voltages later).

i_n increases at lower frequencies for op amps and BJTs - it increases at higher frequencies for FETs.

Signal-to-Noise Ratio:

Expressed in decibels, the default definition is a ratio of signal power to noise power (delivered to the same resistance, and measured with the same bandwidth and center frequency):

$$SNR = 10\log\left(\frac{P_{sig}}{P_n}\right) \quad \text{dB} \tag{318}$$

It can also be expressed as the ratio of *rms* voltages:

$$SNR = 20\log\left(\frac{v_{sig}}{e_n}\right) \quad \text{dB} \tag{319}$$

Noise Figure:

This is a figure of merit for comparing amplifiers. It indicates how much noise an amplifier adds.

Defined simply:

$$NF = 10\log\left[\frac{\left(P_{sig} / P_n\right)_{input}}{\left(P_{sig} / P_n\right)_{output}}\right] \quad \text{dB} \tag{320}$$

It can be written even more simply:

$$NF = SNR_{input} - SNR_{output} \tag{321}$$

Note that *NF* will always be greater than 0 dB for a real amplifier.

Noise Temperature:

An alternative figure of merit to noise figure, it gives the same information about an amplifier. The definition is illustrated below:

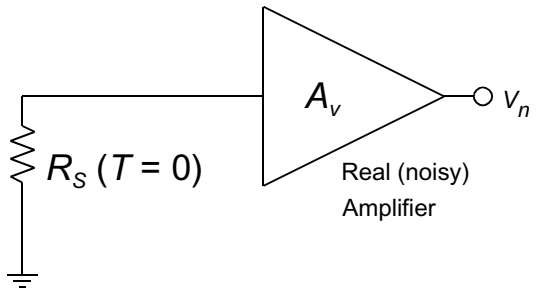

Fig. 290. Noisy amplifier with ideal input.

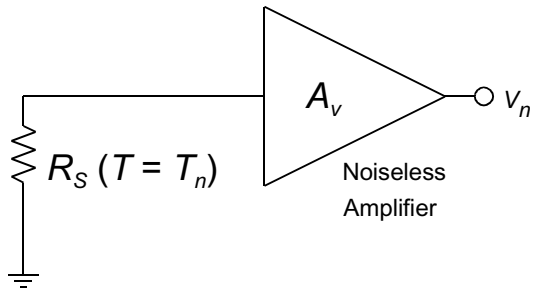

Fig. 291. Ideal amplifier with noisy input.

A real amplifier (Fig. 290) that produces v_n at its output with a noiseless input, has the noise temperature T_n.

An ideal, noiseless amplifier (Fig. 291) with a source resistance at $T = T_n$ produces the same noise voltage at its output.

Converting NF to/from T_n:

$$T_n = T\left(10^{NF/10} - 1\right) \quad \Leftrightarrow \quad NF = 10\log\left(\frac{T_n}{T} + 1\right) \tag{322}$$

where, *NF* is expressed in dB

T is the ambient (room) temperature, usually 290 K

For good, low-noise amplifier performance:

NF << 3 dB and/or T_n << 290 K

Adding and Subtracting Uncorrelated Quantities

This applies to operations such as *noise* ± *noise*, or *noise* ± *signal*.

Because noise is probabilistic, we don't know instantaneous amplitudes. As a result we can only add and subtract powers.

This means *squared* amplitudes add (*rms* amplitudes do not), e.g.:

$$v_{total}^{\ 2} = v_{sig}^{\ 2} + e_n^{\ 2} \tag{323}$$

Amplifier Noise Calculations

Introduction

Repeating our amplifier noise model:

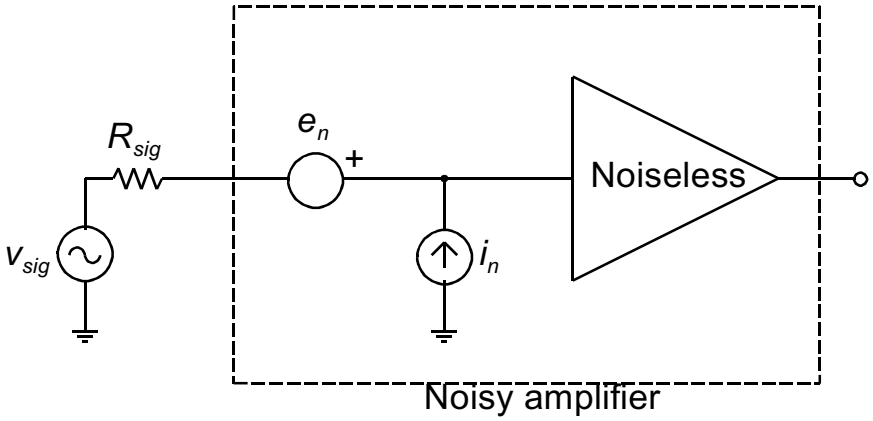

Fig. 292. Noise model of an amplifier (Fig. 289 repeated).

We presume the input resistance of the noiseless amplifier is much larger than R_{sig}, and describe the following amplifier noise sources:

e_r, the Johnson noise of R_{sig},

e_n,the amplifier noise source (amplifier noise referred to the input),

$i_n R_{sig}$, the noise voltage resulting from i_n flowing through R_{sig}

The total input noise is (assuming they are uncorrelated):

$$e_t^2 = e_r^2 + e_n^2 + i_n^2 R_{sig}^2 \quad \textbf{(324)}$$

For convenience, we define the last two terms of eq. (324) as the *equivalent amplifier input noise*, i.e., the amplifier noise contribution with a noise-free R_{sig}:

$$e_{eq}^2 = e_n^2 + i_n^2 R_{sig}^2 \quad \textbf{(325)}$$

Calculating Noise Figure

The noise figure of this amplifier may now be calculated. We use the definition of *NF* as the ratio of powers, and let G_p represent the amplifier *power gain*:

$$NF = 10\log\left[\frac{\left(P_{sig}\,/\,P_n\right)_{input}}{\left(P_{sig}\,/\,P_n\right)_{output}}\right] = 10\log\left(\frac{P_{sig\ input}\times P_{n\ output}}{P_{n\ input}\times P_{sig\ output}}\right)$$

$$= 10\log\left[\frac{P_{sig\ input}\left(G_p e_t^{\,2}\right)}{e_r^{\,2}\left(P_{sig\ input}G_p\right)}\right] = 10\log\left(\frac{e_t^{\,2}}{e_r^{\,2}}\right) = 10\log\left(\frac{e_r^{\,2}+e_n^{\,2}+i_n^{\,2}R_{sig}^{\,2}}{e_r^{\,2}}\right) \quad \textbf{(326)}$$

$$= 10\log\left(1+\frac{e_n^{\,2}+i_n^{\,2}R_{sig}^{\,2}}{e_r^{\,2}}\right) = 10\log\left(1+\frac{e_{eq}^{\,2}}{e_r^{\,2}}\right)$$

Observe that for small R_{sig}, amplifier noise voltage dominates, while for large R_{sig}, the amplifier noise current dominates.

FET amplifiers have nearly zero noise current, so they have a clear advantage *!!!*

Remember, *NF* data must include values of R_{sig} and frequency to have significance.

Typical Manufacturer's Noise Data

Introduction

Manufacturers present noise data in various ways. Here is some typical data for Motorola's 2N5210 *npn* BJT:

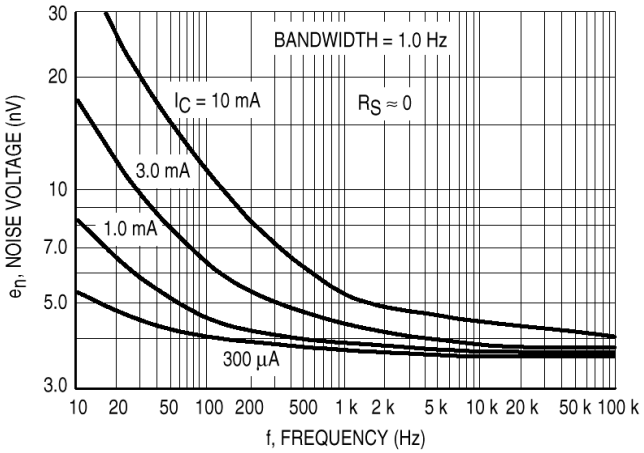

Fig. 293. 2N5210 noise voltage vs. frequency, for various quiescent collector currents.

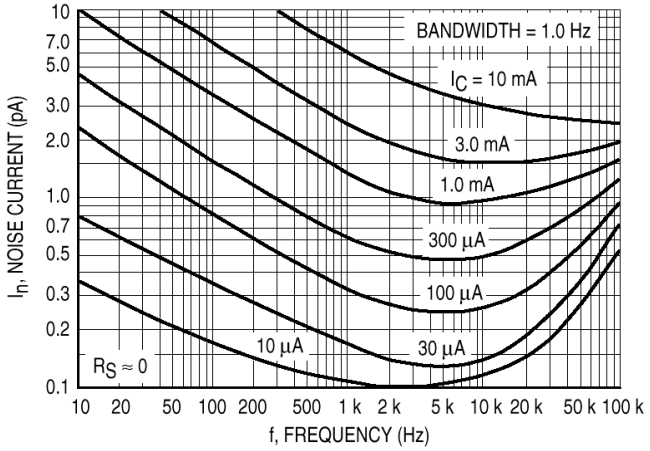

Fig. 294. 2N5210 noise current vs. frequency, for variousquiescent collector currents.

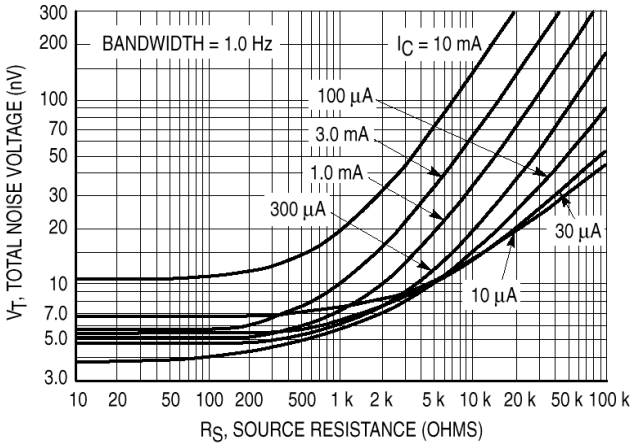

Fig. 295. 2N5210 total noise voltage at 100 Hz vs. source resistance, for various quiescent collector currents

The e_n , i_n data of Figs. 293 and 294 can be used to construct Fig. 295, a plot of *total* noise voltage, e_t, for various values of R_{sig}. We simply follow eq. (324), repeated here:

$$e_t^2 = e_r^2 + e_n^2 + i_n^2 R_{sig}^2 \qquad \textbf{(327)}$$

Example #1

Calculate the total equivalent input noise per unit bandwidth, for a 2N5210 operating at 100 Hz with a source resistance of 1 kΩ, and a collector bias current of 1 mA:

1. $e_r \approx 4.02 \text{ nV} / \sqrt{\text{Hz}}$ from eq. (316).

2. $e_n \approx 4.5 \text{ nV} / \sqrt{\text{Hz}}$ (f = 100 Hz, I_C = 1 mA) from Fig. 293.

3. $i_n \approx 3.5 \text{ pA} / \sqrt{\text{Hz}}$ (f = 100 Hz, I_C = 1 mA) from Fig. 294.

Evaluating eq. (327) - remembering to square the terms on the right-hand side, and take the square root of the resulting sum - gives :

$$e_t = 6.97 \text{ nV} / \sqrt{\text{Hz}} \qquad \textbf{(328)}$$

This compares favorably (within graphical error) with a value slightly greater than $7 \text{ nV} / \sqrt{\text{Hz}}$ obtained from Fig. 295.

Of course, it would take *many* calculations of this type to produce the curves of Fig. 295.

Example #2

Determine the narrow bandwidth noise figure for the amplifier of example #1 (f = 100 Hz, I_{CQ} = 1 mA, R_{sig} = 1 kΩ).

1. From eq. (326), repeated here

$$NF = 10\log\left(1+\frac{e_n^{\,2}+i_n^{\,2}R_{sig}^{\,2}}{e_r^{\,2}}\right) \qquad \textbf{(329)}$$

with the values of e_n, i_n, and e_r from example #1, we calculate:

$$NF = 10\log\left(1+\frac{(5.70)^2}{(4.02)^2}\right) = 10\log(3.01) = 4.79\ \text{dB} \qquad \textbf{(330)}$$

which compares favorably to the value of approx. 5 dB obtained from the manufacturer's data shown below:

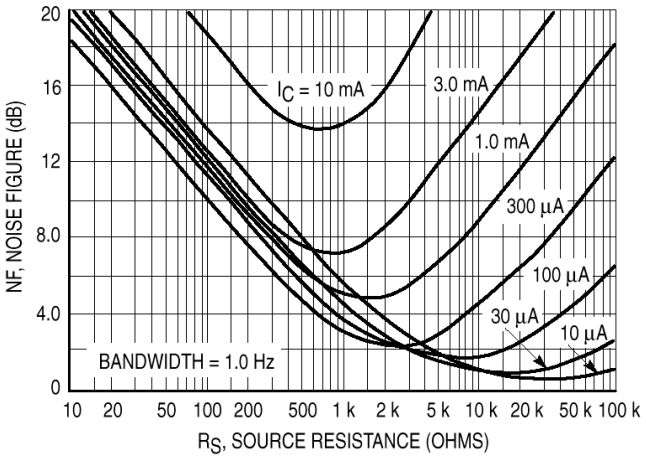

Fig. 296. 2N5210 100-Hz noise figure vs. source resistance, at various quiescent collector currents.

Noise - References and Credits

References for this section on noise are:

1. *Noise Specs Confusing?*, Application Note 104, National Semiconductor Corp., May 1974.

This is an *excellent* introduction to noise. I highly recommend that you get a copy. It is available on National's website at http://www.national.com

2. *The Art of Electronics,* 2nd ed., Paul Horowitz and Winfield Hill, Cambridge University Press, New York, 1989.

This text has a good treatment of noise, and makes a good general electronics reference. Check it out at http://www.artofelectronics.com

3. The 2N5210 data sheets, of which Figs. 293 - 296 are a part, are available from Motorola, Inc., at http://www.motorola.com

Introduction to Logic Gates

The Inverter

We will limit our exploration to the logic *inverter*, the simplest of logic gates. A logic inverter is essentially just an inverting amplifier, operated at its saturation levels:

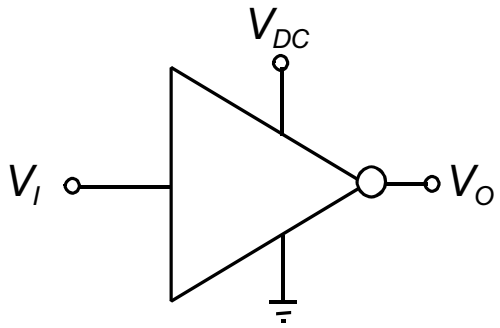

Fig. 297. Logic inverter. DC supply connections are not normally shown.

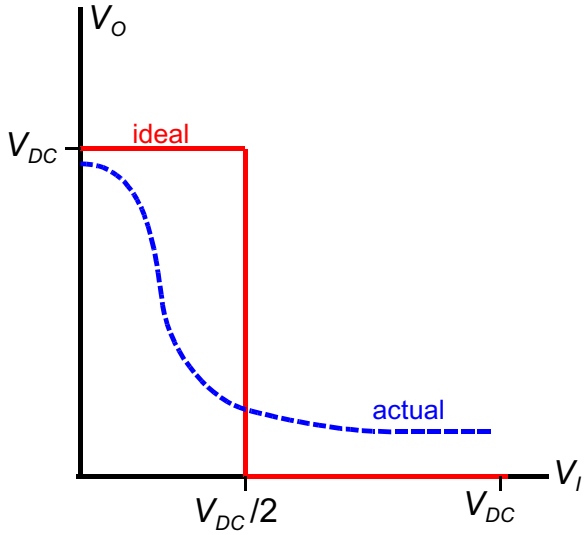

Fig. 298. Ideal and actual inverter transfer functions.

The Ideal Case

V_I is either V_{DC} (logic 1) or zero (logic 0).

V_O is either zero (logic 0) or V_{DC} (logic 1).

The Actual Case

We don't know the exact transfer function of any individual logic inverter.

Manufacturer's specifications give us a clue about the "range" of permitted input and output levels.

Manufacturer's Voltage Specifications

- V_{IH} = *lowest* V_I guaranteed to be "seen" as "high" (logic 1).
- V_{IL} = *highest* V_I guaranteed to be "seen" as "low" (logic 0).

And with V_I meeting the above specifications:

- V_{OH} = *lowest* "high" (logic 1) output voltage.
- V_{OL} = *highest* "low" (logic 0) output voltage.

Noise Margin

Noise margin is the maximum noise amplitude that can be added to the input voltage, *without causing an error in the output logic level.* It is the smaller of:

$$NM_H = V_{OH} - V_{IH} \quad \text{and} \quad NM_L = V_{IL} - V_{OL} \tag{331}$$

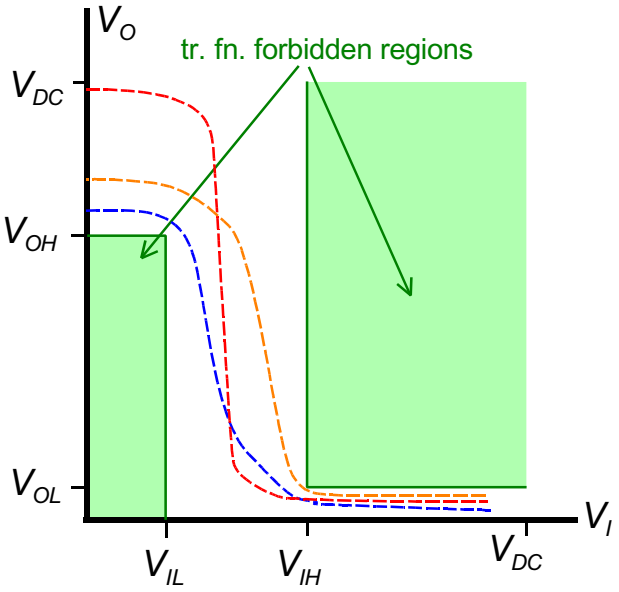

Fig. 300. Mfr's voltage specs illustrated with example transfer functions.

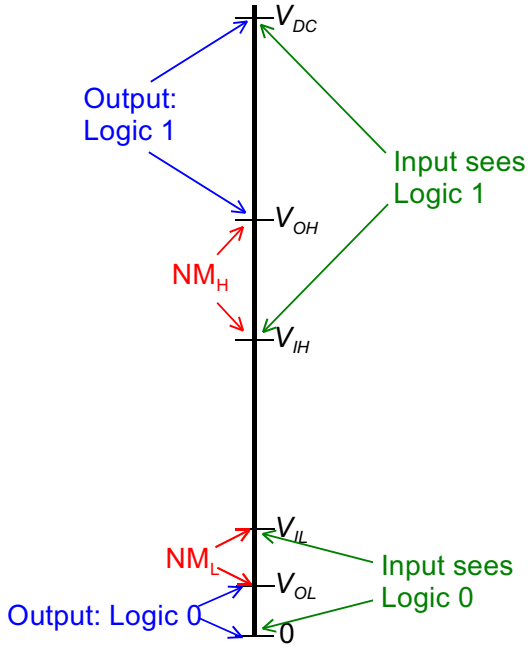

Fig. 299. Mfr's voltage specs illustrated on a number line.

Manufacturer's Current Specifications

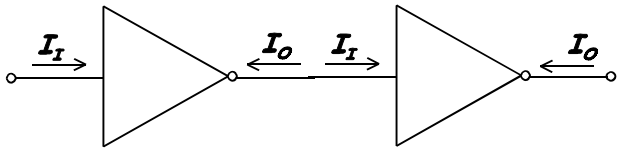

Fig. 301. Reference directions for mfr's current specifications.

Note that the reference direction for both input and output currents is *into the chip*.

- I_{OH} = *highest* current that output can source with $V_O \geq V_{OH}$.
- I_{OL} = *highest* current that output can sink with $V_O \leq V_{OL}$.
- I_{IH} = *highest* possible input current with $V_I \geq V_{IH}$.
- I_{IL} = *highest* possible input current with $V_I \leq V_{IL}$.

Fan-Out

Fan-out is defined as the maximum number of gates that can be driven without violating the voltage specifications. It must be an integer, of course; it is the smaller of:

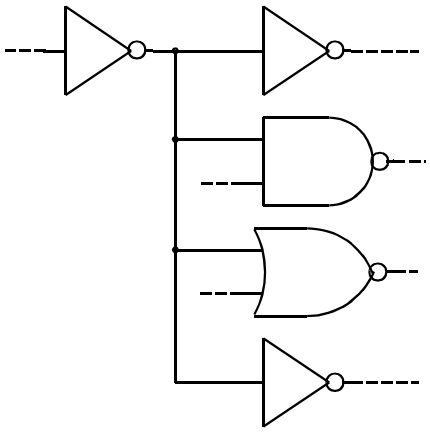

Fig. 302. Fan-out illustrated.

$$FO_H = \text{int}\left(\left|\frac{I_{OH}}{I_{IH}}\right|\right) \quad \textbf{(332)}$$

and

$$FO_L = \text{int}\left(\left|\frac{I_{OL}}{I_{IL}}\right|\right) \quad \textbf{(333)}$$

Power Consumption

Static Power Consumption:

The *static* power is the power required to run the chip when the output isn't changing.

It may be different when the output is high may be different than when the output is low. Thus, we normally assume that it is merely the average of the two.

Dynamic Power Consumption:

Because load capacitance is always present, additional power is required when the output is changing states.

To understand this, consider the following logic gate model, and presume the switch begins in the low position.

When the switch goes high, C_{LOAD} charges from V_{OL} (≈ 0) to V_{OH} ($\approx V_{DC}$).

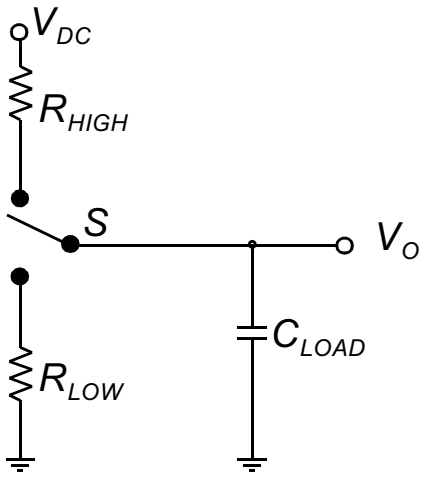

Fig. 303. Simple model of logic gate output.

At the end of this charging cycle, the charge stored in C_{LOAD} is:

$$Q = C_{LOAD} V_{DC} \qquad \textbf{(334)}$$

And the *energy* required of V_{DC} to deliver this charge is:

$$E = Q V_{DC} = C_{LOAD} V_{DC}^{\,2} \qquad \textbf{(335)}$$

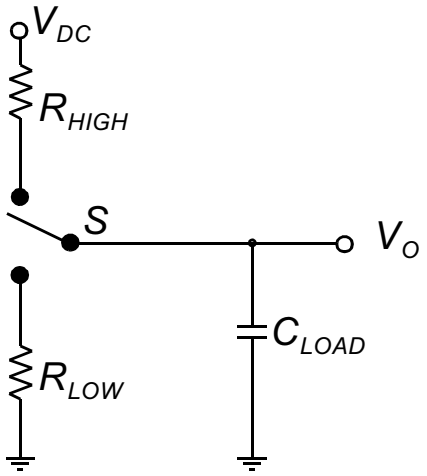

Fig. 304. Logic gate model (Fig. 303 repeated).

Of the energy required of V_{DC} , half is stored in the capacitor:

$$E_C = \frac{1}{2} C_{LOAD} V_{DC}^{\ 2} \qquad \textbf{(336)}$$

The remaining half of the energy required of V_{DC} has been dissipated as heat in R_{HIGH}.

Now the switch changes state, i.e., goes low. C_{LOAD} discharges toward V_{OL} (≈ 0), and the energy stored in C_{LOAD} is dissipated in R_{LOW}.

Finally, suppose V_O is continually changing states, with a frequency f (i.e., with period T). The energy dissipated in the gate *per* period is:

$$\frac{C_{LOAD} V_{DC}^{\ 2}}{T} = C_{LOAD} V_{DC}^{\ 2} f \qquad \textbf{(337)}$$

But energy per unit time is power, i.e., the *dynamic power dissipation*:

$$P_{dynamic} = C_{LOAD} V_{DC}^{\ 2} f \qquad \textbf{(338)}$$

Rise Time, Fall Time, and Propagation Delay

We use the following definitions to describe logic waveforms:

t_r, *rise time* - time interval for a waveform to rise from 10% to 90% of its total change

t_f, *fall time* - time interval for a waveform to fall from 90% to 10% of its total change

t_{PHL} and t_{PLH}, *propagation delay* - time interval from the 50% level of the input waveform to 50% level of the output

t_{PD}, *average propagation delay* - simply, the average of t_{PHL} and t_{PLH}

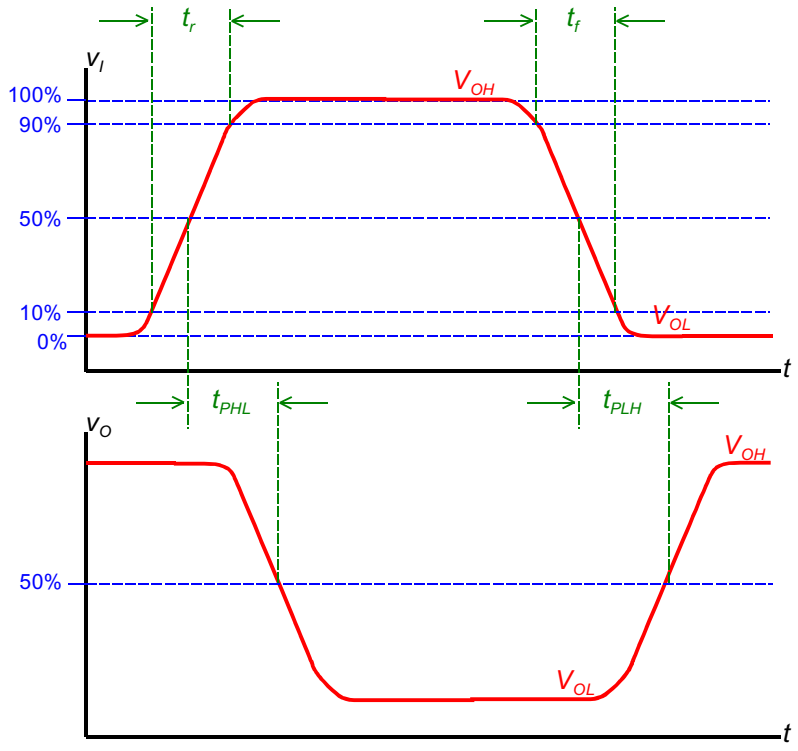

Fig. 305. Generic examples of rise time, fall time, and propagation delay.

Speed-Power Product

The *speed-power product* provides a “figure of merit” of a logic family.

It is defined as the *product* of *propagation delay* (speed) and *static power dissipation* (power) per gate

Note this product has units of energy.

Currently, the speed-power product of logic families range from approximately from 5 pJ to 50 pJ

TTL Logic Families & Characteristics

hex inverter ⟹		7404	74S04	74LS04	74AS04	74ALS04	74F04
parameter	unit	standard	S Schottky	LS low-power S	AS advanced S	ALS advanced LS	F FAST
t_{PD}	ns	10	3	10	2	4	3
P_{static}	mW	10	19	2	7	1	4
I_{OH}	µA	-400	-1000	-400	-2000	-400	-1000
I_{OL}	mA	16	20	8	20	8	20
I_{IH}	µA	40	50	20	20	20	20
I_{IL}	mA	-1.6	-2.0	-0.4	-0.5	-0.1	-0.6
V_{OH}	V	2.4	2.7	2.7	3.0	3.0	2.7
V_{OL}	V	0.4	0.5	0.5	0.5	0.5	0.5
V_{IH}	V	2.0 V for all TTL families					
V_{IL}	V	0.8 V for all TTL families					

. . . table compiled by Prof. D.B. Brumm

CMOS Logic Families & Characteristics

These are typical examples of the guaranteed values for V_{DC} = 5 V, and are specifications for driving auxiliary loads, not other gates alone..

Output current ratings depend upon the specific gate type, esp. in the 4000 series.

Ratings for I_{OH} and I_{OL} are given for the specific V_{OH} and V_{OL} .

parameter	unit	4000	74C	74HC	74HCT	AC	ACT
t_{PD}	ns	80	90	9	10	5	5
P_{static}	< 1 μW for all versions						
I_{OH}	mA	-1.0	-0.36	-4.0	-4.0	-24	-24
I_{OL}	mA	2.4	0.36	4.0	4.0	24	24
I_{IH}	μA	1.0	1.0	1.0	1.0	1.0	1.0
I_{IL}	mA	-1.0	-1.0	-1.0	-1.0	-1.0	-1.0
V_{OH}	V	2.5	2.4	3.5	3.5	3.7	3.7
V_{OL}	V	0.4	0.4	0.4	0.4	0.4	0.4
V_{IH}	V	3.5	3.5	3.5	2.0	3.5	2.0
V_{IL}	V	1.5	1.5	1.0	0.8	1.5	0.8
V_{DC}	V	3 - 15	3 - 15	2 - 6	5±0.5	2 - 6	5±0.5

. . . table compiled by Prof. D.B. Brumm

MOSFET Logic Inverters

NMOS Inverter with Resistive Pull-Up

As Fig. 306 shows, this is the most basic of inverter circuits.

Circuit Operation:

The term NMOS implies an *n*-channel enhancement MOSFET. Using a graphical analysis technique, we can plot the load line on the output characteristics, shown below.

When the FET is operating in its triode region, it *pulls* the output voltage low, i.e., toward zero. When the FET is in cutoff, the drain resistance *pulls* the output voltage *up*, i.e., toward V_{CC}, which is why it is called a *pull-up resistor*.

Because $V_{GS} = V_I$ and $V_{DS} = V_O$, we can use Fig. 307 to plot the transfer function of this inverter.

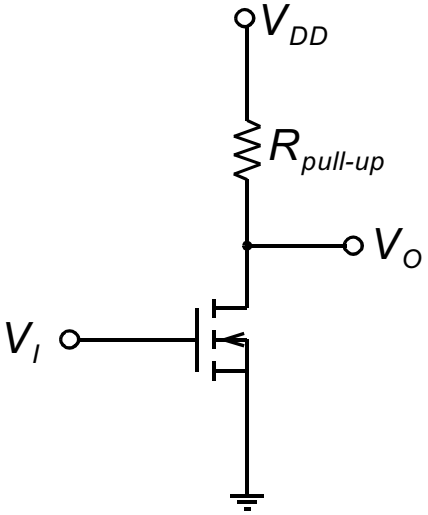

Fig. 306. NMOS inverter with resistive pull-up for the load.

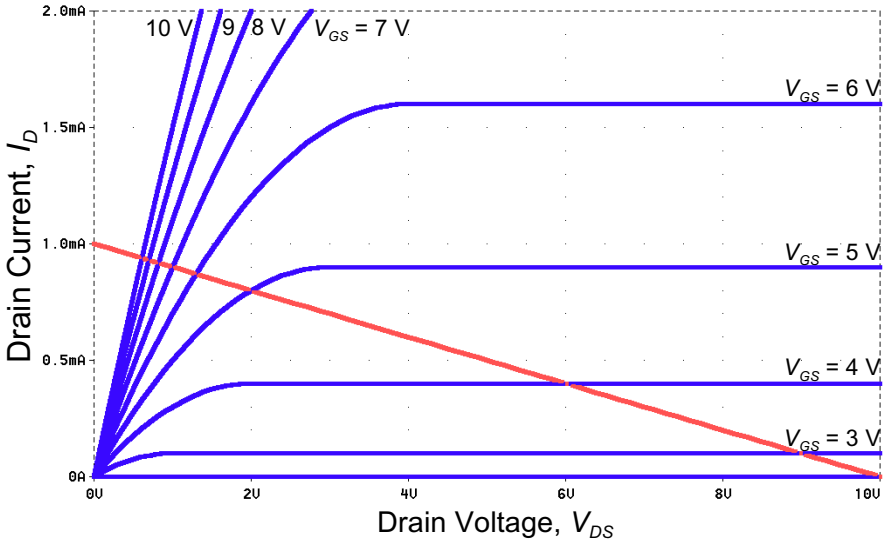

Fig. 307. Ideal FET output characteristics, and load line for V_{DD} = 10 V and $R_{pull\text{-}up}$ = 10 kΩ.

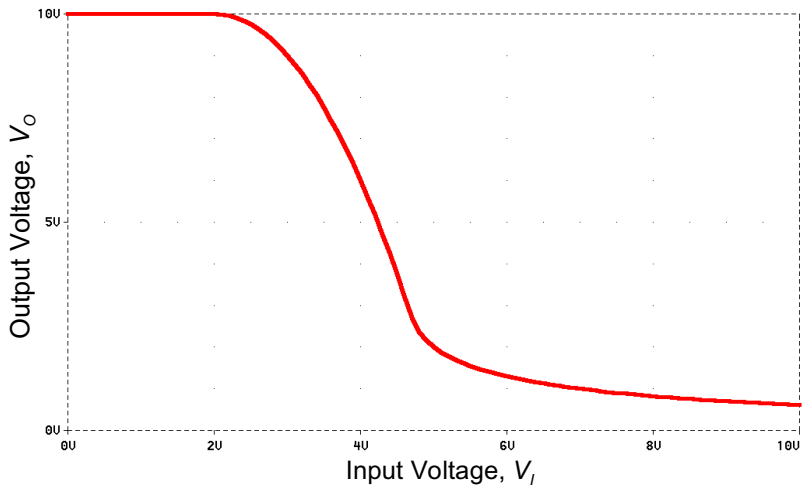

Fig. 308. Inverter transfer function.

Drawbacks:

1. A large R results in reduced V_O for anything but the largest loads, and slows output changes for capacitive loads.

2. A small R results in excessive current, and power dissipation, when the output is low.

The solution to both of these problems is to replace the pull-up resistor with an *active pull-up*.

CMOS Inverter

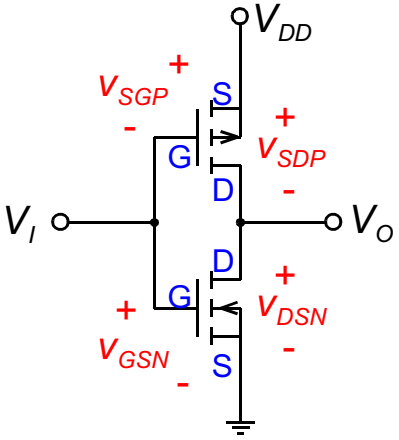

Fig. 309. CMOS inverter.

Circuit Operation:

The CMOS inverter uses an *active pull-up*, a PMOS FET in place of the resistor.

The PMOS and NMOS devices are *complementary* MOSFETs, which gives rise to the name *CMOS*.

In the previous example, the resistor places a *load line* on the NMOS output characteristic.

Here, the PMOS FET places a *load curve* on the output characteristic. *The load curve changes as V_I changes !!!*

The NMOS output curves are the usual fare, and are shown in the figure below:

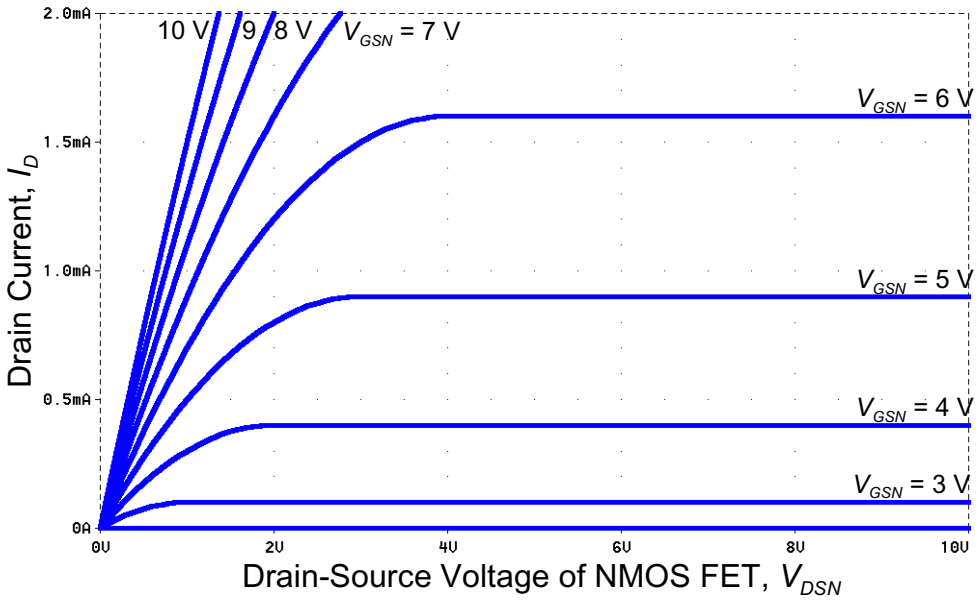

Fig. 310. Ideal NMOS output characteristics.

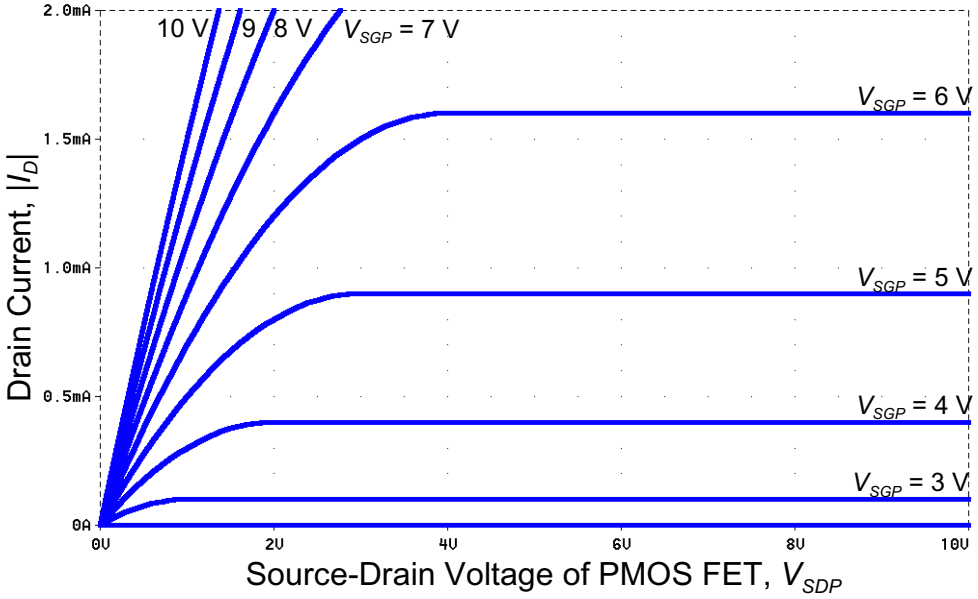

Fig. 311. Ideal PMOS output characteristics.

The PMOS output curves, above, are typical also, but on the input side of the PMOS FET:

$$v_{SGP} = V_{DD} - v_{GSN} \tag{339}$$

This means we can re-label the PMOS curves in terms of v_{GSN}.

And, on the output side of the PMOS FET:

$$v_{SDP} = V_{DD} - v_{DSN} \tag{340}$$

This means we can “rotate and shift” the curves to display them in terms of v_{DSN}. This is done on the following page.

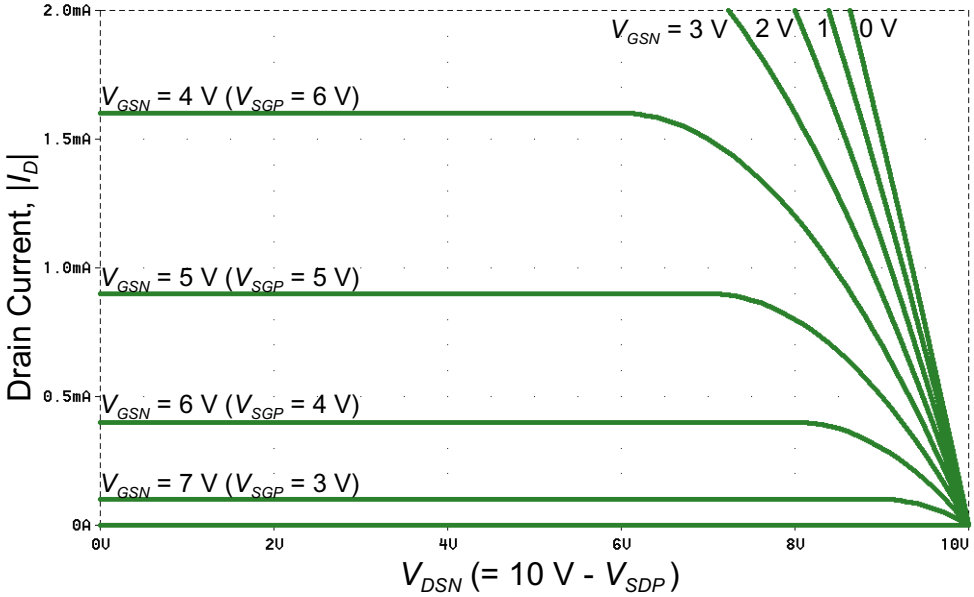

Fig. 312. PMOS "load curves" for V_{DD} = 10 V.

The curves above are the same PMOS output characteristics of Fig. 233, but they've been:

1. Re-labeled in terms of v_{GSN}.

2. Rotated about the origin and shifted to the right by 10 V (i.e., displayed on the v_{DSN} axis).

We can now proceed with a graphical analysis to develop the transfer characteristic. We do so in the following manner:

1. We plot the NMOS output characteristics of Fig. 310, and the PMOS load curves of Fig. 312, on the same set of axes.
2. We choose the single correct output characteristic and the single correct load curve for each of several values of v_I.
3. We determine the output voltage from the intersection of the output characteristic and the load curve, for each value of v_I chosen in the previous step.
4. We plot the v_O *vs.* v_I transfer function using the output voltages determined in step 3.

The figure below shows the NMOS output characteristics and the PMOS load curves plotted on the same set of axes:

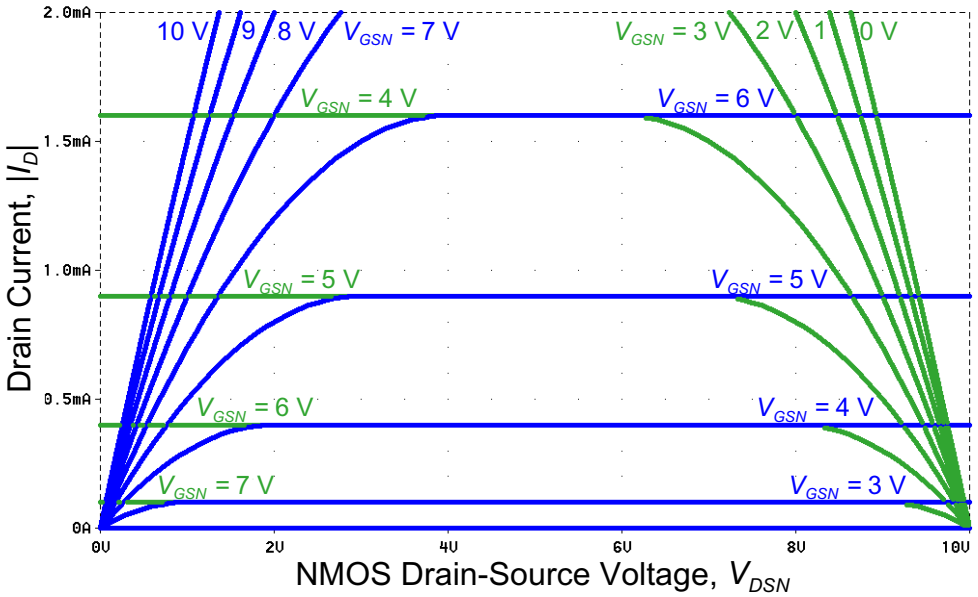

Fig. 313. NMOS output characteristics (in blue) and PMOS load curves (in green) plotted on same set of axes.

Note from Fig. 313 That for $V_I = V_{GSN} \leq 2$ V the NMOS FET (blue curves) is in cutoff, so the intersection of the appropriate NMOS and PMOS curves is at $V_O = V_{DSN} = 10$ V.

As V_I increases above 2 V, we select the appropriate NMOS and PMOS curve, as shown in the figures below.

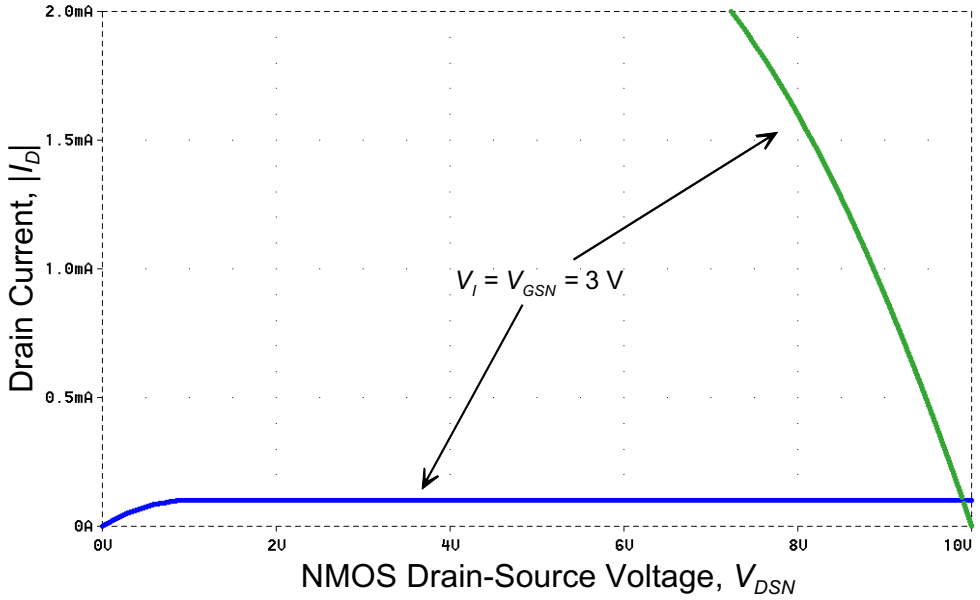

Fig. 314. Appropriate NMOS and PMOS curves for $v_I = 3$ V.

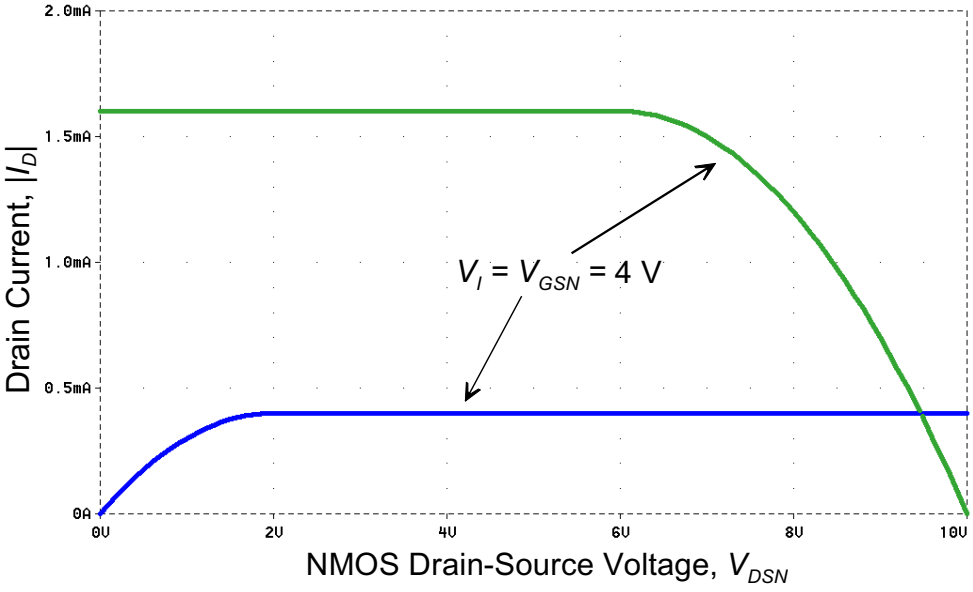

Fig. 315. Appropriate NMOS and PMOS curves for $v_I = 4$ V.

Because the ideal characteristics shown in these figures are horizontal, the intersection of the two curves for $V_I = V_{GSN} = 5$ V appears ambiguous, as can be seen below.

However, *real* MOSFETs have finite drain resistance, thus the curves will have an upward slope. Because the NMOS and PMOS devices are complementary, their curves are symmetrical, and the true intersection is precisely in the middle:

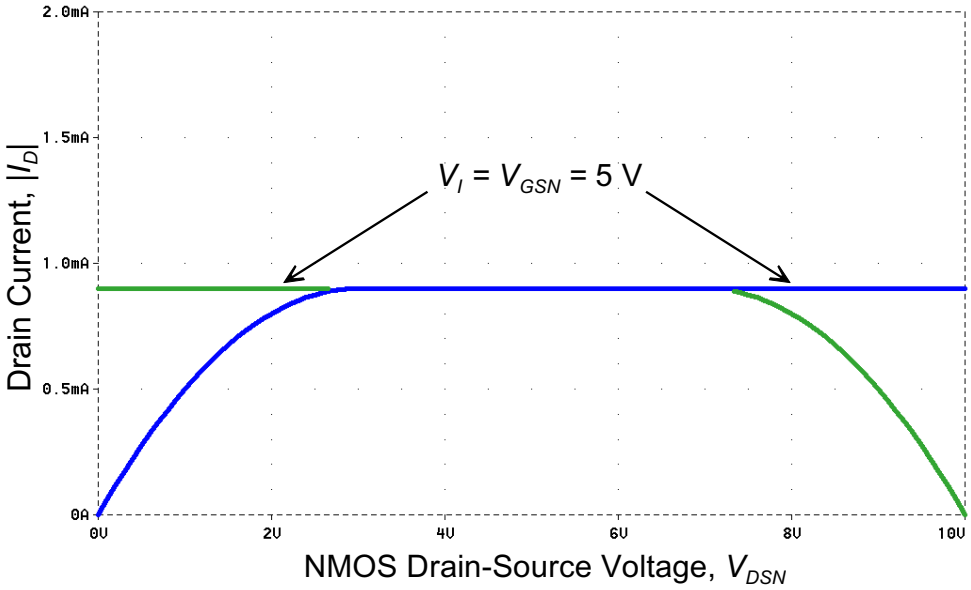

Fig. 316. Appropriate NMOS and PMOS curves for $v_I = 5$ V.

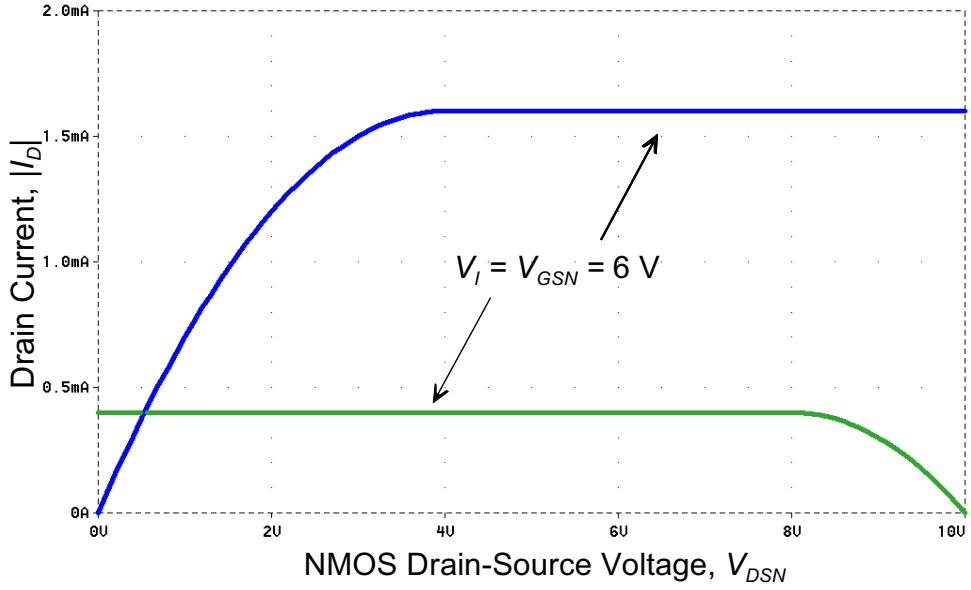

Fig. 317. Appropriate NMOS and PMOS curves for $v_I = 6$ V.

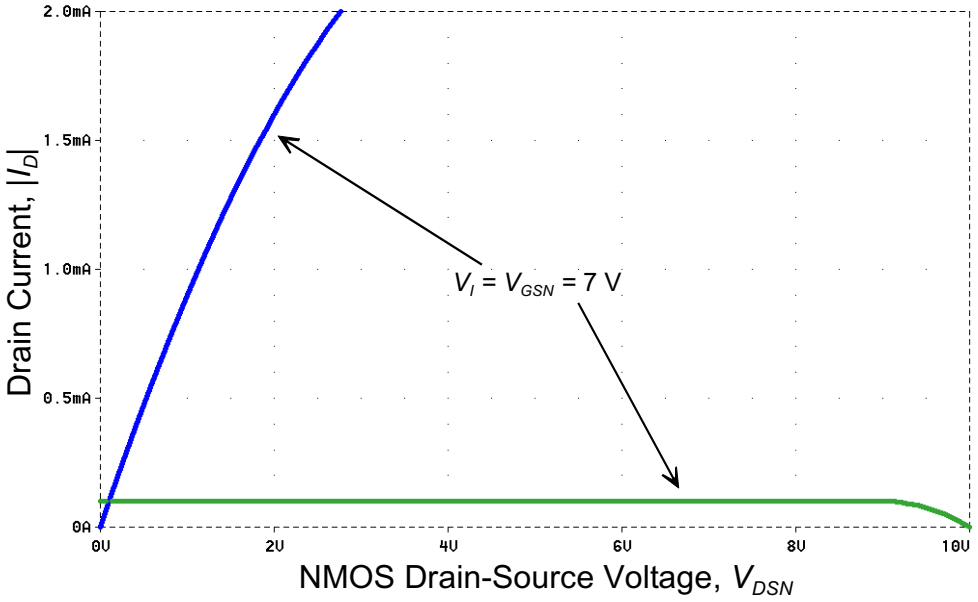

Fig. 318. Appropriate NMOS and PMOS curves for $v_I = 7$ V.

For $V_I = V_{GSN} \geq 8$ V, the PMOS FET (green curves) is in cutoff, so the intersection is at $V_O = V_{DSN} = 0$ V.

Collecting "all" the intersection points from Figs. 314-318 (and the ones for other values of v_I that aren't shown here) allows us to plot the *CMOS inverter transfer function*:

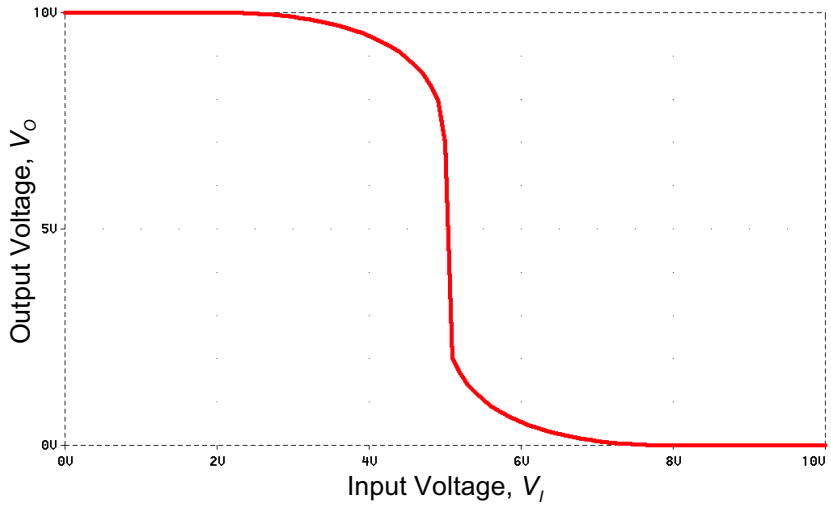

Fig. 319. CMOS inverter transfer function. Note the similarity to the ideal transfer function of Fig. 298.

Differential Amplifier

We first need to remind ourselves of a fundamental way of representing any two signal sources by their differential and common-mode components. This material is repeated from pp. 27-28:

Modeling Differential and Common-Mode Signals

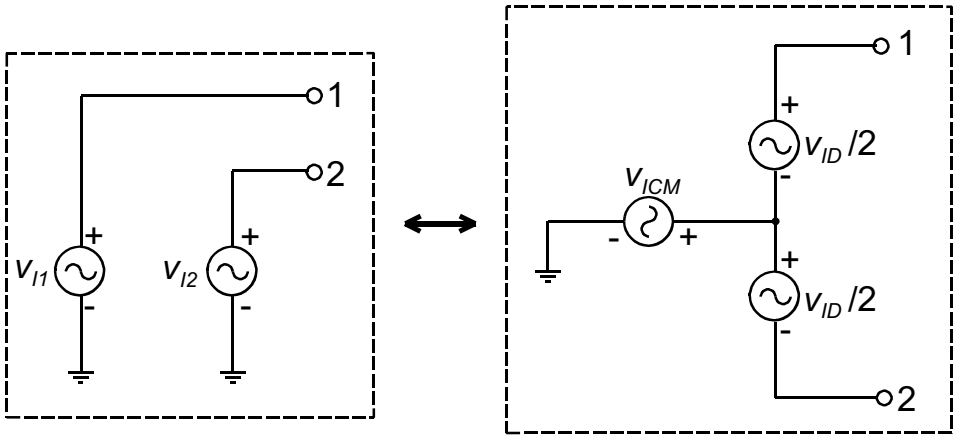

Fig. 320. Representing two sources by their *differential* and *common-mode* components (Fig. 41 repeated).

As shown above, *any* two signals can be modeled by a *differential* component, v_{ID}, and a *common-mode* component, v_{ICM}, *if:*

$$v_{I1} = v_{ICM} + \frac{v_{ID}}{2} \qquad \text{and} \qquad v_{I2} = v_{ICM} - \frac{v_{ID}}{2} \tag{341}$$

Solving these simultaneous equations for v_{ID} and v_{ICM}:

$$v_{ID} = v_{I1} - v_{I2} \qquad \text{and} \qquad v_{ICM} = \frac{v_{I1} + v_{I2}}{2} \tag{342}$$

Note that the *differential* voltage v_{ID} is the *difference* between the signals v_{I1} and v_{I2}, while the *common-mode* voltage v_{ICM} is the *average* of the two (a measure of how they are similar).

Basic Differential Amplifier Circuit

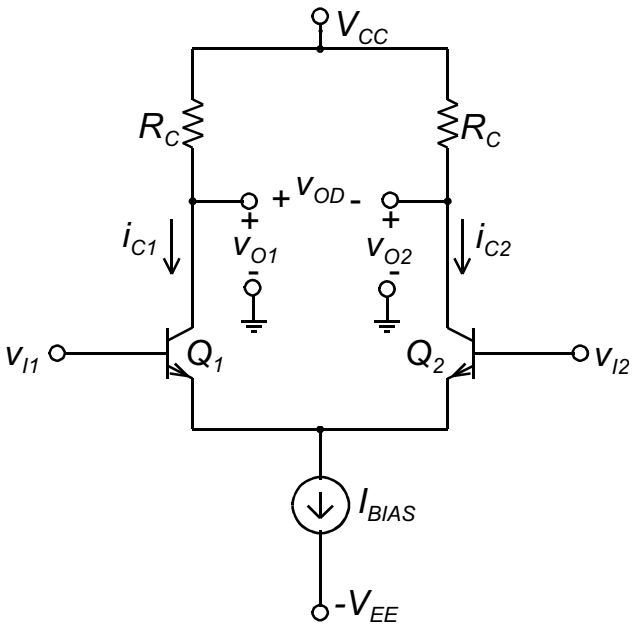

Fig. 321. Differential amplifier.

The basic *diff amp* circuit consists of two *emitter-coupled* transistors.

We can describe the total instantaneous output voltages:

$$v_{O1} = V_{CC} - R_C i_{C1}$$
$$v_{O2} = V_{CC} - R_C i_{C2} \quad \textbf{(343)}$$

And the total instantaneous differential output voltage:

$$v_{OD} = v_{O1} - v_{O2}$$
$$= R_C (i_{C2} - i_{C1}) \quad \textbf{(344)}$$

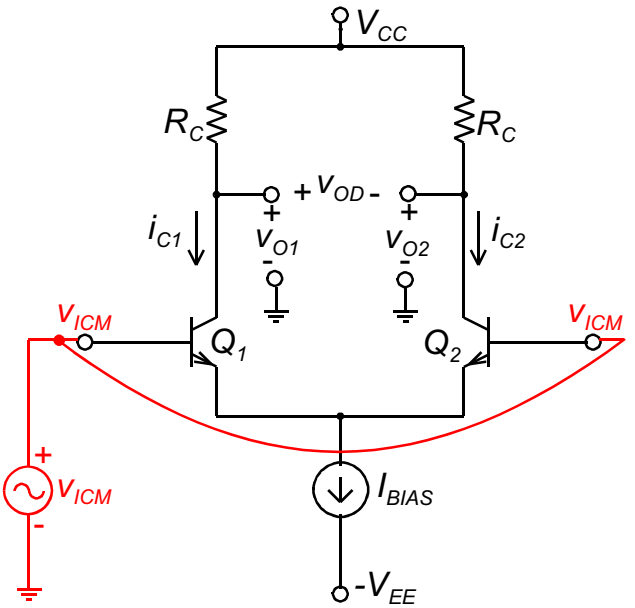

Fig. 322. Differential amplifier with only a common-mode input.

Case #1 - Common-Mode Input:

We let $v_{I1} = v_{I2} = v_{ICM}$, i.e., $v_{ID} = 0$.

From circuit symmetry, we can write:

$$i_{E1} = i_{E2} = \frac{I_{BIAS}}{2} \quad \textbf{(345)}$$

$$i_{C1} = i_{C2} = \frac{\alpha I_{BIAS}}{2} \quad \textbf{(346)}$$

and

$$v_{OD} = 0 \quad \textbf{(347)}$$

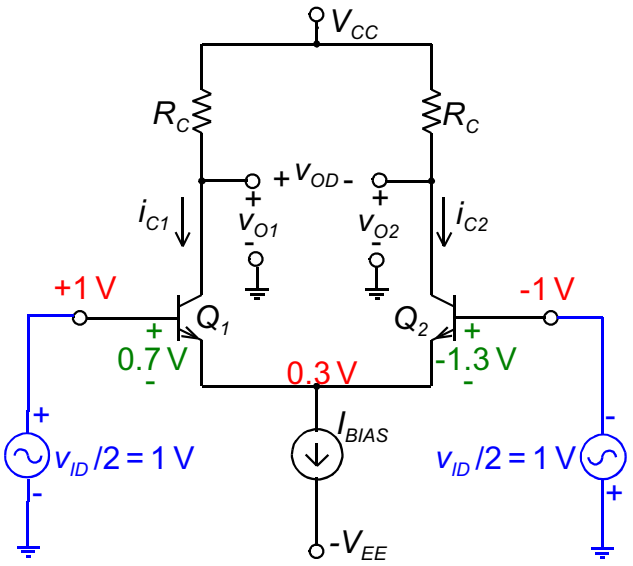

Fig. 323. Differential amplifier with +2 V differential input.

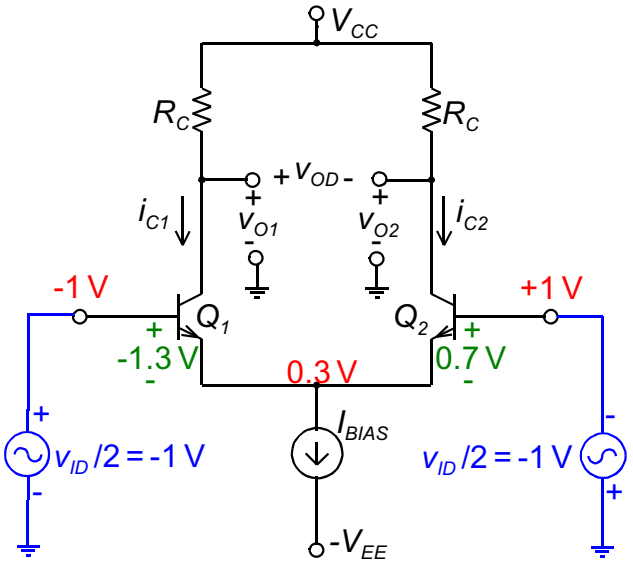

Fig. 324. Differential amplifier with -2 V differential input.

Case #2A - Differential Input:

Now we let $v_{ID} = 2$ V and $v_{ICM} = 0$.

Note that Q_1 is active, but Q_2 is cutoff. Thus we have:

$$i_{C2} = 0 \quad \textbf{(348)}$$

$$v_{O2} = V_{CC} \quad \textbf{(349)}$$

$$i_{C1} = \alpha i_{E1} = \alpha I_{BIAS} \quad \textbf{(350)}$$

$$v_{O1} = V_{CC} - \alpha R_C I_{BIAS} \quad \textbf{(351)}$$

$$v_{OD} = -\alpha R_C I_{BIAS} \quad \textbf{(352)}$$

Case #2B - Differential Input:

This is a mirror image of Case #2A. We have v_{ID} = -2 V and $v_{ICM} = 0$.

Now Q_2 is active and Q_1 cutoff:

$$i_{C1} = 0 \quad \textbf{(353)}$$

$$v_{O1} = V_{CC} \quad \textbf{(354)}$$

$$i_{C2} = \alpha i_{E2} = \alpha I_{BIAS} \quad \textbf{(355)}$$

$$v_{O2} = V_{CC} - \alpha R_C I_{BIAS} \quad \textbf{(356)}$$

$$v_{OD} = \alpha R_C I_{BIAS} \quad \textbf{(357)}$$

These cases show that a *common-mode input is ignored*, and that a *differential input steers I_{BIAS} from one side to the other*, which reverses the polarity of the differential output voltage*!!!*

We show this more formally in the following sections.

Large-Signal Analysis of Differential Amplifier

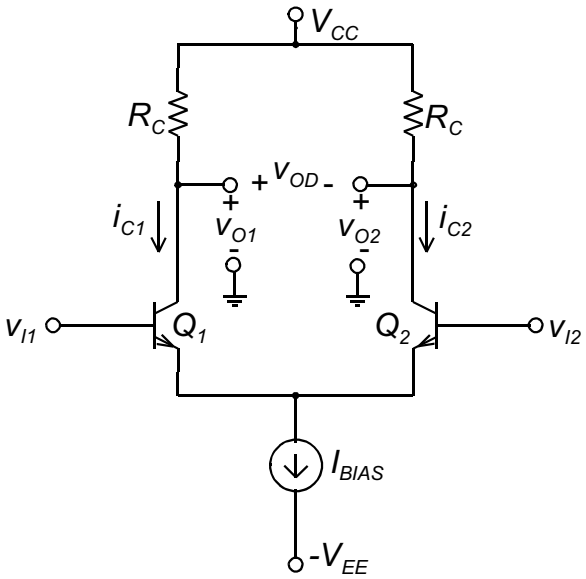

Fig. 325. Differential amplifier circuit (Fig. 321 repeated).

We begin by assuming identical devices in the active region, and use the forward-bias approximation to the Shockley equation:

$$i_{C1} = I_S \exp\left(\frac{V_{BE1}}{V_T}\right) \tag{358}$$

$$i_{C2} = I_S \exp\left(\frac{v_{BE2}}{V_T}\right) \tag{359}$$

Dividing eq. (358) by eq. (359):

$$\frac{i_{C1}}{i_{C2}} = \exp\left(\frac{v_{BE1} - v_{BE2}}{V_T}\right) = \exp\left(\frac{v_{ID}}{V_T}\right) \tag{360}$$

From eq. (360) we can write:

$$\frac{i_{C1}}{i_{C2}} + 1 = 1 + \exp\left(\frac{v_{ID}}{V_T}\right) \tag{361}$$

And we can also write:

$$\frac{i_{C1}}{i_{C2}} + 1 = \frac{i_{C1} + i_{C2}}{i_{C2}} = \frac{\alpha I_{BIAS}}{i_{C2}} \tag{362}$$

Equating (361) and (362) and solving for i_{C2}:

$$i_{C2} = \frac{\alpha I_{BIAS}}{1+\exp\left(\frac{v_{ID}}{V_T}\right)} \tag{363}$$

To find a similar expression for i_{C1} we would begin by dividing eqn. (359) by (358) . . . the result is:

$$i_{C1} = \frac{\alpha I_{BIAS}}{1+\exp\left(-\frac{v_{ID}}{V_T}\right)} \tag{364}$$

The current-steering effect of varying v_{ID} is shown by plotting eqs. (363) and (364):

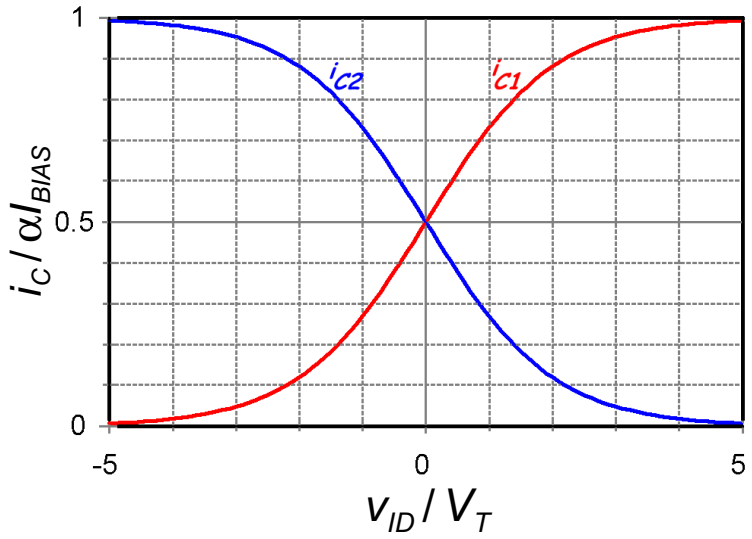

Fig. 326. Normalized collector currents vs. normalized differential input voltage, for a differential amplifier.

Note that I_{BIAS} is steered from one side to the other . . .as v_{id} changes from approximately -4V_T (-100 mV) to +4V_T (+100 mV)*!!!*

Using (363) and (364), and recalling that $v_{OD} = R_C(i_{C2} - i_{C1})$:

$$i_{C2} = \left[\frac{\alpha I_{BIAS}}{1+\exp\left(\frac{v_{ID}}{V_T}\right)}\right]\left[\frac{\exp\left(-\frac{v_{ID}}{2V_T}\right)}{\exp\left(-\frac{v_{ID}}{2V_T}\right)}\right] = \frac{\alpha I_{BIAS}\exp\left(-\frac{v_{ID}}{2V_T}\right)}{\exp\left(\frac{v_{ID}}{2V_T}\right)+\exp\left(-\frac{v_{ID}}{2V_T}\right)} \quad (365)$$

$$i_{C1} = \left[\frac{\alpha I_{BIAS}}{1+\exp\left(-\frac{v_{ID}}{V_T}\right)}\right]\left[\frac{\exp\left(\frac{v_{ID}}{2V_T}\right)}{\exp\left(\frac{v_{ID}}{2V_T}\right)}\right] = \frac{\alpha I_{BIAS}\exp\left(\frac{v_{ID}}{2V_T}\right)}{\exp\left(\frac{v_{ID}}{2V_T}\right)+\exp\left(-\frac{v_{ID}}{2V_T}\right)} \quad (366)$$

$$v_{OD} = -\alpha I_{BIAS} R_C \frac{\exp\left(\frac{v_{ID}}{2V_T}\right)-\exp\left(-\frac{v_{ID}}{2V_T}\right)}{\exp\left(\frac{v_{ID}}{2V_T}\right)+\exp\left(-\frac{v_{ID}}{2V_T}\right)} \quad (367)$$

$$v_{OD} = -\alpha I_{BIAS} R_C \tanh\left(\frac{v_{ID}}{2V_T}\right) \quad (368)$$

Thus we see that differential input voltage and differential output voltage are related by a hyperbolic tangent function*!!!*

A normalized version of the hyperbolic tangent transfer function is plotted below:

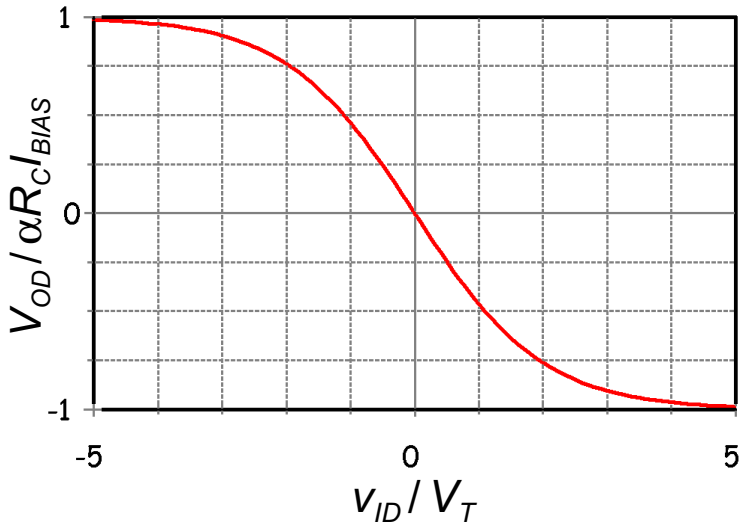

Fig. 327. Normalized differential output voltage *vs.* normalized differential input voltage, for a differential amplifier.

This transfer function is linear only for $|v_{ID}/V_T|$ *much less* than 1, i.e., for $|v_{ID}|$ *much less* than 25 mV*!!!*

We usually say the transfer function is acceptably linear for a $|v_{ID}|$ of 15 mV or less.

If we can agree that, for a differential amplifier, a *small input signal* is less than about 15 mV, we can perform a *small-signal analysis* of this circuit *!!!*

Small-Signal Analysis of Differential Amplifier

Differential Input Only

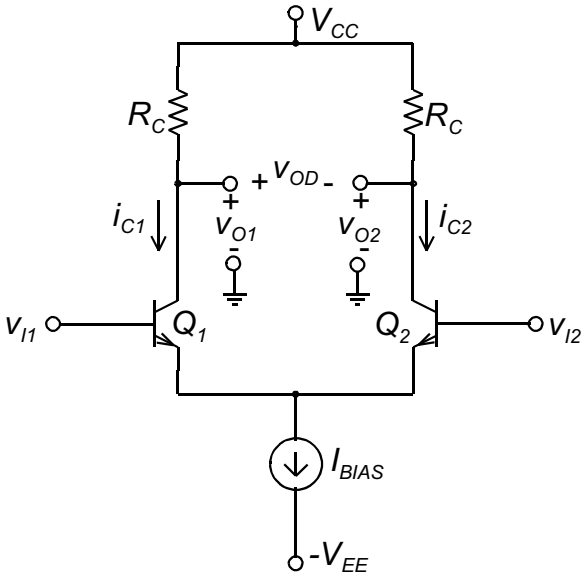

Fig. 328. Differential amplifier (Fig. 321 repeated).

We presume the input to the differential amplifier is limited to a purely differential signal.

This means that v_{ICM} can be any value.

We further presume that the differential input signal is *small* as defined in the previous section.

Thus we can construct the small-signal equivalent circuit using exactly the same techniques that we studied previously:

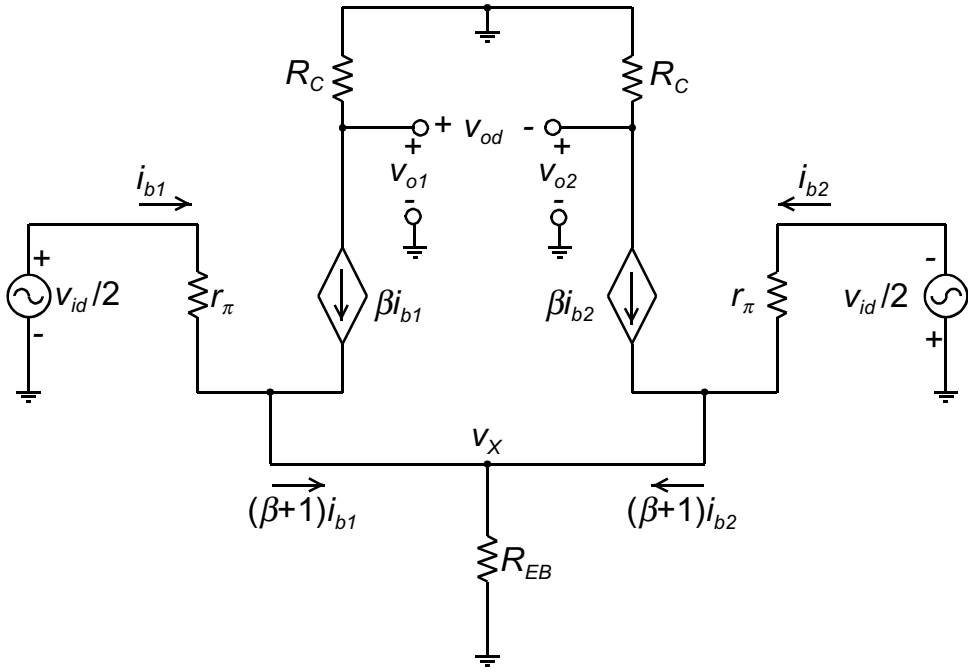

Fig. 329. Small-signal equivalent with a differential input. R_{EB} is the equivalent ac resistance of the bias current source.

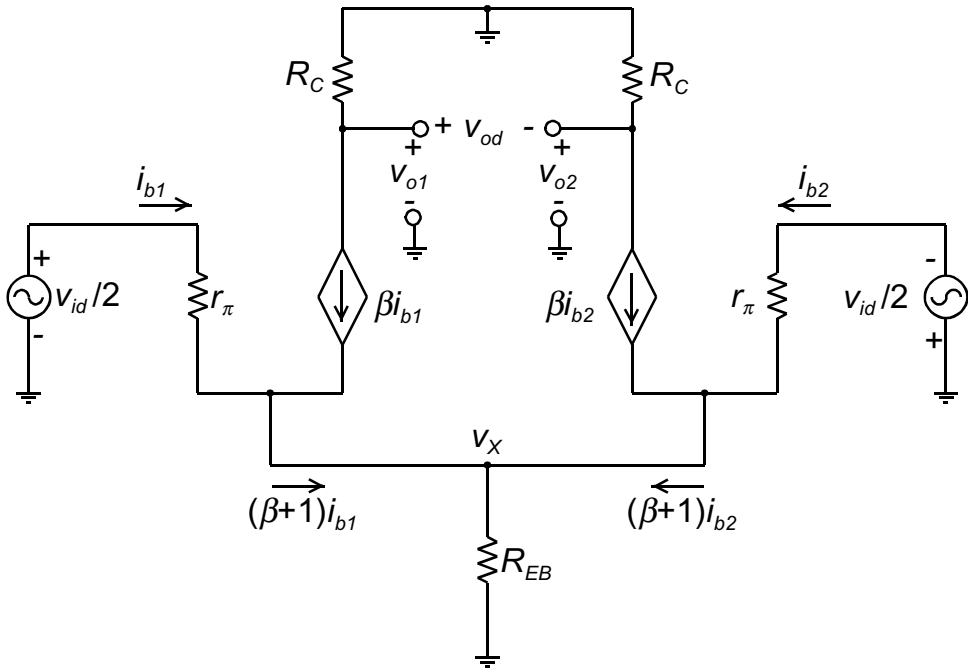

Fig. 330. Diff. amp. small-signal equivalent (Fig. 329 repeated).

We begin with a KVL equation around left-hand base-emitter loop:

$$\frac{v_{id}}{2} = i_{b1} r_\pi + (\beta + 1)(i_{b1} + i_{b2}) R_{EB} \tag{369}$$

and collect terms:

$$\frac{v_{id}}{2} = i_{b1}\left[r_\pi + (\beta + 1) R_{EB}\right] + i_{b2}\left[(\beta + 1) R_{EB}\right] \tag{370}$$

We also write a KVL equation around right-hand base-emitter loop:

$$-\frac{v_{id}}{2} = i_{b2} r_\pi + (\beta + 1)(i_{b1} + i_{b2}) R_{EB} \tag{371}$$

and collect terms:

$$-\frac{v_{id}}{2} = i_{b2}\left[r_\pi + (\beta + 1) R_{EB}\right] + i_{b1}\left[(\beta + 1) R_{EB}\right] \tag{372}$$

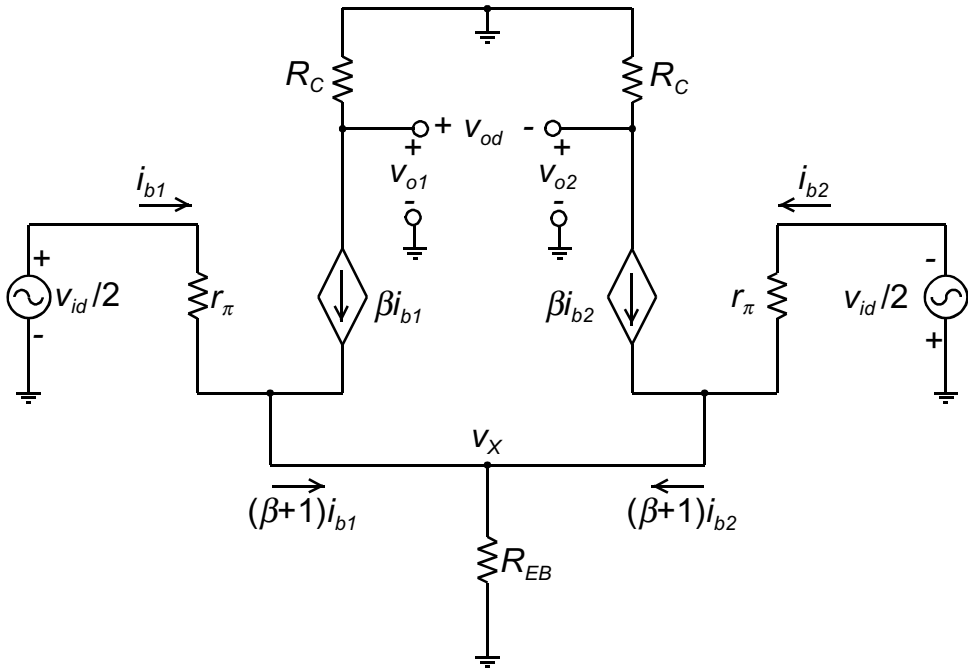

Fig. 331. Diff. amp. small-signal equivalent (Fig. 329 repeated).

Adding (370) and (372):

$$0 = \left(i_{b1} + i_{b2}\right)\left[r_\pi + 2(\beta + 1)R_{EB}\right] \tag{373}$$

Because neither resistance is zero or negative, it follows that

$$\left(i_{b1} + i_{b2}\right) = 0 \tag{374}$$

and, because $v_X = (i_{b1} + i_{b2})R_{EB}$, the voltage v_X must be zero, i.e., *point X is at signal ground for all values of R_{EB} !!!*

The junction between the collector resistors is also at signal ground, *so the left half-circuit and the right half-circuit are independent of each other, and can be analyzed separately !!!*

Analysis of Differential Half-Circuit

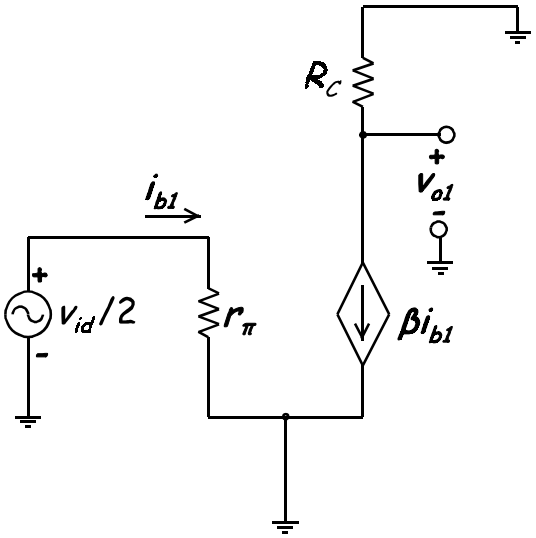

Fig. 332. Left half-circuit of differential amplifier with a differential input.

The circuit at left is just the small-signal equivalent of a common emitter amplifier, so we may write the gain equation directly:

$$\frac{v_{o1}}{v_{in}} = \frac{v_{o1}}{v_{id}/2} = \frac{-\beta R_C}{2r_\pi} \qquad \textbf{(375)}$$

For v_{o1}/v_{id} we must multiply the denominator of eq. (375) by two:

$$A_{vds1} = \frac{v_{o1}}{v_{id}} = \frac{-\beta R_C}{2r_\pi} \qquad \textbf{(376)}$$

In the notation A_{vds} the subscripts mean:

v, voltage gain *d*, differential input *s*, single-ended output

The right half-circuit is identical to Fig. 332, but has an input of $-v_{id}/2$, so we may write:

$$A_{vds2} = \frac{v_{o2}}{v_{id}} = \frac{\beta R_C}{2r_\pi} \qquad \textbf{(377)}$$

Finally, because $v_{od} = v_{o1} - v_{o2}$, we have the result:

$$A_{vdb} = \frac{v_{od}}{v_{id}} = \frac{-\beta R_C}{r_\pi} \qquad \textbf{(378)}$$

where the subscript *b* refers to a *balanced output*.

Thus, we can refer to differential gain for either a single-ended output or a differential output.

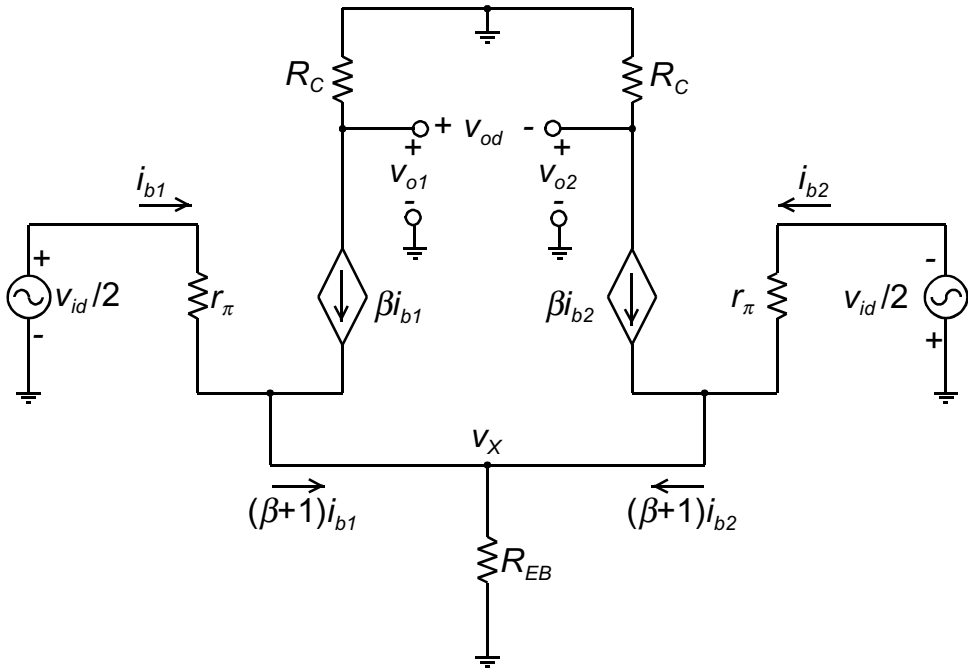

Fig. 333. Diff. amp. small-signal equivalent (Fig. 329 repeated).

Remember our hyperbolic tangent transfer function? Eq. (378) is just the slope of that function, evaluated at $v_{ID} = 0$ *!!!*

Other parameters of interest . . .

Differential Input Resistance

This is the small-signal resistance seen by the differential source:

$$\frac{v_{id}/2}{i_{b1}} = r_\pi \qquad \Rightarrow \qquad \frac{v_{id}}{i_{b1}} = R_{id} = 2r_\pi \tag{379}$$

Differential Output Resistance

This is the small-signal resistance seen by the load, which can be single-ended or balanced. We can determine this by inspection:

$$R_{os} = R_C \qquad \text{and} \qquad R_{od} = 2R_C \tag{380}$$

Common-Mode Input Only

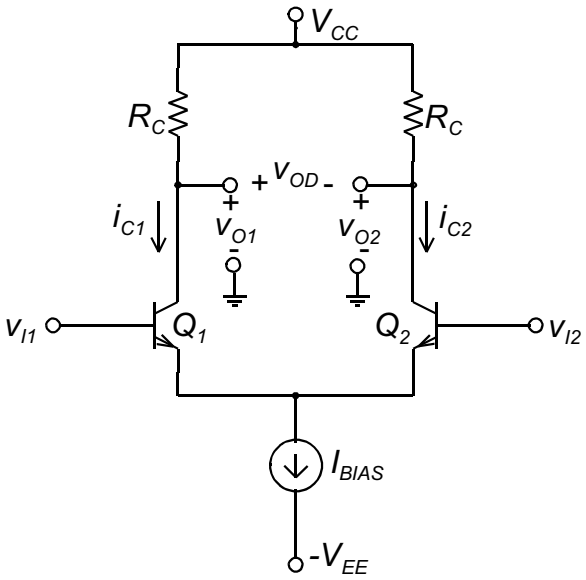

Fig. 334. Differential amplifier (Fig. 321 repeated).

We now restrict the input to a common-mode voltage only.

This is, we let $v_{ID} = 0$.

We again construct the small-signal circuit using the techniques we studied previously.

As a bit of a trick, we represent the equivalent ac resistance of the bias current source as two resistors in series:

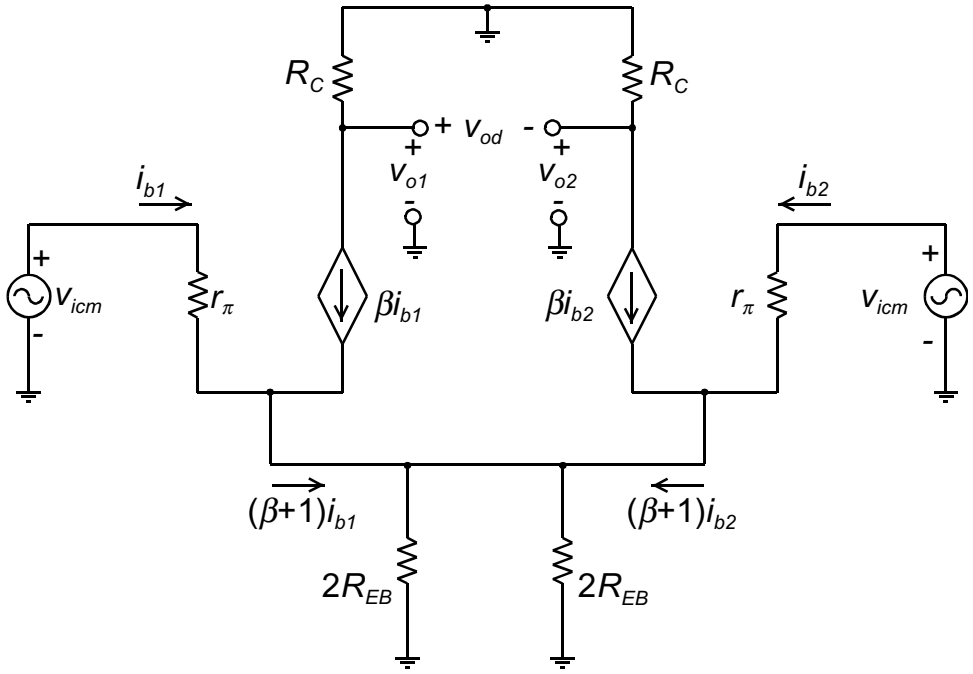

Fig. 335. Small-signal equivalent with a common-mode input. The resistance of the bias current source is represented by $2R_{EB} \,||\, 2R_{EB} = R_{EB}$.

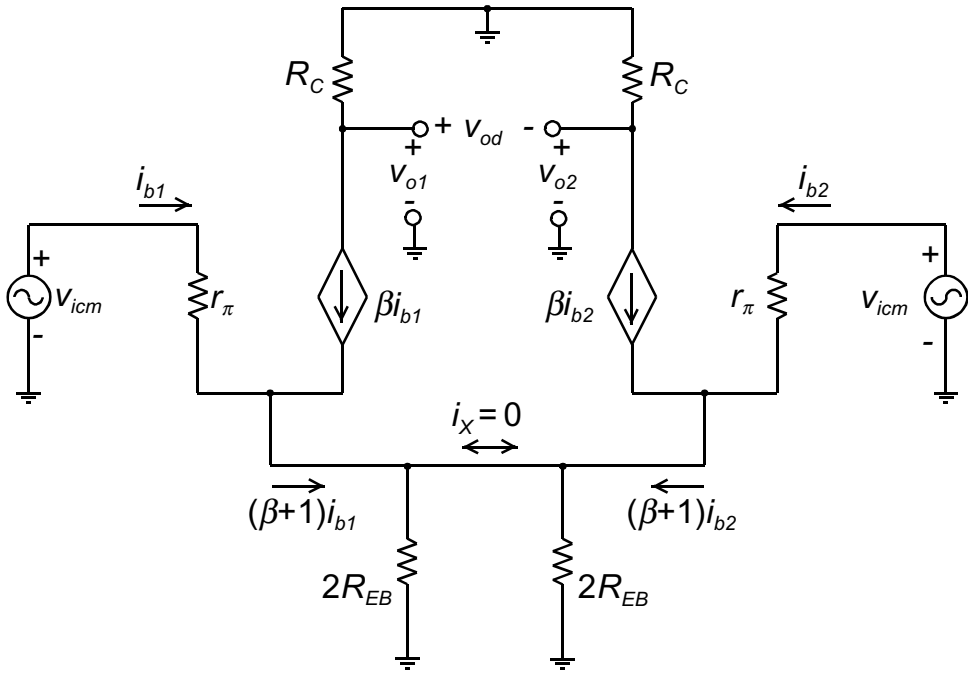

Fig. 336. Small-signal equivalent with a common-mode input. Note the current i_X.

The voltage across each $2R_{EB}$ resistor is identical because the resistors are connected across the same nodes.

Therefore, the current i_X is zero and *we can remove the connection between the resistors !!!*

This "decouples" the left half-circuit from the right half-circuit at the emitters.

At the top of the circuit, the small-signal ground also decouples the left half-circuit from the right half-circuit.

Again we need only analyze one-half of the circuit *!!!*

Analysis of Common-Mode Half-Circuit

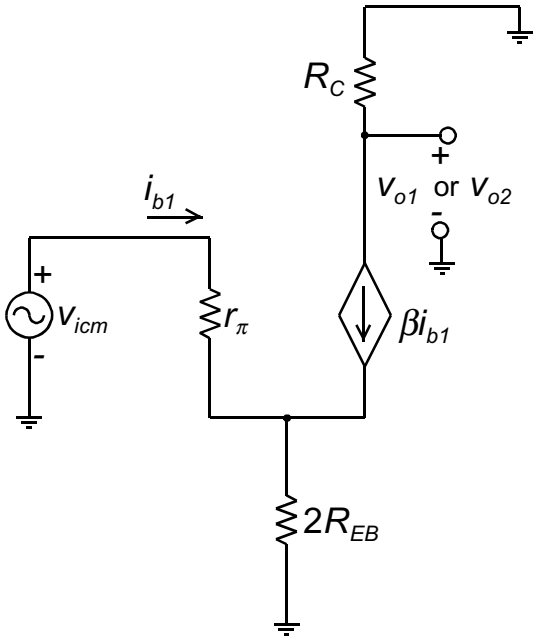

Fig. 337. *Either* half-circuit of diff. amp. with a common-mode input.

Again, the circuit at left is just the small-signal equivalent of a common emitter amplifier (this time with an emitter resistor), so we may write the gain equation:

$$\frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}} = \frac{-\beta R_C}{r_\pi + (\beta+1)2R_{EB}} \qquad \textbf{(381)}$$

Eq. (381) gives A_{vcs} , the common-mode gain for a single-ended output.

Because v_{o1} = v_{o2} , *the output for a balanced load will be zero*:

$$A_{vcd} = 0 \qquad \textbf{(382)}$$

Common-mode input resistance:

Because the same v_{icm} source is connected to *both* bases:

$$R_{icm} = \frac{v_{icm}}{i_{b1} + i_{b2}} = \frac{v_{icm}}{2i_{b1}} = \frac{1}{2}\left[r_\pi + (\beta+1)2R_{EB}\right] \qquad \textbf{(383)}$$

Common-mode output resistance:

Because we set independent sources to zero when determining R_o, we obtain the same expressions as before:

$$R_{os} = R_C \qquad \text{and} \qquad R_{od} = 2R_C \qquad \textbf{(384)}$$

Common-Mode Rejection Ratio

CMRR is a measure of how well a differential amplifier can amplify a differential input signal while rejecting a common-mode signal.

For a single-ended load:

$$CMRR = \frac{A_{vds}}{A_{vcs}} = \frac{r_\pi + (\beta + 1)2R_{EB}}{2r_\pi} \approx \frac{\beta R_{EB}}{r_\pi} \qquad \textbf{(385)}$$

For a differential load *CMRR* is theoretically *infinite* because A_{vcd} is theoretically zero. In a real circuit, *CMRR* will be *much* greater than that given above.

To keep these two *CMRR*s in mind it may help to remember the following:

- A_{vcs} = 0 if the bias current source is ideal (for which $R_{EB} = \infty$).
- A_{vcd} = 0 if the circuit is symmetrical (identical left- and right-halves).

CMRR is almost always expressed in dB:

$$CMRR_{dB} = 20 \log CMRR \qquad \textbf{(386)}$$