Testing Interconnects for Noise and Skew in Gigahertz SoCs

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ABSTRACT

Voltage distortion (noise) and delay violations (skew) contribute to the signal integrity loss and ultimately functional error, performance degradation and reliability problems. We present a BIST-based test methodology that includes two special cells to detect and measure noise and skew occurring on the interconnects of the gigahertz system-on-chips.

I. INTRODUCTION

With fine miniaturization of the VLSI circuits and rapid increase in the working frequency (gigahertz range) of digital system-on-chips (SoC), the signal integrity becomes a major concern for design and test engineers. Although various parasitic factors for transistors can be well controlled during fabrication, the parasitic capacitances, inductances and their cross coupling effects on the interconnects play a significant role in the proper functionality and performance of high-speed SoCs. As we approach $100nm$ technology, the effect of interconnect on the signal integrity is becoming one of the main concerns in testing gigahertz system-on-chips.

Signal integrity is the ability of a signal to generate correct responses in a circuit. It generally includes all effects that cause a design to malfunction due to the distortion of the signal waveform. According to this informal definition, a signal with good integrity has: (i) voltage values at required levels and (ii) level transitions at required times. For example, an input signal to a flip-flop with good signal integrity arrives early enough to guarantee the setup and hold time requirements and it does not have spikes causing undesired logic transition.

A. Prior Work

Various signal integrity problems have been studied previously for radio frequency (RF) circuits and recently for high-speed deep-submicron VLSI chips. The most important ones are: *crosstalk* (signal distortion due to cross coupling effects between signals) [CDBZ99] [ChGB98], *overshoot* (signal rising momentarily above the power supply voltage) [FTCH98] [Lebl96], *reflection* (echoing back a portion of a signal), *electro-magnetic interference* (resulting from the antenna properties) [KiNa99], *power supply noise* [ZhRo00] and *signal skew* (delay in arrival time to different receivers) [ChWa97][CSKW96].

There is a long list of possible design and fabrication solutions to enhance signal integrity on the interconnect. None guarantees to resolve the issue perfectly. These solutions include: 3-D layout modeling and parasitic extraction [Gree99], accurate RLC simulation of on-chip power grid [ChWa97], using decoupling capacitors to limit the maximum dV/dt [DoGK93][ZhRo00] and to improve IR-drop [ChWa97][SaOT98], inserting repeaters/buffers on the interconnects [Gree99] and shielding wires (e.g. grounding every other line) [KaMS99].

Noise and skew imposed by interconnects have emerged as main concerns in the interconnect design of gigahertz SoCs. Buffer insertion and transistor resizing methods [TeSa97] [JSBK98] are used as two design techniques to achieve better power-delay and area-delay tradeoffs. Self-test methodologies have been developed to test signal integrity in high-speed SoCs. Testing crosstalk in chip interconnects [CDBZ99][BaDR00] and a BIST (built-in self-test) structure using D flip-flops that detects the propagation delay deviation of operational amplifiers

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[RaVN99] are among such methods.

B. Contribution and Paper Organization

Our main contribution is an on-chip mechanism to detect noise and skew violations occurring on the interconnects of high-speed SoCs. We present special cells to monitor signals received from the system interconnect and record the occurrence of signal entering the vulnerable region over a period of operation. By resizing transistors within these cells, they can be easily tuned to define the acceptable levels of noise and skew. We also propose a BIST methodology that uses pseudo-random patterns and accumulates the integrity test information using the detector cells. The statistics will be eventually sent out for final test analysis, reliability judgment and diagnosis.

The rest of this paper is organized as follows. The signal integrity model and test strategy are discussed in Section II. Section III and IV analyze CMOS circuits that detect noise and skew violations occurring on the interconnects, respectively. Section V explains the test architecture to store and read out the information. The experimental results are discussed in Section VI. Finally, the concluding remarks are in Section VII.

II. Integrity Test Methodology

The origin of signal integrity problems (i.e. noise and skew) lies in the circuit interconnects [NTOG98]. In low and mid-range frequencies, common in the past, the RC delays have been the dominating factors in the global interconnect delay and distortion. Inductance (L) effects are becoming increasingly important as the frequency of operation increases.

There
are numerous efficient distributed interconnect models in the literature [CLLC00][Veen98][Shee99]. The values of distributed R, L, C and the number of segments depend on many factors including the operating frequency, the length of the interconnect and technology. All simulation results reported in this work are based on distributed RLC model as reported in [CLLC00][NoAt01].

A. A Model for Signal Integrity

True characteristics of a signal is reflected in its waveform. Recent interconnect simulation, design and optimization methods not only consider peak voltage and delay, but also take into account the signal waveform [CoHe99] [ReRW99]. In reality, electronic components can tolerate certain level of noise. For example, a CMOS gate interprets any voltage in the $[V_{Hmin}, V_{dd}]$ range as logic "1" and any voltage in the $[V_{ss}, V_{Lmax}]$ range as logic "0". Frequently, digital circuits are designed to tolerate certain amount of skew delay, i.e. T_{SI_R} for rising delay and T_{SI_F} for falling delay (see Figure 1).

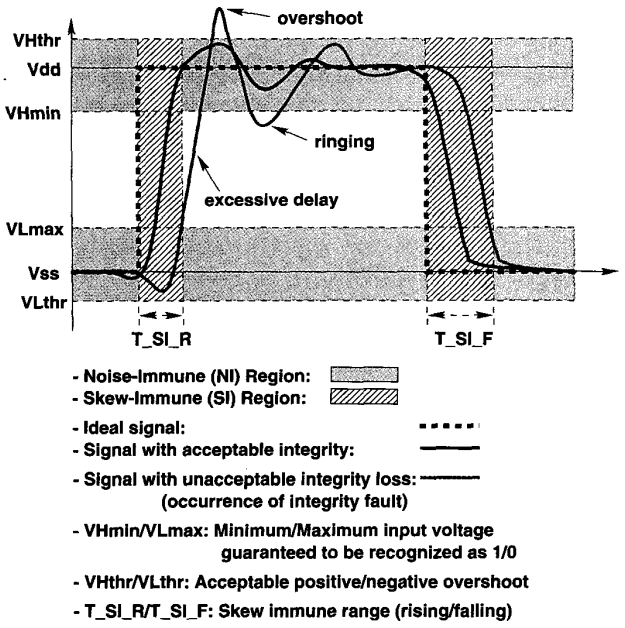

Fig. 1. Immune regions and the concept of integrity loss.

In practice, circuits have *noise-immune* (NI) regions that tolerate certain level of voltage swing and *skew-immune* (SI) regions that tolerate certain level of delay. Any portion of signal that exits the NI and SI regions indicates the integrity loss. This concept has been shown graphically in Figure 1 in which the shaded and unshaded (white) strips show the immune and vulnerable regions, respectively.

The focal point in this paper is the NI and SI regions and a mechanism to detect signals that exit these regions. Leaving the NI-region not only causes error in functionality (ringing), but also repeated overshoots are known to inject high-energy electrons and holes (also called *hot-carriers*) into the gate oxide that ultimately cause permanent degradation of MOS transistors' performance and reliability [FTCH98] [Lebl96].

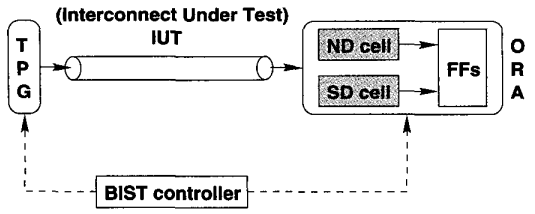

Fig. 2. BIST Architecture.

Leaving the SI-region means that the interconnect adds unacceptable skew delay that may lead to functional error or serious performance degradation.

B. BIST-Based Test Methodology

At-speed testing (testing system functionality at its nominal working frequency) is a necessity for manufacturing test and validation of system performance. However, the ATE (automatic test equipment) speeds have always lagged behind the CUT (circuit under test) speed. As a result of this speed difference, the high-speed circuits are tested at clock rates that are much slower than their specification [SIA99] [Flin94]. Furthermore, the pin and probing limitations of ATEs restrict the accurate observation of test results. Therefore, an on-chip test mechanism such as BIST can fulfill requirements for at-speed testing of complex high-speed SoCs.

In BIST architecture, a TPG (test pattern generation) circuit generates the pseudorandom patterns to stimulate possible defects in the CUT. The ORA (output response analyzer) circuit observes the outputs and analyzes their validity [AbBF90]. Figure 2 demonstrates our basic BIST-based architecture to test the SoC's interconnects for integrity. The TPG and ORA circuits are located in two sides of the IUT (interconnect under test). The IUTs could be long interconnects or those suspicious of having noise/skew violations due to environmental factors (e.g. crosstalk, electromagnetic effects, etc.).

Researchers have searched for test patterns causing the worst case of signal integrity to enhance their test quality. In [BaDR00] and [CDBZ99], the worst case test patterns associated with a specific fault model (MAFM) were presented. They used the RC model of the interconnect to generate test patterns and applied identical transitions to all wires except the victim net to create maximal integrity loss in the victim wire.

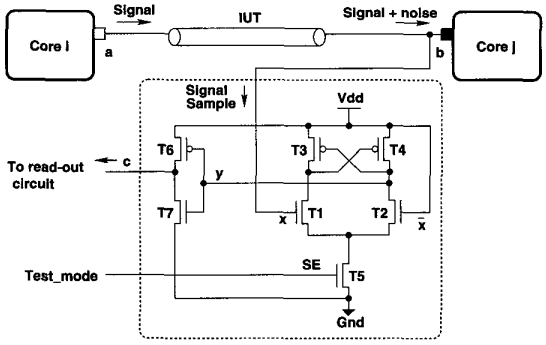

Fig. 3. The ND cell using cross-coupled PMOS amplifier.

Our rationale in using pseudorandom patterns for integrity testing is the fact that finding patterns that are guaranteed to create the worst case scenarios for integrity loss (e.g. noise and skew) is almost impractical with the current state of knowledge. This is mainly due to the complexity of distributed RLC interconnect model, parasitic values and too many influential factors. The approaches reported so far in literature consider limited integrity loss [BaDR00] and the results are inconclusive. In [NoAt01], we have presented empirical evidences indicating that random patterns are more qualified than those conjectured to create the worst case integrity loss. Since the focus of this paper is on the observation part (i.e. noise/skew detection cells), we do not pursue the test pattern generation issue further.

Integrity loss cannot be captured using conventional ORAs due to the complexity of interconnect behavior. Hence, a complete ORA circuitry, which includes ND (noise detector) and SD (skew detector) cells will be used in this work. The ND and SD cells detect voltage and timing violations of the signal, respectively. We will elaborate on their structures and behaviors in the next two sections.

III. Detecting Noise Violation

A modified cross-coupled PMOS differential sense amplifier is designed to detect integrity loss (noise) relative to voltage violations. Figure 3 shows the noise detector (ND) cell, which sits physically near the receiving core and samples the actual signal plus noise received by *Core j*.

Figure 4 shows signals on the input and output (points *b* and *c*) of the cell to validate the behavior of our noise detector cell. Each time that noise occurs

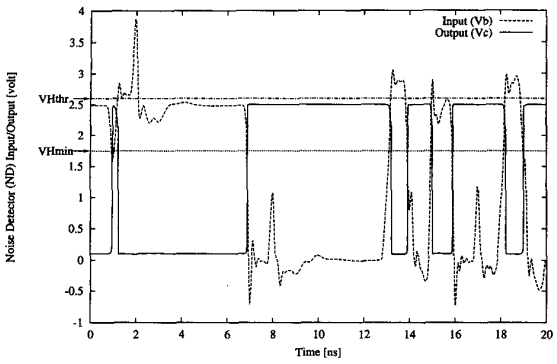

Fig. 4. The SPICE simulation of the ND cell for the top vulnerable region.

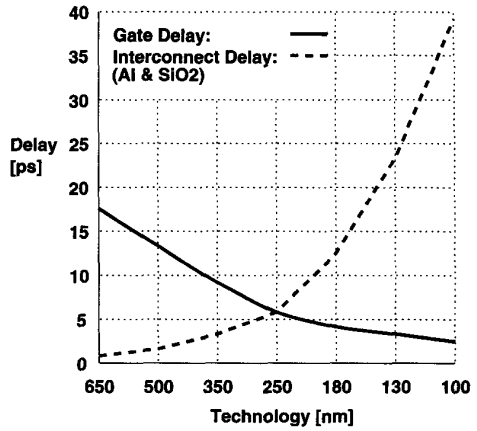

Fig. 5. Gate and interconnect delay versus technology.

(i.e. $V_b > V_+ = V_{Hthr}$), the ND cell generates a "0" signal that remains unchanged until V_b drops below $V_- = V_{Hmin}$. The waveforms in Figure 4 reflect that the ND cell shows a *hysteresis* (Schmitt-trigger) property which implicitly indicates a (temporary) storage behavior. This property helps to detect the violation of two threshold voltages (i.e. V_{Hthr} and V_{Hmin}) with the same ND cell. A similar cell can be designed to detect crossing V_{Lthr} and V_{Lmax} threshold voltages. Details can be found in [NoAt01].

The unacceptable level of noise (integrity) (i.e. V_{Hthr} and V_{Hmin}) is a matter of test and reliability debate. For instance, some researchers estimated that $0.1V_{dd}$ or more overshoot values create hot-carriers and thus may lead to a permanent damage [CLLC00]. Although the level of unacceptable noise can vary, our ND cell can be accurately tuned by resizing transistors T_1 through T_4 to meet the desired noise level, as described in [NoAt01].

IV. Detecting Skew Violation

As stated in Section I, in addition to voltage distortion, timing violation (skew) is another important factor that contributes directly to the integrity loss. Specifically, in deep sub-micron technology the interconnect delay is a detrimental factor. Figure 5, presented in the SIA roadmap [SIA99], shows the gate and interconnect delays versus technology generations. The curves clearly show the dominance of interconnect delay over gate delay as we approach $100nm$ technology. Using copper (instead of aluminium) and low dielectric constant insulators can reduce the delay of interconnects. However, it is certain that the interconnect delay will remain the dominating factor [SIA99]. This trend justifies the efforts needed to detect the delay violation due to the interconnect.

A. Skew Immunity Range

We defined the skew-immune (SI) region in Figure 1 as the delay range that is considered "acceptable". If signal skew goes beyond that range we consider it as serious integrity loss. The range of immunity depends on the system topology, speed, core interactions and the yield margin that a designer defines to achieve the nominal performance of the system. Such yield margin is often considered in the design phase. However, the delay values of components as well as interconnects may not eventually be kept within such bound since the layout generation tools and the fabrication process each may add additional delays. More importantly, as we have discussed in [NoAt01] signal integrity factor in general and noise/skew in particular are data-dependent phenomena that cannot be predicted accurately through analytical or simulation based approaches. Thus, similar to the noise detection only an on-chip methodology can successfully test the delay violation.

In synchronous systems, maximum communication speed between two interacting cores depends on the maximum storage-to-storage (s-to-s) path delay [Wake00]. Figure 6 shows this graphically. As long as $T_{clock} > T_{interconnect} + T_{comb\_max} + T_{CQ} + T_{setup}$ the functionality of system will remain error-free. For simplicity, we did not differentiate between rising and falling skews. Thus, the skew immune range T_{SI} can

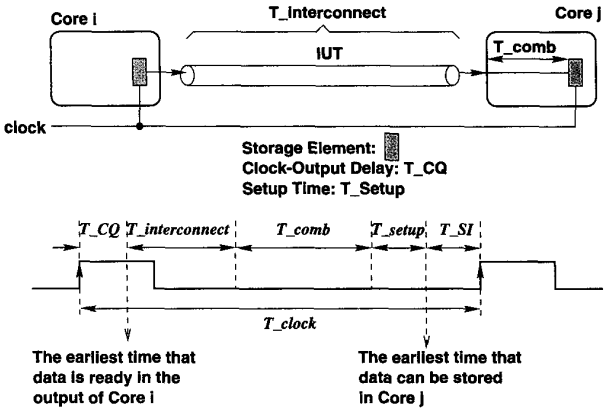

Fig. 6. The effect of interconnect skew (delay).

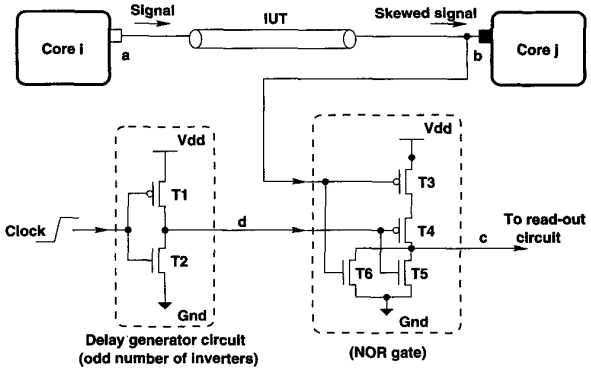

Fig. 7. Skew Detector circuitry (SD cell).

be estimated based on the clock period, timing behavior of the storage elements and storage-to-storage paths within the system:

$$T_{SI} \approx \max_{s-to-s} \{T_{clock} - (T_{comb\_max} + T_{CQ} + T_{setup})\}$$

B. Skew Detector (SD) Cell

In designing high speed cores, very firm delay budget has to be met. Any minor violation of skew or unpredictable delay (e.g., the interconnect effect) may cause functional error or significant degradation of performance. Numerous research endeavors have been dedicated to the testing of logic gates for their timing behavior [SpMR99][MaAg98]. Since the interconnect skew delay will be the dominant factor in determining the clock period of future technologies, it is essential to detect the skew violation on the interconnects.

Detecting the skew violations of interconnects can unlikely be fulfilled off-chip due to the speed limitations of ATEs. Nevertheless, the features of an on-chip test mechanism such as BIST can be utilized to observe the skew violations accurately. Figure 7 depicts the proposed on-chip test circuitry (SD cell). A delay generator cell is used to create the desired delay value (i.e. acceptable skew-immune range T_{SI}) as it is defined by a designer based on the delay budget of the interconnect. This cell is essentially made of odd number of cascaded CMOS inverters that receives the system clock and outputs the delayed inverted clock. The delayed clock is compared with the interconnect output. If the skew of the signal on the interconnect output is not within the acceptable range, the SD cell issues a pulse. The duration of this pulse depends on the interconnect delay. From testing point of view, the pulse generated by the SD cell can be used as the indication of skew violation. For example, it can trigger a D flip-flop to store a "1" as indication of such occurrence.

The SPICE [TISP00] simulation of the SD cell has been illustrated in Figure 8 for two signals. The first signal (*SIGNAL1*) does not violate the skew limit (T_{SI}) and thus the output of the cell remains zero. The second signal (*SIGNAL2*), however, exceeds the acceptable skew and the SD cell generates a pulse. As shown in the figure, this pulse appears in the output of the SD cell after delay associated with the NOR gate. Notice that possible clock skew does not have significant effect on the behavior of the SD cell. There are many approaches such as [TeSa97][LiCL96] to minimize the clock skew in a large chip. However, in the presence of clock skew T_{SI} changes to $T_{SI} + T_{clock\_skew}$ where the T_{clock_skew} is the skew on the clock wire attached to the SD cell. This change increases the acceptable skew range to which the cell reacts but the functionality of the cell remains intact.

To illustrate the true behavior of the SD cell in test mode, while connected to an interconnect, we ran the SPICE simulation on the integrated interconnect and test circuitry. The results are shown in Figure 9. If the output of interconnect does meet the skew requirements (less than $T_{SI} = 100ps$ as happens for *SIGNAL1*), the output of the SD cell stays at zero. However, a marginally late signal (*SIGNAL2*) causes a pulse at the output of the SD cell.

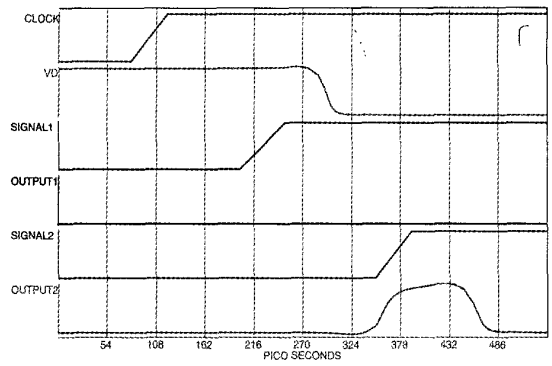

Fig. 8. The SPICE simulation of SD cell for two signals.

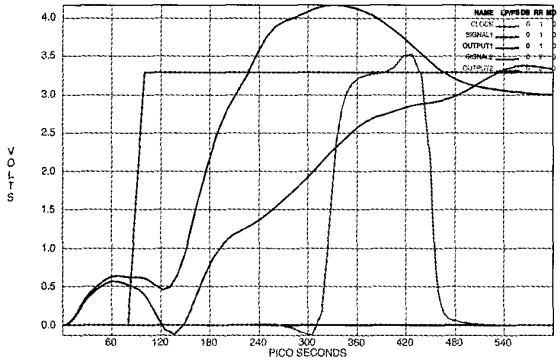

Fig. 9. The SPICE simulation of SD cell connected to an interconnect.

C. Delay Generator Circuit

As discussed before the accuracy of the SD cell depends on accurate implementation of delay generator block. This circuit generates a specific delay value (e.g. T_{SI}), predefined by the designer. The implementation of such accurate delay circuitry is a challenging issue. We have employed the classic driver design [AdFr98] [ZhLi91] to implement the delay generator circuit. Many researchers have extensively investigated how to achieve the optimal driver for long VLSI interconnects considering different objectives such as minimum delay, area or power consumption [LiCL96] [ZhLi91]. For instance, several design parameters, such as the number of drivers and their aspect ratio, are adjusted using optimization techniques to obtain an optimal driver configuration. Similarly, obtaining a specific delay value for a driver, while minimizing the overall area can be another objective in driver design problem. This can be the goal in optimizing the delay generator circuit. Such optimization technique, although important in our application, is beyond the scope of this paper. We simply comment that optimizing delay generator circuit can be done systematically using *optimal driver design* concept [TeSa97] [ZhLi91].

TABLE I
STATISTICS FOR FOUR DELAY GENERATOR CIRCUITS.

Design	*# of Inverters*	*Area* $[\mu m^2]$	*Delay* $[ps]$
#1	1	6	42
#2	1	2	87
#3	3	10.5	250
#4	3	15	410

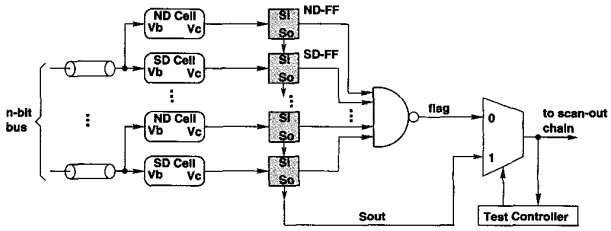

Fig. 10. Test architecture.

As for experimentation, we designed few delay generator circuits to show typical values for T_{SI}. Table I shows the specifications of four different delay generators. We used cascaded inverters with different size transistors to design and tune them. As seen in this table, the variety of delay values (i.e. T_{SI}) can be created using the inverters with reasonable area.

V. TEST ARCHITECTURE

Detecting signals that leave the noise-immune (NI) and skew-immune (SI) regions is a crucial step. This is performed by the ND and SD cells explained in the previous sections. These cells are not expensive – seven and six transistors per ND and SD cells, respectively. Overall two cells are needed per interconnect to detect noise (crossing V_{Hthr} and V_{Hmin}) and skew violations. The test architecture to read out the information stored in these cells is a DFT decision which depends on the overall SoC test methodology, testing objective and cost consideration.

Figure 10 demonstrates a scan flip-flop chain ar-

chitecture, which is able to record the occurrence of noise/skew violation and transfer it to the output. In the test-mode, first the *flag* signal is transferred, through MUX, to the test controller. If noise or skew violation (low integrity signal) occurs ($flag = 1$), the content of flip-flops (ND-FFs and SD-FFs) are scanned out through S_{out} for further reliability and diagnosis analysis. Suppose an n-bit interconnect is under test for m cycles (i.e. m pseudorandom test patterns). The very pessimistic worst case scenario in terms of test time is a case in which all lines are subject to noise in all m test cycles. This situation requires overall m and $m \cdot n$ cycles for response capture and readout, respectively. In practice, a much shorter time (e.g. $k \cdot n$, where $k << m$) is sufficient since the presence of defects or environmental factors causing unacceptable level of noise/skew (integrity loss) is quite limited. In terms of test overhead, n ND cells, n SD cells and $2n$ scan flip-flops are needed.

VI. Simulation Results

The number of cores in the SoC and the number of input ports of cores do not influence the low-integrity (noise/skew) detection process since the ND and SD cells independently function near core input ports. They do, however, influence the cost of test overhead (e.g. cells and FFs) and test time (e.g. scan-out time).

The experimental results here are reported using SPICE [TISP00]. We analyzed five main buses (data, address, control and two internal) of the famous 8051 microprocessor [Inte94]. In our implementation the 7 cores communicate through these buses and are potentially subject to noise in high frequency. For experimentation purpose, we used the interconnect architecture of 8051 assuming that it runs in 1 GHz. Typical global interconnect lengths in large SoC systems are chosen as the wire lengths in our experiments. Then, we have applied random patterns to the interconnects assuming that they run under 1 GHz frequency. The statistics are summarized in Table II. As shown in Table II, the average occurrence of unacceptable noise and skew (low integrity signals) in a presumed 1 GHz 8051 system will be 32.44% and 22.46% that may create functional error or cause severe damages (e.g. reliability, lifetime) on chip over time.

Table III summarizes the test overhead for the buses in 8051 reported by SYNOPSYS design compiler toolset [Syno00] when 100 random patterns are applied. We assumed that all interconnect lines need to be tested for integrity. All costs are expressed in terms of 2-input NAND gates. The readout time overhead results are also included in this table.

TABLE II
INTEGRITY TEST RESULTS FOR 8051 BUS STRUCTURE.

Buses	Bitwidth	Length [mm]	Noise [%]	Skew [%]
Data	8	20	43.38	31.32
Address	16	5	23.28	15.78
Control	10	10	28.50	25.53
Internal 1	10	10	34.40	21.20
Internal 2	8	10	32.62	18.47
Average	10.40	11.00	32.44	22.46

TABLE III
TEST OVERHEAD FOR 8051 BUS STRUCTURE.

Overhead	Data	Address	Control	Int. 1	Int. 2
Cost [NANDs]	158	254	194	194	158
Time [Cycle]	1600	3200	2000	2000	1600

A. The Effect of Process Variation

Variation of different factors in the fabrication process may cause considerable deviation from the nominal or expected behavior of the circuit. This may affect the integrity of signals traveling on the interconnect and also the functionality of the ND/SD cells. For example, due to the limited resolution of the photolitographic process, the transistor dimensions (W, L), on die may be different from the ideal dimensions expected. Other process parameters include transconductance (κ), threshold voltage (V_{th}), impurity concentration on densities, oxide thicknesses and diffusion depths [Raba96]. In this section we only show our simulation results on the sensitivity of the interconnect and cells with respect to different process variation factors. In-depth analysis of process variation is beyond the scope of this paper.

In all simulation results reported here, a normal distribution with $\sigma = 0.06\mu$ is used to generate variation on such factors. This means that the change of the nominal value will remain in $[\mu - 3\sigma, \mu + 3\sigma]$ range [Devo99]. The average value (μ) is the re-

sult of simulation without any variation of parameters. The value for variance (σ) is selected to keep the random parameter values between a lower and upper bound. In practice, such bounds depend on the statistical data extracted for each fabrication plant [MOSIS01]. The CODAC [TICO00] and TISPICE [TISP00] tools are used in a Monte-Carlo simulation environment to model and simulate the repercussion of process variations on the interconnects or cells. In each iteration the interconnect or cells is simulated using a randomly-chosen value for that specific process factor.

A.1 The Effect on the Interconnect

To examine the effects of process variations on the long interconnects parameters such as thickness, width, interlayer dielectric thickness, and contact resistance in fabrication process are taken into account as variances on the distributed R, L, and C values of the interconnect model.

Table IV shows the adverse effects of process variation on long on-chip interconnects when $R/L/C$ values are varied randomly using normal distribution. E obtained in the simulation expresses the percentage of violations (overshoot, undershoot or skew that are 20% larger than their nominal values) occurred on the interconnects. For example, 24.7% of the inputs cause significant overshoots, which reduces chip reliability.

Many researchers showed the importance of detecting skew and voltage violations of long interconnects on chips [NaBG98] [NaBC01]. Our simulation results also confirm this fact. Due to its probabilistic and environment-dependent nature, the process variation cannot be considered or modeled in the design phase. Thus, after fabrication a significant percentage of overshoots, violation of noise margin or settling time may appear on long interconnects. These situations can be only tested using an on-chip approach such as ours.

A.2 The Effect on the ND cell

To show the sensitivity of the ND cell with respect to the process variation, we have simulated the ND cell with variations of the different parameters. Using CODAC and SPICE, we trace the effect of variation of width (W), length (L), transconductance (κ), and threshold voltage (V_{th}) on the behavior of ND cell. Table V demonstrates the results. The last column in this table (E) shows the percentage of unacceptable outputs compared to the output of ND cell under no process variations for different parameters. As reflected in the table, the ND cell can quite adequately tolerate the variations on κ and length of transistors. However, the adverse effects of deviations of the threshold voltage and transistor width are larger.

TABLE IV
THE EFFECT OF PROCESS VARIATIONS ON THE INTERCONNECT.

Parameters	*Nominal* [μ]	E[%]
Peak Overshoot [*volt*]	1.62	24.7
Peak Undershoot [*volt*]	0.95	6.7
Skew Delay [*ns*]	0.4	4.7

TABLE V
THE EFFECT OF PROCESS VARIATIONS ON THE ND CELL.

Parameters	*Nominal* [μ]	E[%]
Width ($W_{T1}, \cdots, W_{T7}$) [μm]	4,4,8,7,4,1.2,4	6.2
Length [μm]	0.5	11.0
κ *(NMOS, PMOS)*	(0.161,9.366)	2.1
V_{th} *(NMOS, PMOS)* [*volt*]	(0.6684,−0.9352)	15.1

A.3 The Effect on the SD cell

Monte-Carlo simulations were also carried out for the SD cell. Table VI demonstrates the sensitivity of the SD cell due to the process variations. As tabulated, the SD cell can adequately tolerate variations on width, κ, and threshold voltage. The percentage of unacceptable skewed signals is less than 5% for above factors. However, the variations on the length of SD cell seem to be larger.

VII. CONCLUSION

The rising level of complexity and frequency of chips makes it increasingly difficult to achieve an adequate interconnect test using the ad-hoc techniques currently practiced in industry. Signal integrity is often degraded as signal travels through the interconnect. Such integrity loss may lead to functional error and reliability loss. We proposed a systematic BIST-based methodology to model and test signal integrity

TABLE VI
THE EFFECT OF PROCESS VARIATIONS ON THE SD CELL.

Parameters	*Nominal* [μ]	E[%]
Width ($W_1, W_2, \cdots, W_6$) [μm]	1.5,1,2,2,1,1	5.0
Length [μm]	0.5	17.5
κ *(NMOS, PMOS)*	(0.161,9.366)	0.6
V_{th} *(NMOS, PMOS) [volt]*	(0.6684,−0.9352)	2.6

in deep-submicron high-speed interconnects. Using inexpensive built-in noise and skew detection cells we offered an efficient architecture to capture and scan out the occurrences of noise and skew violations.

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