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Review on the Digital Control Laws for the High-Frequency Point-of-load Converters

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Abstract This review presents a practical evaluation of some digital control laws employed in Point-of-Load converters (PoL). For that, the high-frequency digital DC-DC converters test bank have been developed. The control laws are investigated by using Simulink models and they have been implemented by using the 16 bits DSC to validate them in high-frequency applications. This review lets to remark the pros and contras of each control laws for commercial PoL applications.

Keywords: *digital control, point-of-load converters, DC-DC converters, digital voltage-mode control, digital predictive current-programmed control*

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1. Introduction

The Digital Point-of-Load converters have significantly emerged in recent years. The boom of these converters is explained thanks to the notable benefits of digital systems [1]. Moreover, recent progress in microelectronic technologies are the source of significant improvements in commercial digital controllers. This new digital controllers allows implementing more accurate regulation systems in terms of accuracy and rapidness [2]. In consequence, digital systems replace progressively analogical control stages for more reliable and cheaper digitally-controlled ICs.

In brief, the digital power converter includes several stages. Firstly, one stage is dedicated to signal acquisition owning sensors, adaptation circuits and ADCs. Second stage is formed by the digital controller which will generate the digital control laws [3]. Different options of digital controllers are available depending on the expected performances of the final system and their resolution trade-offs. As an example, the resolution of the digital controller finite word and the maximal number of instructions to compute the algorithm are some limiting factors in digital controllers [4]. Finally, the output stage involves the DPWM module that generates the duty cycle for the power converter [5]. According to literature, the split digital control laws for power converters was explored [6]. First category corresponds to those based on the output voltage feedback regulation. Main differences between these laws are focus on the implementation of the voltage compensation network [7].

The digital current-programmed regulation techniques was explored. Previous works have verified the difficulty of modeling classical current-control techniques in the digital field, especially, in high-frequency applications [8]. In this technique, a strict tracking of the converter current is required to minimize the current error [9]. This fact is often difficult to achieve in the digital case due to the important sampling frequency needed. The digital approach of the peak-current technique in a Boost converter using the 8 bits PIC was explored [10]. Nowadays, predictive current-programmed control offers the best performances in digital converters [11]. The predictive algorithm calculates the duty cycle for next switching periods making that inductor current reaches the current reference in the determined number of cycles [12]. Other variations of predictive techniques, like estimative control, reconstructs the inductor current in order to predict the duty cycle for next switching periods [13]. Other control techniques are based on deadbeat controls where duty cycle is calculated in the limited number of cycles [14].

In this review, the method to design digital control laws for high-frequency PoL converters based on matlab-simulink models is illustrated [15]. For that, two digital control laws with their respective S-function models are present [16]. After, we implement the control laws using the same power plant to compare their performances in high switching frequency applications. First one belongs to Digital Voltage-Mode Control (DVMC) and the second one is a minor variation of the Digital Predictive current-programmed Control law (DPRC) [17]. Digital control can be used to implement the main control methods, and digital control offers the opportunity to implement more complex algorithms based in the quality and the amount of information available to make the decisions that can be combined to perform more sophisticated functions [18].

The goal of this review is to discuss about classical digital control laws and to discern the best one between voltage and current feedback regulation adapted for a high-frequency PoL converter application. This review is composed by four parts. After a brief introduction, the

matlab-simulink models of our high-frequency PoL converter are presented in the second chapter. Experimental results validating these digital control laws are shown in third part. Finally, conclusions are done in fourth chapter.

2. Theoretical Study of Control Laws

2.1. Selection of the Digital Compensation Network

One of the main discussion points is the structure of the voltage compensation network and its implementation as a digital filter. As a matter of fact, the compensation network architecture influences directly in the converter behavior. Thus, while some topologies are chosen for their higher accuracy, others are preferred by their lower computational cost.

For classical digital designs, equations of the digital filter representing the voltage compensation networks are shown in equations (1)-(4). On one hand, serial or incremental algorithms present the lower computational costs but they are very sensible to variations in the coefficients, thus, the stability of the converter using them is limited. On the other hand, parallel or position algorithms allow higher robustness face coefficients variations although they need more software instructions to be implemented. As a result, the final system is stable in a larger range of values but they are not performing in high-frequency applications due to the elevated delays that they introduce to the system. This later architectures admit three variations depending on how the integral part is calculated. Next, we present the digital control laws for each voltage compensation network.

Incremental PI:

$$u[n] = u[n\text{-}1] + K_1 \cdot e[n] + K_2 \cdot e[n\text{-}1] \quad (1)$$

with:

$$K_1 = K_p + \frac{K_i \cdot T_{sam}}{2}$$

$$K_2 = \frac{K_i \cdot T_{sam} - 2 \cdot K_p}{K_i \cdot T_{sam} + 2 \cdot K_p}$$

Position PI:

$$u[n] = u[n\text{-}1] + K_p \cdot e[n] + K_i \cdot G[n] \quad (2)$$

with:

$G[n] = y[n\text{-}1] + \frac{T_{sam}}{2} \cdot (e[n] + e[n\text{-}1])$ trapezoidal law

$G[n] = y[n\text{-}1] + T_{sam} \cdot e[n]$ backward Euler law

$G[n] = y[n\text{-}1] + T_{sam} \cdot e[n\text{-}1]$ forward Euler law

Incremental PI:

$$u[n] = u[n\text{-}1] + K_1 \cdot e[n] + K_2 \cdot e[n\text{-}1] + K_3 \cdot e[n\text{-}2] \quad (3)$$

with:

$$K_1 = K_p + \frac{K_i \cdot T_{sam}}{2} + \frac{K_d}{T_{sam}}$$

$$K_2 = -K_p - \frac{2 \cdot K_d}{T_{sam}} + \frac{K_i \cdot T_{sam}}{2}$$

$$K_3 = \frac{K_d}{T_{sam}}$$

Position PI:

$$u[n] = K_p \cdot e[n] + K_i \cdot G[n] + K_d \cdot (e[n] - e[n\text{-}1]) \quad (4)$$

2.2. Digital Voltage-mode Control

Digital output voltage feedback regulation has been traditionally used due to its easy implementation. The control design is easy since the current measurement is avoided and it requires only a simple measurement of the output voltage of the converter. Moreover, the sampling frequency has not to be very elevated due to the slow variations of the output voltage feedback loop.

Figure 1 show the Simulink model developed to study this control law. This model has been obtained using the Matlab S-Function where the digital control law algorithm can be directly integrated in the design by means of C code. Thanks to these functions, accurate simulations of the real system can be obtained. Moreover, to preserve the exactness of the model, fix-point, delay and quantification errors have been taken into account.

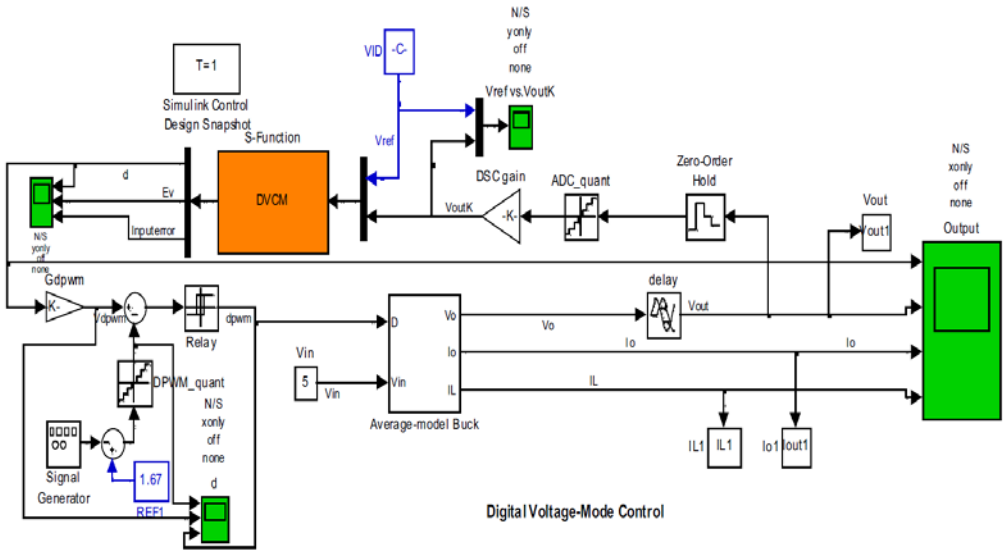

Figure 1. Simulink model of DVMC law

Then, the output voltage is measured and digitalized. Next, it is compared with a voltage reference before to be introduced in the voltage compensator network. The output of the compensator is calculated by means of any of the equations presented in equations (1)-(4). After, the DPWM calculates the duty cycle using next equation:

$$d[n] = d[n\text{-}1] + a \cdot u[n] \tag{5}$$

Where the coefficient "*a*" defines the dynamics of the system and $u[n]$ is the voltage compensator network output of the external loop. In equation (5), we see how the system achieves the steady-state when the error voltage is zero.

2.3. Digital Predictive Current-Programmed Control

The digital predictive current-programmed control law was developed [19]. The main idea is that inductor current reaches the current reference in a determined number of cycles. This current reference is imposed by the external voltage regulation loop [20]. Once the inductor current attains the reference, the current error is zero and the system reaches the steady state [21].

Then, the duty-cycle for the next switching period is calculated as follows [22]:

$$d[n] = \frac{L}{V_{in} \cdot T_{sw}} \cdot \left[i_c[n] - i_l[n] \right] + D \tag{6}$$

Where L corresponds to the inductor value, V_{in} the input voltage, T_{sw} the switching period, $i_c[n]$ the current reference, $i_l[n]$ the inductor current and D the steady-state duty cycle.

In order to achieve the digital voltage-mode control law, the sampling frequency has to be high enough to sample accurately the inductor current once (at least) at the beginning of each switching period [23]. In real high-frequency digital converters, this is difficult to achieve due to the conversion times of the ADCs and the inherent delays (delays of the signal propagation and the algorithm execution in the digital controller). As a result, main digital controllers cannot update the duty cycle each switching period when the switching frequencies are elevated.

Nevertheless, this control law can be adapted to be less exigent in terms of computational cost using equation (5). Then, equation (6) is adapted to:

$$d[n] = d[n\text{-}1] + a \cdot u[n] \tag{5}$$

with:

$$u[n] = e_v[n] - i_l[n]$$

Where e_v is the output of the voltage compensator network of the external loop and the coefficient "*a*" defines the dynamics of the system again [24]. Figure 2 shows the Simulink model developed for this control law.

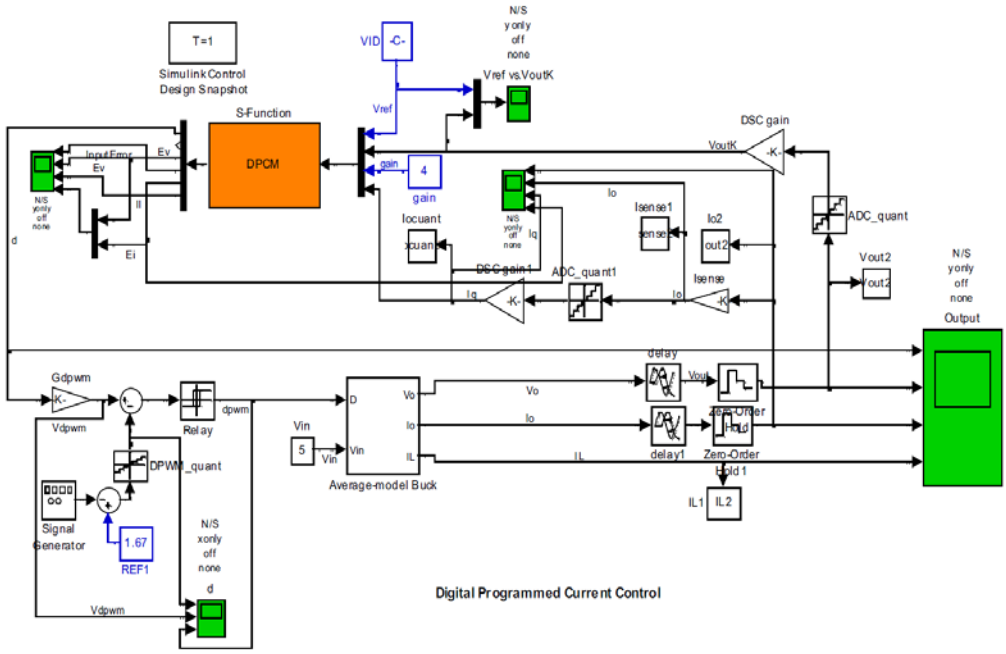

Figure 2. Simulink model of DPRC law

3. Matlab-simulink Simulation Results

Our models have been designed for a synchronous Buck converter. This step-down DC-DC converter topology is the preferred one in PoL converters because of its simplicity and its behavior is well-known. The converter parameters as observed in Table 1 have been selected according to current specifications of low-voltage, high-current DC-DC converters to supply power microprocessors [25].

Figure 3 is an example of the simulation results obtained with our models. We see the converter behavior against a load variation of 5A (20A). Output voltage (top) and current (bottom) are represented for DVCM and DPRC respectively.

The digital control laws designed in part II have been implemented in a PoL converter prototype using a 16 bits DSC of Freescale [26]. This fix-point DSC owns internal

built-in ADCs and DPWMs. Nevertheless, the elevated conversion time of the built-in ADC induces a significant delay that degrades the performances of the final system. At high switching frequencies, this delay reduces drastically the system stability. Each control law has a maximal acceptable delay and, beyond this limit, the system becomes oscillating. As a matter of fact, delay is more critical in DPRC than in DVMC due to the double analogical-to-digital conversion and the increase of the size of the algorithm. To solve this problem, we have developed at LAAS/CNRS an external acquisition board incorporating high-frequency ADCs (20MHZ). Thus, electrical signals can be sampled at higher frequencies and the algorithm execution times reduced.

Table 1. Converter parameters

Parameter	Value
Input Voltage	3-12 V (5 V typ)
Output Voltage	1 V
Output current	25 A max.
Switching freq.	1 MHz
Output Capacitor	410 µF
Input Capacitor	720 µF
R_{ds} Power Switch	7.5 mΩ
R_{ds} Synch. Switch	2.4 mΩ
Output Inductance	300 nH
Output Induct. DCR	0.588 mΩ
Output Capacitor ESR	2 mΩ
Input Capacitor ESR	1.27 mΩ

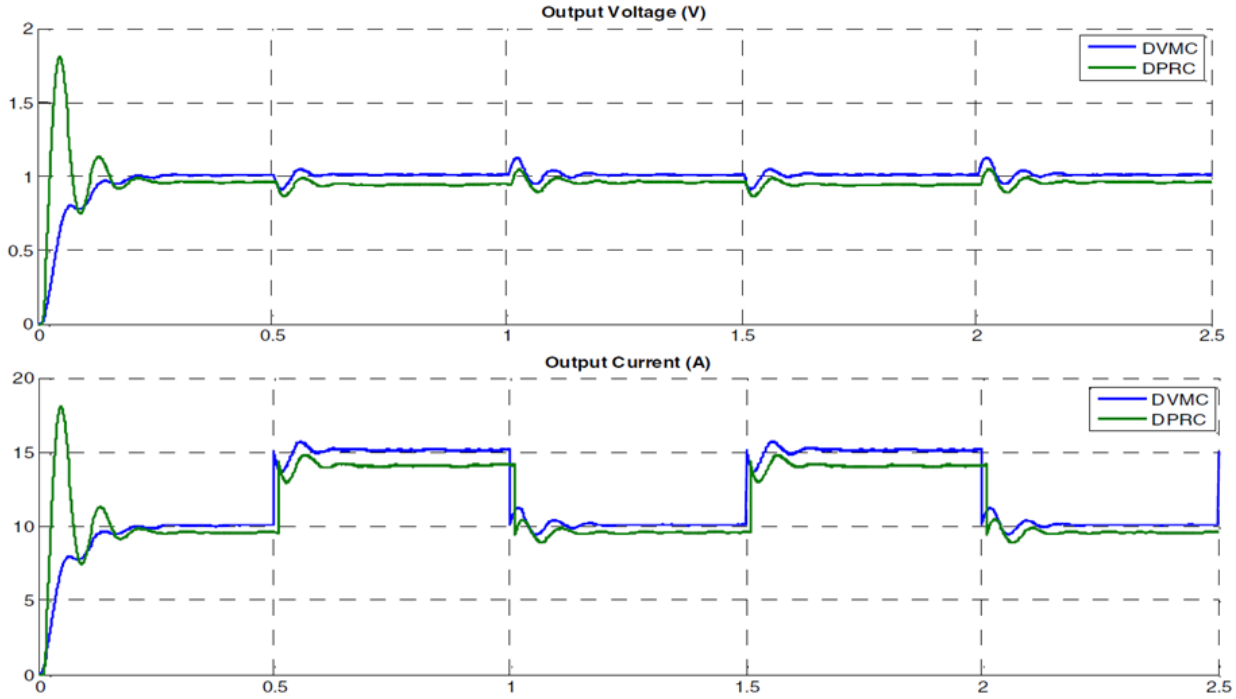

Figure 3. Simulation of ΔI_{out} = 5 A for DVCM and DPRC laws

Otherwise, it is well-known that the resolution of the DPWM has to be higher than the one of the ADC in order to avoid limit-cycle oscillations in the output magnitudes [27,28]. This fact is not accomplished in the MC56F8367EVM since the resolution of the built-in DPWM is depending of the converter switching frequency. In our case, for a switching frequency of 1MHz and a DPWM clock frequency of 60MHz (that means a time resolution of 16ns), we have 60 digital steps resulting in a resolution lower an 6 bits. The effect of this lack of resolution in the output module is observed in the left side of the Figure 4. Here, we observe how steady-state output voltage varies due to undesired changes in the PWM signal. These variations are produced because the digital output value of the control stage jumps between two digital values of the DPWM. On the other side, if the resolution is higher enough (DPWM quantification level smaller than in ADC), we avoid these errors in the output signals as observed in the right side of the Figure 4.

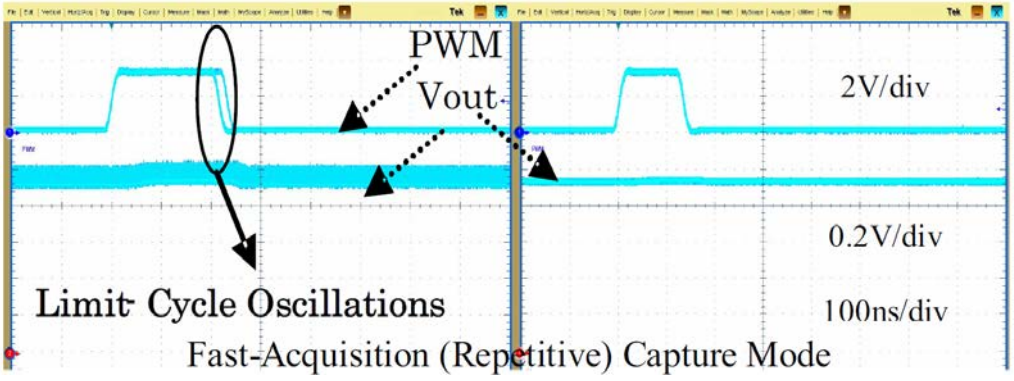

Figure 4. Effect of the cycle-limits in the output voltage

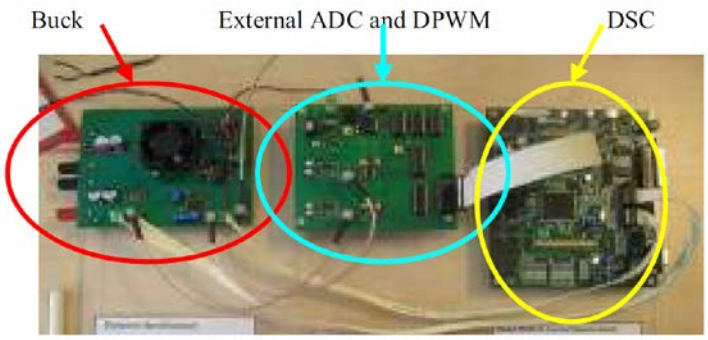

Figure 5. The prototype of our Digital DC-DC converter

The prototype of our Digital DC-DC converter is shown in Figure 5. Thus, we have also developed in the LAAS/CNRS and external 12bit DPWM to solve the lack of resolution of the internal DPWM and to avoid the cycle-limit oscillation problem. Table 2 resume the prototype parameters and the test conditions for the experimental results.

Table 2. Digital prototype results

	execution time (µs)	Settling time (µs)		Maximal peak (%)	
		Unders	Oversh	Unders	Oversh
DVMC Simulation	-	< 100	< 140	< 12	< 12
DVMC Experiment	5.04	< 100	< 100	< 18	< 18
DPRC Simulation	-	< 160	< 140	< 10	< 10
DPRC Experiment	6.74	< 130	< 140	< 14	< 20

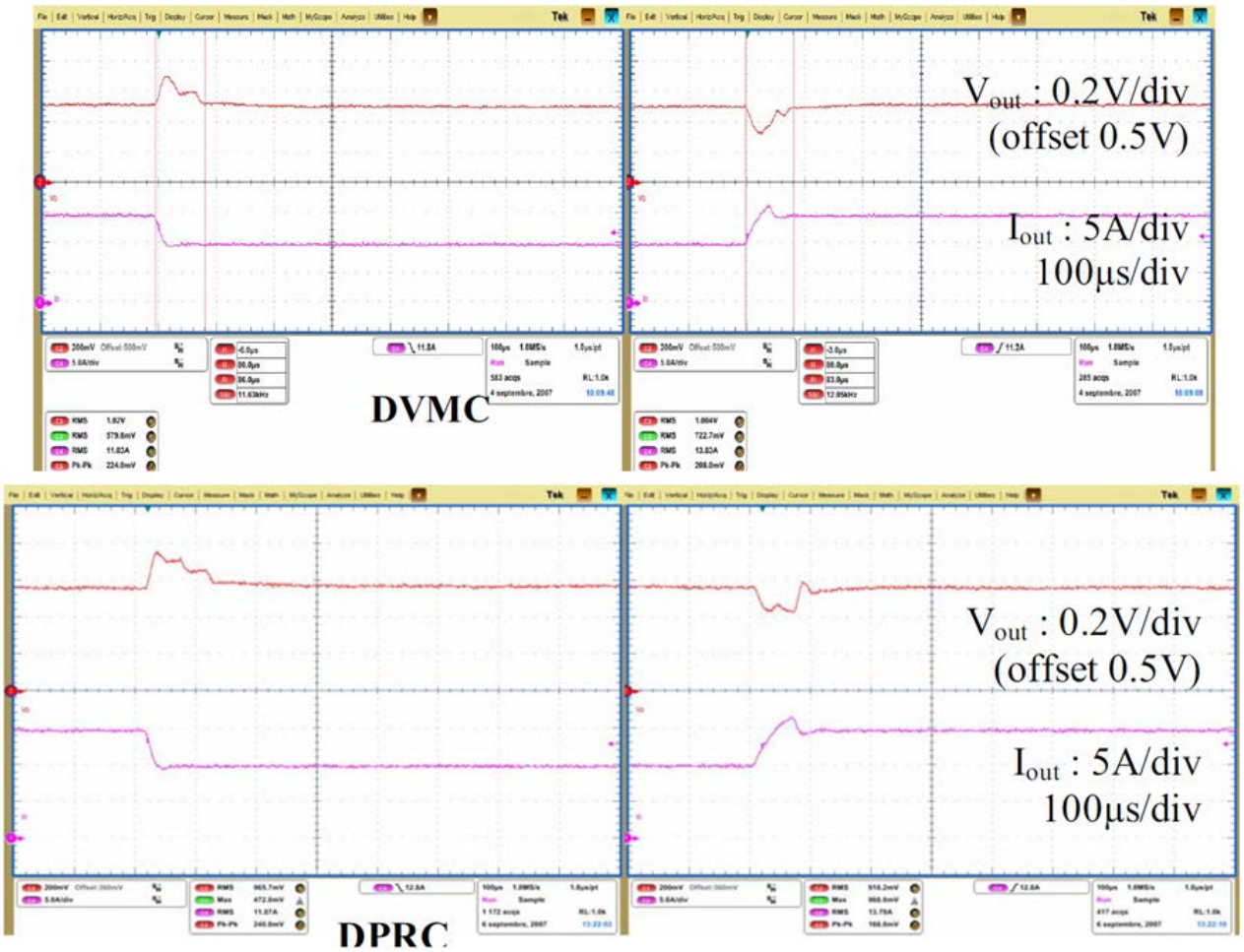

Figure 6. Output voltage and current for ΔI_{out} = 5 A using DVMC (top) and DPRC (bottom) law

Figure 6 shows a load variation of 5A (20% maximal load) using DVMC and DPRC laws respectively. The compensation network chosen has been the incremental PI due its low computational cost. We observe how dynamics is not degraded using DPRC despite of its delays are bigger. Experimental and simulation results do not offer big variations. We see also how DPRC presents a small steady state error that is not present in DVMC.

4. Conclusions

The goal of this article is to discuss about classical digital control laws and to discern the best one between voltage and current feedback regulation adapted for a high-frequency PoL converter application.

In this work, some examples of classical digital control have been introduced to show the feasibility of the design. Future works will develop new control laws and their adaptation for high-frequency PoL converters.

Therefore, we have studied both control laws by means of Matlab-Simulink models. These models uses S-functions allowing integrating the algorithm of the digital control law into the model. Then, simulations of the real system are now available. Moreover, these models help to calibrate the experimental system and to study the influence of quantification, fix-point and delays error in each control law. Furthermore, several architectures of digital compensation networks have been analyzed and compared in this revision. At this point, incremental digital PI and PID have shown enough dynamical performances.

In order to have an accurate comparison, we have implemented these experimental laws in our prototype. The results shown that DPCM does not improve the converter performances despite of the tracking of the inductor current. Moreover, the system calibration is more difficult and the computational cost of the algorithm is higher introducing larger delays that can make unstable the system. For those reasons, DPRC is preferred only when the narrow tracking of the inductor current is required. This fact is only required in high-output current PoL converters where the load variations are significant (e.g. interleaved converters for Voltage Regulator Modules). On the other side, for the low-power PoL converters, DVMC is the good strategy due to its simple implementation, low cost and fast algorithm execution.

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